A wideband high-linearity RF receiver front-end in CMOS

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Abstract

This paper presents a wideband high-linearity RF receiver front-end, implemented in standard 0.18 μm CMOS technology. The design employs a noise-canceling LNA in combination with two passive mixers, followed by lowpass-filtering and amplification at IF. The achieved bandwidth is > 2 GHz, with a noise figure of 6.5 dB, +1 dBm IIP_3, +34.5 dBm IIP_2 and <50 kHz 1/f-noise corner frequency.

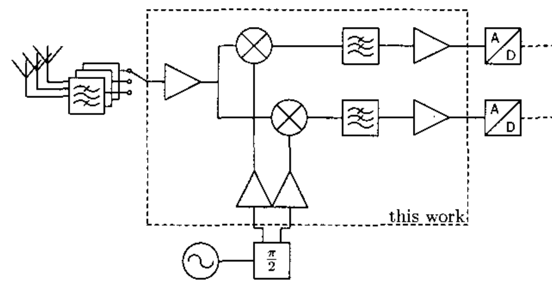

Figure 1. system overview

1. Introduction

Narrowband radio receivers have a bandwidth which is only a small fraction of the center frequency of the radio band, allowing the use of LC-tuned circuits with a high quality factor. In contrast, in wideband radio receivers the ratio between bandwidth and center frequency can be as large as two. Wideband receivers find application in for instance base stations and in analogue cable (50-850 MHz), satellite (950-2150 MHz) and terrestrial digital (450-850 MHz) video broadcasting. Moreover, a wide-band receiver can replace several LC-tuned narrowband front-ends typically used in multi-narrow-band receivers. A wide-band solution saves chip-area and fits better in the trend towards flexible radios with as much signal processing (e.g. channel selection, image rejection) as possible in the digital domain.

Some attention has been given recently to the design of wideband, multistandard receiver front-ends, e.g. [1, 2]. These designs are however not in CMOS, which hampers integration with the ever-expanding digital parts of contemporary receivers. In the field of CMOS, we are unaware of any published low-noise wideband front-ends. Some wideband LNAs however, have been published, e.g. [3, 4, 5]. Also, several CMOS receivers for satellite reception have been published [6, 7], but as they are to be used in conjunction with outdoor LNCs, their noise figures are rather high (e.g. 16 dB for [7]). This is far too high for wireless applications where the front-end is working directly at RF.

This paper presents a flexible wideband front-end for wireless receivers in a standard 0.18 μm CMOS technology. In the next section some design considerations will be discussed. In section 3 the circuit is presented. Section 4 contains measurement results and finally section 5 presents the conclusions.

2. Design considerations

A large bandwidth potentially contains many interfering signals, some of which can be very strong. This leads to very high linearity requirements. These can be relaxed by the use of RF pre-filtering as can be seen in figure 1, but still the required linearity is higher than that of a narrowband receiver, and > 0 dBm IIP_3 is preferred.

Noise requirements for a wideband receiver are generally the same as for narrowband receivers. However, low noise figures for the front-end are harder to obtain and require higher power consumption due to the unavailability of high-Q LC filters. In order to minimize power consumption for the whole receiver, this often leads to a different distribtution of NF over the various receiver subblocks, and this somewhat relaxes front-end demands.

Image rejection using an RF filter is not very attractive in wideband front-ends, because either a very high IF or a tunable RF filter is required. This suggests a zero-IF or low-IF architecture. The decision between these two depends on the standard for which receivers are designed. Different standards have different requirements for image suppression; for some signals DC offset is a problem, for others hardly so; sometimes 1/f noise is a problem (especially in CMOS), sometimes not, et cetera. Therefore, the front-end should support both.

A zero-IF receiver requires low 1/f noise at the output. This, combined with linearity demands, suggests the use of a passive mixer. Because a passive mixer doesn't have gain, a high-gain LNA is required. This LNA also has to exhibit low noise over a wide band, and input matching. This combination can be achieved by the use of noise canceling [3].

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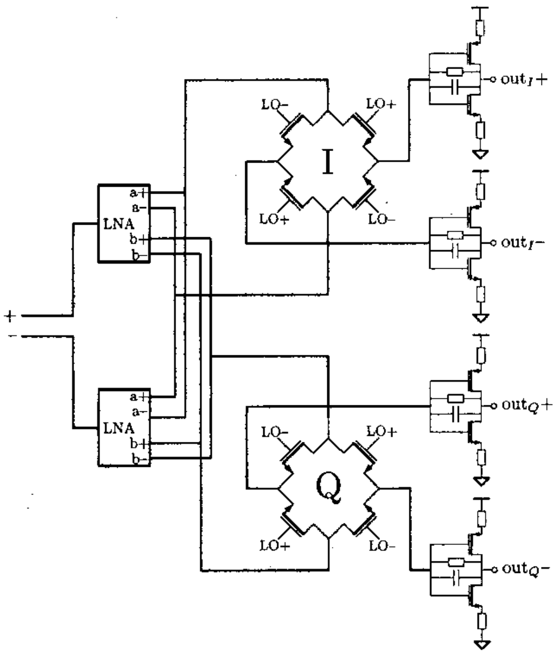

Figure 2. Overview of the implemented system, excluding the LO buffers. The schematic of the two LNA blocks is shown in figure 3.

Most commercially available RF-filters and duplexers have 50Ω input and output impedances. Therefore, in order to maximise chip re-use and flexilibity, the input impedance of the downconverter was chosen to be 50Ω, even though this is non-optimal considering power consumption. This flexiblity can be exploited by using several filters and a switch on one PCB, as shown in figure 1.

3. Circuit description

An overview of the downconverter can be seen in figure 2. It contains an LNA with current source outputs. The transistors in the mixers act as current switches, and the transimpedance amplifers at intermediate frequency convert the current into voltage again. This section discusses the design of the different parts of the downconverter.

3.1. Low-Noise Amplifier

As shown in figure 2, the LNA consists of two (equal) parts. The circuit implementation of one half of the LNA can be seen in figure 3. A fully balanced design is very much wanted to achieve low even-order distortion, which is important for wideband downconverters. This also reduces other common mode interferences and improves the power supply rejection. Both parts of the LNA have a single ended input and a differential output. Cross-coupling the outputs of these parts results in a compound amplifier with a differential input.

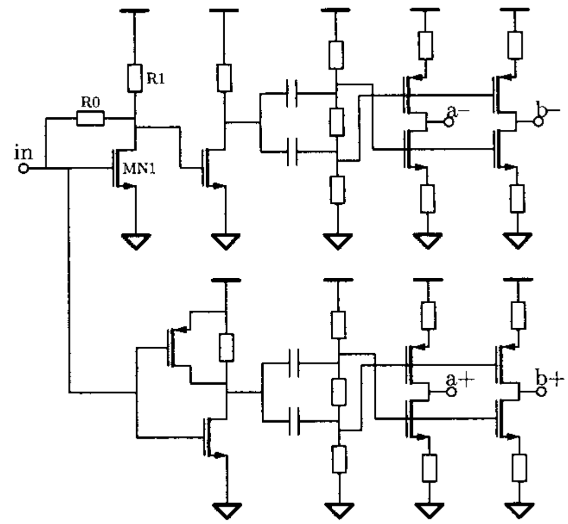

Figure 3. schematic of one half of the LNA. The full LNA is formed by cross-coupling the outputs.

The LNA in figure 3 has two separate differential current outputs, one for each mixer. This is to prevent noise degradation due to the existence of a low-ohmic current-path between the inputs of two transimpedance amplifiers during the time that both the I- and the Q-path are switched on [8]. The LNA basically consists of three cascaded stages. Each stage has a different trade-off between required gain, bandwidth, noise and linearity.

The common-source input stage with MN1 is responsible for input matching. A resistive load (R1) instead of a current source improves the bandwidth. Because this stage is an inverting amplifier, the signal is in anti-phase on the gate and drain of MN1. On the other hand, the noise current in MN1's channel produces in-phase noise voltages at these nodes (through the voltage divider consisting of R0 and the impedance of the signal source). Both signal and noise on these two nodes are inverted twice before they reach the two ouputs of the LNA. Therefore, the input signal is present on the outputs in anti-phase, while the noise of MN1 is in-phase. This is exploited to add signal contributions while cancelling the noise of MN1 [3].

Simulations show that the noise cancelling can bring the noise figure of the LNA below 3 dB. With high LNA gain, a front-end with close to 3 dB noise figure could be designed, but at the cost of linearity and bandwidth. However, noise figure was deemed less important than IIP_3 and high bandwidth. Therefore we choose to accept 6 dB NF for the front-end.

The output stages consist of inverters. To improve linearity, these stages are degenerated. In a normal inverter the gates of both the NMOST and PMOST are at the same voltage. This would normally lead to a lower gate overdrive voltage $V_{gs} - V_t$, which is bad for bandwidth and linearity. Therefore, gate overdrive voltages have been increased by the coupling capacitors and the voltage divider.

Notwithstanding the use of differential circuits, extensive on-chip supply decoupling is employed to further enhance the power supply rejection.

3.2. Mixer

Fully balanced passive mixers were used to achieve high linearity and low 1/f noise. See figure 2.

Both mixers consist of four switch transistors. These switches are driven by CMOS inverters acting as LO buffers. Because of the high output impedance of the LNA (current source), a low on-resistance of the switch transistors and the low input impedance of the following IF amplifier, variations in the channel conductivity of the switch transistors have little impact on the signal. This has two advantages. First, because variations in the conductivity caused by large signals have less impact, linearity is improved. Second, both 1/f and thermal noise in the channel current of the switches have less impact, thus allowing smaller transistors to be used, lowering the load presented to the LO buffers, and thus improving LO bandwidth. Especially the lower 1/f noise here is a big plus for zero-IF reception.

3.3. IF filter and amplifier

The IF amplifier and filter is implemented as a transimpedance amplifier with a parallel RC-combination as a feedback network. The bandwidth is 16 MHz, so that in a zero-IF configuration signals with a bandwidth of up to 32 MHz can be received, or multiple narrowband signals at the same time. To improve the LNA/mixer linearity, the IF amplifier has a low input impedance up to high frequencies. To improve the linearity of the IF amplifier itself, the transistors have been degenerated. The transistors were designed for a 1/f noise corner frequency well below 100 kHz.

4. Experimental results

The front-end was realised in a 0.18 μm standard CMOS process (figure 8). The active chip area is 800$\times$ 650 μm, most of which is taken by filter capacitors.

Measurements were done on a packaged chip (HVQFN24 package). It was mounted on a PCB made of Rogers RO4003 substrate with a thickness of 0.8 mm.

Figure 4 shows the measured voltage conversion gain as a function of input frequency, showing 200 MHz–2.2 GHz −3 dB bandwidth. The lower cut-off frequency is determined by the coupling capacitors in the LNA. At higher frequencies the conversion gain is still considerable, albeit at increased noise figure. The same figure also shows S_{11}. This is lower than -10 dB up to 1.9 GHz.

Figure 5 shows the noise figure, at two different supply voltages. This is the noise figure when taking image rejection into account.

Figure 6 shows the output noise of the downconverter. This was measured using a differential probe. Note the 1/f noise corner frequency of <50 kHz.

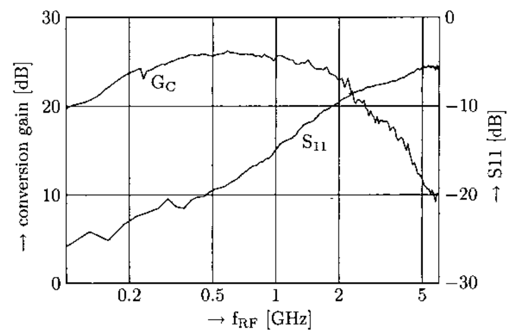

Figure 4. voltage conversion gain vs. input frequency (output frequency=5 MHz) and S_{11} (V_{dd}=1.8 V)

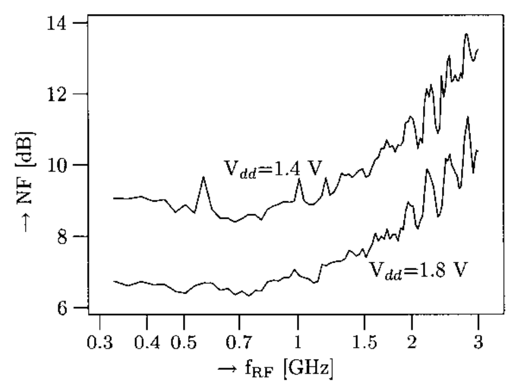

Figure 5. Noise figure (taking image rejection into account) versus input frequency (output frequency=10 MHz)

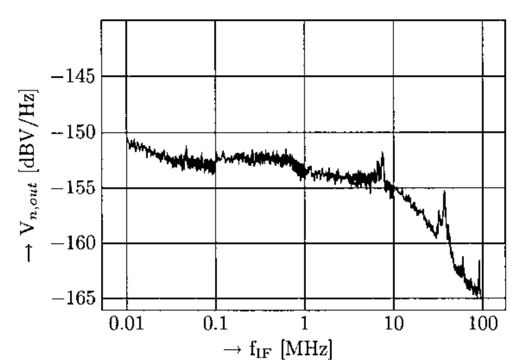

Figure 6. output noise vs. frequency. LO=1 GHz, V_{dd}=1.8 V

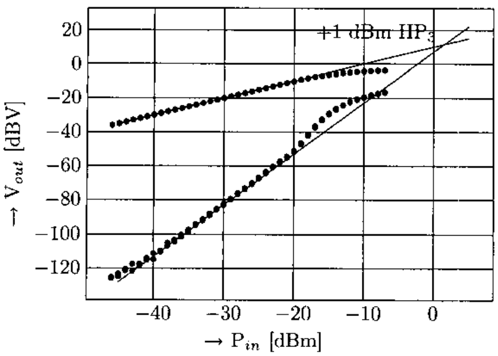

Figure 7. Two-tone 3rd order intermodulation distortion. input at 1005 and 1006 MHz, V_{dd}=1.8 V.

Table 1. Key performance measurements

	Vdd = 1.4 V[a]	Vdd=1.8 V
−3 dB BW	0.2 – 2.2 GHz	0.2 – 2.2 GHz
G_C	21	25
$NF_{DSB,min}$	8.5 dB	6.5 dB
IIP_3	+1 dBm	+1 dBm
IIP_2	+31 dBm	+35 dBm
−1 dB CP	-14.5 dBm	-16 dBm
LO radiation @1 GHz	-47 dBm	-47 dBm
P	130 mW	200 mW

[a]supply of LO buffers at 1.8 V

Figure 7 shows an IIP_3 plot, measured with an LO frequency of 1 GHz and two input signals at 1005 and 1006 MHz. The IIP_3 is +1 dBm (OIP_3: 13 dBV), which is considerably better than typically found for narrowband receivers. IIP_2 is +35 dBm and the -1 dB compression point is -16 dBm. A summary of the measurement results can be found in table 1.

5. Conclusions

A wideband downconverter front-end has been designed and realised in 0.18 μm CMOS. It achieves 25 dB conversion gain, >2 GHz bandwidth, an IIP_3 of +1 dBm (OIP_3: 13 dBV) and an IIP_2 of +35 dBm, at 200 mW power consumption. The noise figure is 6.5 dB and the 1/f corner frequency is below 50 kHz.

Overall, the results indicate that a high-linearity flexible wideband downconverter is feasible in CMOS, but has its price especially in power consumption and higher noise figure.

6. Acknowledgements

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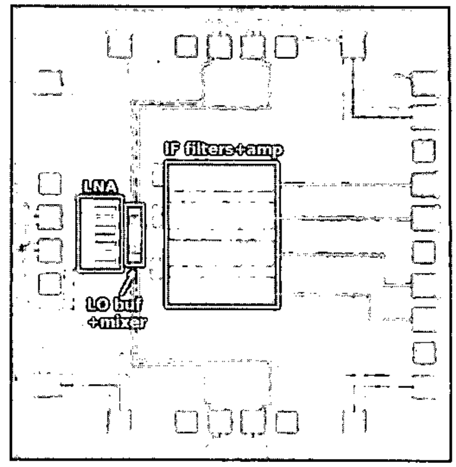

Figure 8. Chip micrograph

7. References

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