GATE-DRAIN CAPACITANCE COMPENSATION TECHNIQUE FOR TRIODE MOS TRANSCONDUCTORS

Indexing term: Metal–oxide–semiconductor devices

It is shown that phase errors in triode MOS transconductors due to gate-drain capacitances can largely be compensated using a crosscoupled quad of transistors with balanced input voltages. The compensation is insensitive to temperature and IC-processing variations and remains good even when the transconductance of the triode MOS transistors is varied.

Introduction: In the past few years several triode MOS transconductors for use in continuous-time integrated filters have been proposed.[1–4] In these transconductors, MOS transistors operating in the triode region are used as linear voltage-to-current conversion elements, by forcing their drain-source voltages to be constant. It was shown that these transconductors have attractive properties for filter applications, such as a large voltage handling capability with good linearity, low noise, a large transconductance control range and a low sensitivity for common voltages.

It is well known that transconductance-C filter characteristics are very sensitive to phase errors in the transconductors.[5] In triode transconductors the gate-drain capacitance is an important cause of these errors. In this Letter it will be shown that these phase errors can largely be compensated for by using a crosscoupled quad of triode MOS transistors. Limitations and drawbacks of the technique will be discussed and simulation results will be presented.

Phase error of cross coupled quad: Fig. 1 shows a crosscoupled quad of MOS transistors (assume M1a = M1b, M2a = M2b and equal bulk-source voltages). Just as in References 1–4, the

drain-source voltages of these transistors are kept equal and constant, and their gates are driven by voltages $v_{in}/2$, balanced around a certain common level V_{CM}. The phase error of the

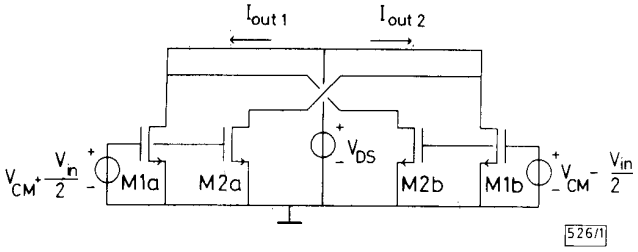

Fig. 1 *Crosscoupled quad of triode transistors*
$W_2 = W_1/n \quad L_2 = nL_1$

cross coupled quad can be estimated using the small signal equivalent circuit of Fig. 2. In this Figure C_{gd1} and C_{gd2} are the intrinsic gate-drain capacitances of M1 and M2 and g_{m1} and g_{m2} are their transconductances. The transfer function of the circuit can be written as

$$\frac{i_{out}}{v_{in}} = \frac{i_{out1} - i_{out2}}{v_{in}} = (g_{m1} - g_m)\left(1 - j\omega \frac{C_{gd1} - C_{gd2}}{g_{m1} - g_{m2}}\right) \quad (1)$$

Without transistors $M2$, i_{out} would exhibit a phase lag with respect to v_{in} because of the right half plane zero at g_{m1}/C_{gd1}.

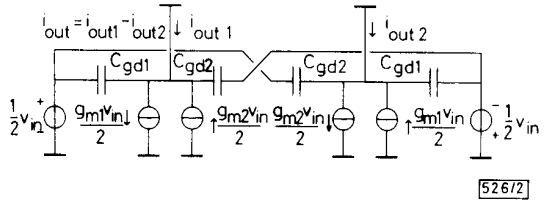

Fig. 2 *Small signal equivalent circuit of crosscoupled quad*

Note that this phase shift can be significant because C_{gd} can amount to half the gate-oxide capacitance in the triode region. From eqn. 1 it can be seen that this phase shift is eliminated for $C_{gd2} = C_{gd1}$. The dependence of g_m and C_{gd} on transistor dimensions and biasing can be modelled as[6]

$$g_m = \frac{W}{L} \mu C_{ox} V_{DS} \quad (2a)$$

$$C_{gd} = \frac{2}{3} WLC_{ox} \frac{\alpha^2 + 2\alpha}{(\alpha + 1)^2} \quad (2b)$$

where $\alpha = 1 - V_{DS}/V_{DSSAT}$ and W, L, μ, C_{ox} and V_{DSSAT} have their usual meaning.[6] For $v_{in} = 0$, all transistors have equal α values. Therefore C_{gd1} and C_{gd2} can be made equal by making gate areas W_1L_1 and W_2L_2 equal. Furthermore, obviously g_{m2} should not be equal to g_{m1}, because zero output current would result. Both conditions can be satisfied by choosing

$$W_2 = \frac{1}{n} W_1 \quad \text{and} \quad L_2 = nL_1 \qquad (n \geq 1) \quad (3)$$

Thus the currents through capacitors C_{gd1} are compensated for by equal but opposite currents through C_{gd2}, under the condition that balanced input voltages are applied. Note that if transistors M1 and M2 are located close to each other, the compensation will be insensitive to temperature and IC-processing variations, as these will largely affect C_{gd1} and C_{gd2} in the same way. Moreover, because C_{gd1} and C_{gd2} depend on V_{DS} in the same way (α dependence in eqn. 2*b*), the compensation remains good when the transconductance is changed by means of V_{DS}. This property can be very useful in programmable filter applications.

Limitations of technique: One limitation for the achievable degree of compensation results from the fact that the effective value of W and L on an actual chip deviates from the designed value. Although these deviations may be systematic (e.g. ΔW and ΔL due to under etching), their relative influence on C_{gd1} and C_{gd2} will in general be different, resulting in a C_{gd} difference ΔC_{gd}. Further, gate-drain overlap capacitances, which are proportional to W, contribute to ΔC_{gd}. Apart from these systematic errors, random mismatches in W, L and C_{ox} affect ΔC_{gd}.

Another potential limitation of the technique is formed by nonquasistatic behaviour of MOS transistors operating at high frequencies. Therefore an alternative expression for eqn. 1 was derived using the 'first order nonquasistatic model' described by Tsividis.[6] This expression also predicts a low phase error over a large frequency range (the numerator and denominator have equal constant and $j\omega$ terms).

Finally a limitation might result from the dependence of α on v_{in}. In fact, thus far the small signal behaviour around $v_{in} = 0$ was analysed. In that case the value of α is equal for M1 and M2, because both V_{DS} and V_{DSSAT} of M1 and M2 are equal. As V_{DSSAT} depends on V_{GS}, α of all transistors will no longer be equal for $v_{in} \neq 0$. However, the value of α of M1*a* and M2*a* will be equal, and that of M1*b* and M2*b* will also be equal. It can be shown that this only results in an AC current that is common for i_{out1} and i_{out2}. This common current is cancelled when $i_{out1} - i_{out2}$ is used as the output variable, which is usually the case in filter applications.

Drawbacks of compensation technique: Because of the addition of compensation transistors M2, the input capacitance is doubled and the bias current is enlarged by a factor $(1 + 1/n^2)$ with respect to the uncompensated situation. Furthermore, the output noise current is enlarged while the overall transconductance is decreased, resulting in a sigal to noise ratio deterioration. It can be shown that the addition of the compensation transistors does not affect the linearity, so that the maximum output signal power is reduced by a factor $[(g_{m1} - g_{m2})/g_{m1}]^2$. The output noise power is enlarged by a factor $(g_{m1} + g_{m2})/g_{m1}$ for thermal noise and by a factor $(g_{m1}^2 + g_{m2}^2)/g_{m1}^2$ for flicker noise. As the increase is always larger for thermal noise, a worst-case estimate of the signal to noise ratio after compensation can be made, using eqn. 2*a* and eqn. 3 and assuming only thermal noise

$$S/N_{comp.} = S/N_{uncomp.} \frac{(n^2 - 1)^2}{(n^2 + 1)n^2} \quad (4)$$

Eqn. 4 predicts a loss in S/N ratio that decreases with increasing n. For practical values of n between 2 and 10, the loss in S/N ratio varies between 3·5 dB and 0·13 dB.

Table 1 MODEL AND DEVICE PARAMETERS FOR M1 USED IN SIMULATIONS

LEVEL	3	*PB*	0·94	*NFS*	10×10^9
LD	227×10^{-9}	*CJ*	336×10^{-6}	*TOX*	25×10^{-9}
WD	696×10^{-9}	*CJSW*	134×10^{-12}	*XJ*	350×10^{-9}
VTO	0·627	*MJ*	0·97	*VMAX*	209×10^3
KP	693×10^{-7}	*MJSW*	0·65	*DELTA*	0·211
GAMMA	0·73	*CGSO*	120×10^{-12}	*THETA*	347×10^{-4}
PHI	0·60	*CGDO*	120×10^{-12}	*ETA*	0·1
RSH	24	*CGBO*	340×10^{-12}	*KAPPA*	8·83
JS	150×10^{-7}	*NSUB*	224×10^{15}	*ΔTOX*	1%
W	50×10^{-6}	*AD, AS*	750×10^{-12}	*NRD, NRS*	0·04
L	10×10^{-6}	*PD, PS*	130×10^{-6}		

were examined by means of PSPICE simulations using the level 3 model with the parameters listed in Table 1. The device parameters of M1 are also given in the Table, and those of M2 were adapted in accordance with the value of n, assuming a rectangular MOS layout. Simulations of the THD of the differential output current confirmed the statement that the addition of compensation transistors M2 does not deteriorate the input swing and distortion. In fact, the THD at high frequencies is even improved.

To evaluate the effectiveness of the phase compensation, the frequency $f_{\Delta\Phi=1^\circ}$ was determined where the phase of the output current $i_{out1} - i_{out2}$ deviates 1 degree from its low frequency value. Both the SPICE level 3 MOS model and the 'first-order nonquasistatic model' described by Tsividis[6] were used. The worst-case value of $f_{\Delta\Phi=1^\circ}$ was determined allowing for 1% random mismatch in TOX. Table 2 gives the results for $V_{CM} = 2{\cdot}5$ V and several values of n and V_{DS}. The results indicate that significant improvements in $f_{\Delta\Phi=1^\circ}$ are achievable, especially for low values of V_{DS} and n. For high values of V_{DS}, nonquasistatic MOS behaviour is the main cause of phase errors, and for low values of V_{DS}, systematic deviations in W and L and random mismatch limit the compensation. Table 2 also shows how the worst-case S/N ratio deterioration (assuming only thermal noise) depends on n. The values are in accordance with those predicted by eqn. 4.

Summarising, simulations indicate that a significant moderate decrease of the S/N ratio (e.g. 3·2 dB).

Table 2 $f_{\Delta\Phi=1^\circ}$ AND S/N RATIO DETERIORATION FOR SEVERAL VALUES OF n AND V_{DS}

	Worst case $f_{\Delta\phi=1^\circ}$ (MHz)			S/N deterioration
	$V_{DS} = 0{\cdot}01$ V	$V_{DS} = 0{\cdot}1$ V	$V_{DS} = 1$ V	(all V_{DS} values)
				dB
Uncompensated	0·026	0·27	3·5*	—
$n = 2$	0·59	6·0	35*	3·2
$n = 3$	0·38	3·9	22*	1·4
$n = 5$	0·23	2·3	12*	0·4
$n = 10$	0·10	1·1	6·1*	0·2

* Limited by nonquasistatic effects

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