Cascadable CMOS current gain cell with gain insensitive phase shift

E.A.M. Klumperink

Indexing terms: CMOS integrated circuits, Transconductors

It is shown that by using a complementary circuit topology, electronically variable gain in combination with a gain insensitive phase shift can be achieved. A cascadable CMOS current gain cell based on this concept is proposed, together with a linearisation technique for this circuit.

Introduction: Circuits that amplify a signal by an electronically variable amount while maintaining a constant phase shift can be very useful. In piezoelectrically driven resonators [1] and other oscillator-like circuits, they enable amplitude control without affecting the resonance frequency and in integrated filters they enhance tuning flexibility and simplify design. Apart from a variable gain and gain insensitive phase shift, such circuits should have a linear transfer function and low noise. Recently several current gain cell circuits have been proposed [2-4] that feature a variable gain in combination with a constant bandwidth, suggesting a gain independent phase shift property. However, although this is true for the basic cell, extra current mirrors are usually needed to separate the output signal current from the biasing current or to cascade single cells. Because these bias currents largely vary with the gain setting, the bandwidth of the mirrors also varies significantly, which introduces considerable phase shift variations. This Letter shows that much lower phase shift variations arise in a complementary circuit topology without mirrors.

Principle of operation: The circuit diagram of the new complementary current gain cell is depicted in Fig 1. The input transistors M1-M4 implement a differential I-V convertor, and output transistors M5-M8 form a transconductance stage, so that overall a current amplifier results. The circuit can handle bidirectional input currents and produces bidirectional output currents. The biasing circuit (current sources I_{IN0} and I_{OUT0} and M9-M10 (matched to M1-M4)) force the input voltages and output currents to zero in the quiescence condition. Thus the output signal current is readily available and cells can directly be cascaded without level shift problems, without using current mirrors.

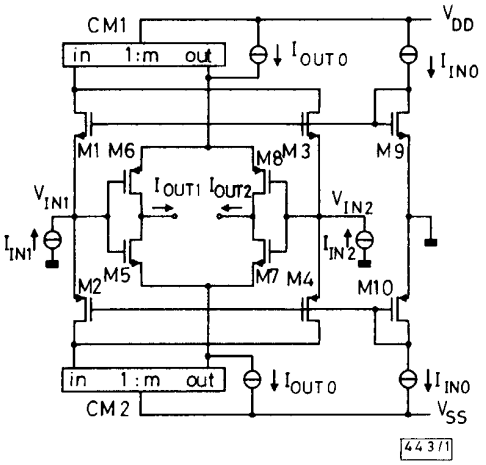

Fig. 1 *CMOS current gain cell with complementary topology*

The input I-V conversion is linear if a square-law model for the MOSTs is used (strong inversion, saturation) and the transconductance parameters of the *p*- and *n*MOST are chosen equal [5]. The output V-I conversion, the sum of a *n*MOST and *p*MOST long tail pair transfer function, can be linearised by adding a tail current proportional to the squared input voltage [2]. A detailed analysis shows that the desired current is already present in the sum of the drain currents of the input transistors, so that it can be added to tail currents I_{OUT0} by means of current mirrors CM1 and CM2. However, the body effect of the input transistors affects the compensation. This effect can be accounted for, however, by changing the mirror ratio m. If a first order body effect model is used, assuming a linear increase of the depletion charge with increasing channel-substrate voltage [6], the resulting optimum current mirror ratio is

$$m_{opt} = \frac{k_{OUT}}{k_{IN}} \cdot \frac{1}{\alpha^2} = \frac{k_{OUT}}{k_{IN}} \cdot \frac{1}{\left(1 + \frac{\gamma}{2\sqrt{\phi_B + V_{SB}}}\right)^2} \quad (1)$$

where k_{IN} and k_{OUT} are the transconductance parameters $\mu C_{ox}W/L$ of the input and output stage, and α is a body effect parameter which can be related to the widely used body-effect model with parameters γ and ϕ_B, by evaluating the derivative of the threshold voltage with respect to V_{SB} in the biasing point. Based on this model, the equivalent differential input resistance becomes

$$R_{IN} = \frac{V_{IN1} - V_{IN2}}{I_{IN1} - I_{IN2}} = \frac{1}{2\sqrt{k_{IN} \cdot \alpha \cdot 2 \cdot I_{IN0}}} \quad (2)$$

For $m = m_{opt}$, the overall transfer function is linear and the current gain becomes

$$A_i = \frac{I_{OUT1} - I_{OUT2}}{I_{IN1} - I_{IN2}} = -m_{opt}\sqrt{1 + \frac{I_{OUT0}}{2 \cdot m_{opt} \cdot I_{IN0}}} \quad (3)$$

Eqn. 3 shows that the current gain A_i equals $-m_{opt}$ for $I_{OUT0} = 0$ and can be varied by means of both I_{OUT0} and I_{IN0} (I_{OUT0} can be both positive and negative). The above equations hold for transistors operating in strong inversion and saturation, which restricts the operating range. Applying the corresponding boundary conditions [6] to the circuit results in theoretical maximum values for $|I_{IN1}-I_{IN2}|$ of $\times I_{IN0}$ for $|A_i|/m_{opt}$ and of $8 \times I_{IN0} \times |A_i|/m_{opt}$ for $|A_i|$ smaller than m_{opt}. Furthermore the load of the gain cell must be such that the output voltages remain between $(V_{IN}-V_{T0P})/\alpha$ and $(V_{IN}-V_{T0P})/\alpha$ for both circuit halves.

Phase shift properties: The dominant pole of the gain cell is determined by the equivalent input resistance and the input capacitance with respect to ground. Detailed analysis shows that for balanced input currents, the common source nodes of the long tail pairs have constant voltages (in fact the cell can be biased by constant voltage sources [5]). Thus almost all parasitic capacitances of the MOSTs operate either at constant voltages or contribute to C_{IN}, which gives the cell a first order behaviour over a large frequency range. The equivalent input resistance given by eqn. 2 is independent of I_{OUT0}. Because C_{IN} is also independent of I_{OUT0}, the phase shift of the gain cell does not change, provided that I_{OUT0} is used to vary the gain. Only the gate-drain capacitance of the output transistors in combination with the transconductance of the output stage gives a gain dependent right half-plane zero. However, because this zero is often located at much higher frequencies than the dominant pole, it introduces relatively small phase variations. Furthermore, if necessary, it can be further reduced by adding crosscoupled compensation capacitors preferably implemented by matched MOSTs.

Table 1: Most important SPICE level 3 simulation parameters used

	KP	VT0	GAMMA	PHI	THETA
	$\mu A/V^2$	V	$V^{0.5}$	V	V^{-1}
*n*MOS	77	0.60	0.61	0.76	0.05
*p*MOS	33	−0.60	0.52	0.70	0.16

Simulation and measurement results: The DC transfer function of the gain cell was examined by means of measurements using 125/10 *p*MOS and 50/10 *n*MOS breadboard transistors (k_N . k_P), fabricated in a 2.5μm CMOS process. A value m_{opt} = 70 was found using eqn. 1 with average values for the *p*- and *n*MOST parameters given in Table 1. For experimental reasons mirrors with bipolar transistors and resistors were used (saturation voltage 0.5V). The solid lines in Fig. 2 show the measured differential gain as a function of the input current for balanced input currents and for several values of I_{OUT0} and constant I_{IN0} = 20μA. When compared to the situation without compensation (m = 0, dashed lines in Fig. 2), it is clear that the linearity is significantly improved. Varying m±10% around its optimum does not drastically change these curves, which indicates that the compensation is not highly critical. The theoretical input frame is roughly related to $8 \times I_{in0}$ as expected (dotted lines in Fig. 2). However, the gain increases less progressively than predicted by eqn. 3, which is mainly due to the mobility reduction effect. The overall gain control range was 0.3 – 2.9, with a $THD \leq 1\%$ for input currents up to 75% of their theoretical maximum. Larger nominal gain values can easily be implemented by choosing k_{OUT}/k_{IN} larger than 1. Simulations indicate that mismatches between k_P and k_N up to 25% contribute less than 0.4% to the *THD*.

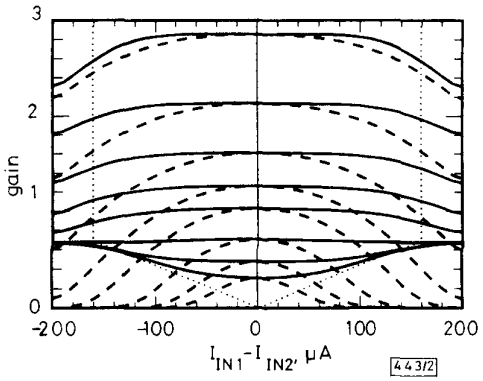

Fig. 2 *Differential gain of the cell for I_{IN0} = 20μA and m = 0.7 and m = 0*

——— *m* = 0.7: I_{OUT0} = −21, −14, 0, 28, 56, 108, 216, 432μA
– – – – *m* = 0: I_{OUT0} = 7, 14, 28, 56, 84, 136, 244, 460μA

The AC behaviour of the gain cell was examined by simulation, because breadboard parasitics would dominate measurements. Simulations showed an equivalent thermal input noise varying between 4.5 and 1.5 pA/√Hz over a gain range 0.3 – 2.9. The simulated bandwidth f_{-3dB} remained constant at 11MHz and the phase shift varied less than 0.2° at 1MHz. When current mirrors with the same transistors are used to subtract the output currents, a significantly larger phase shift variation of 12° is found.

Acknowledgments: The author would like to thank E. Laarhuis for her contribution to the analysis of the circuit, G. Boom for IC fabrication and K. Bult for useful comments.

© IEE 1993
10 September 1993
Electronics Letters Online No: 19931325

E. A. M. Klumperink (*MESA Research Institute, University of Twente, Department of Electrical Engineering, PO Box 217, 7500AE Enschede, The Netherlands*)

References

1 VAN MULLEM, C.J., VAN DAM, F.W.A., FLUITMAN, J.H.J., and WALLINGA, H.: 'Towards a micromachined silicon integrated resonator'. Proc. 7th Int. Conf. on Solid-State Sensors and Actuators, 7-10 June 1993, (Yokohama, Japan), pp. 787–7990
2 KLUMPERINK, E.A.M., and SEEVINCK, E.: 'MOS current gain cells with electronically variable gain and constant bandwidth', *IEEE J. Solid-State Circuits*, 1989, **SC-24**, (5), pp. 1465–1467
3 ADAMS, W.J., and RAMIREZ-ANGULO, J.: 'Extended transconductance adjustment/linearisation technique', *Electron. Lett.* 1991, **27**, (10), pp. 842–844
4 WANG, Z.: 'Two CMOS large current-gain cells with linearly variable gain and constant bandwidth', *IEEE Trans. I: Fundamental Theory and Applications*, 1992, **39**, (12) pp. 1021–1024
5 KLUMPERINK, E.A.M., and JANSSEN, H.J.: 'Complementary CMOS current gain cell', *Electron. Lett.*, 1991, **27**, (1), pp. 38–39
6 WALLINGA, H., and BULT, K.: 'Design and analysis of CMOS analog signal processing circuits by means of a graphical MOST model', *IEEE J. Solid-State Circuits*, 1989, **SC-24**, (3), pp. 672–280