A CMOS TRIODE TRANSCONDUCTOR

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Abstract

A novel versatile CMOS voltage to current converter is presented. The conversion transistors operate in the triode region. Key points are: high linearity (THD<0.4% for $6V_{pp}$ inputs) thanks to a novel compensation technique, large tuning range of the transconductance (factor 100), floating inputs and a resulting good CMRR.

Introduction

Linear CMOS voltage to current converters can be classified in two groups: The first group has conversion transistors operating in saturation. The linearization is in most cases obtained by exploiting the transistor's square law behavior [1-3]. The second class of VI converters has conversion transistors operating in nonsaturation; the triode region [4-6]. The advantages compared to the square-law converters are a higher linearity and a larger tuning range of the transconductance.

This paper describes a novel versatile triode VI converter with floating inputs, having a good linearity and a large transconductance tuning range.

Basic principle

Using a simple model, the drain current of an MOS transistor in triode region can be written as:

$$I_d = \beta V_{ds} \left[(V_{gs} - V_t) - \tfrac{1}{2} V_{ds} \right]$$

$$\text{with} \quad \beta = \frac{\mu C_{ox} W}{L} \qquad (1)$$

If the drain-source voltage V_{ds} is held constant then the triode transistor has a linear V_{gs} to I_d transfer.

The most obvious way to keep V_{ds} constant is to add a (folded) cascode transistor to the triode transistor. A problem is now that any I_d variation of the triode transistor results in a V_{gs} variation of the cascode transistor. This in turn results in a V_{ds} variation of the triode transistor since the gate of the cascoding device is normally biased at a constant voltage. The result of this is nonlinearity in the voltage to current conversion.

To keep V_{ds} after all constant, feedback is generally applied [4,5] resulting in a constant V_{ds} at least for low frequencies. In reference [6] no special circuitry is added to reduce the variation in V_{ds} but the cascode transistor has a very large aspect ratio.

This paper makes use of an alternative way to keep V_{ds} constant: compensation.

The basic principle is given in figures 1 a and b. In figure 1^a the triode transistor M1 is cascoded with a transistor M2 operating in saturation. The gate voltage of M2 is not connected to a static voltage source but to a *dynamic* bias voltage: a static bias plus a copy of the gate-source voltage of M2; $V_{bias} + V_{gs2}$. The result is that if V_{gs2} is modulated, V_{ds1} will remain constant and equal to V_{bias}.

The question is how to generate this dynamic bias voltage. The solution is shown in figure 1^b. The drain current of M1 is split in two equal parts by M2 and M3. The output current flowing through M2 is therefore duplicated in M3 and mirrored into the

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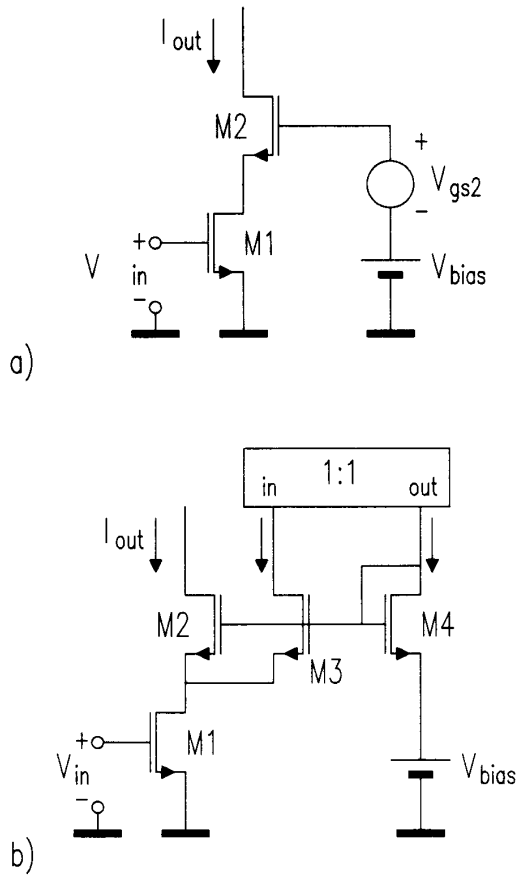


figure 1 *a) basic principle of V_{gs2} compensation.*
b) realization of the dynamic bias voltage

diode connected transistor M4. If M3 = M4 then $V_{gs3} = V_{gs4}$, resulting in proper biasing of the gate of M2 as proposed in figure 1^a.

The circuit of figure 1^b has still several disadvantages: the input is not (truly) floating nor differential and an AC current flows through the bias voltage source. This is overcome in the circuit of figure 2.

The complete circuit

Differential circuits have better linearity thanks to the cancellation of even order distortion terms. The circuit of figure 2^a is the differential version of figure 1^b. The triode transistors performing the linear voltage to current conversion are M1A and M1B. The current mirrors have been replaced by a cross coupled structure with current sources $2I_s$. The voltage source V_{bias} of figure 1^b is replaced by a transistor in triode region (M1C). Thanks to the differential structure the current through M1C is constant (see below) and therefore the drain-source voltage of M1C (V_{ds1c}) will also be constant. The drain source voltages of M1A and M1B are equal to V_{ds1c} due to the circuit configuration similar to fig. 1^b. V_{ds1c} is set up with the voltage source V_b and the current $2I_s$. Note that when no differential input voltage is present it follows that $V_{gs1A} = V_{gs1B} = V_b$ since M1A = M1B = M1C. The transistors M1A, M1B and M1C now all have drain currents equal to $2I_s$ and the transistors M2-M4 all have quiescent currents equal to I_s. The voltage source V_b is implemented by means of a diode connected transistor with constant drain current as shown in figure 2^b. If a positive input voltage is applied to the circuit, the currents in the branches flow as illustrated with arrows. It can be easily argued that the current through M1C is constant indeed. Note that the input voltage is not restricted to a certain common-mode voltage level; the inputs are really floating resulting in a good CMRR (determined by the output impedances of the current sources).

Keeping V_b constant, V_{ds1C} can be varied with I_s. Using equation (1) V_{ds1c} can be solved:

$$V_{ds1c} = (V_b - V_t) - \sqrt{(V_b - V_t)^2 - \frac{4I_s}{\beta_1}} \qquad (2)$$

V_{ds1C} equals V_{ds1A} and V_{ds1B} and thus the transconductance of the V-I converter can be written as:

$$gm = \frac{I_{out+} - I_{out-}}{V_{in+} - V_{in-}} = \frac{1}{2}.\beta_1.V_{ds1c} =$$

$$\frac{1}{2}\beta_1\left[(V_b - V_t) - \sqrt{(V_b - V_t)^2 - \frac{4I_s}{\beta_1}}\right] \qquad (3)$$

The transconductance can be tuned with the tail current I_s. If the transistors M1A, M1B and M1C operate in deep triode i.e. $2I_s << \frac{\beta}{2}(V_b - V_t)^2$ then

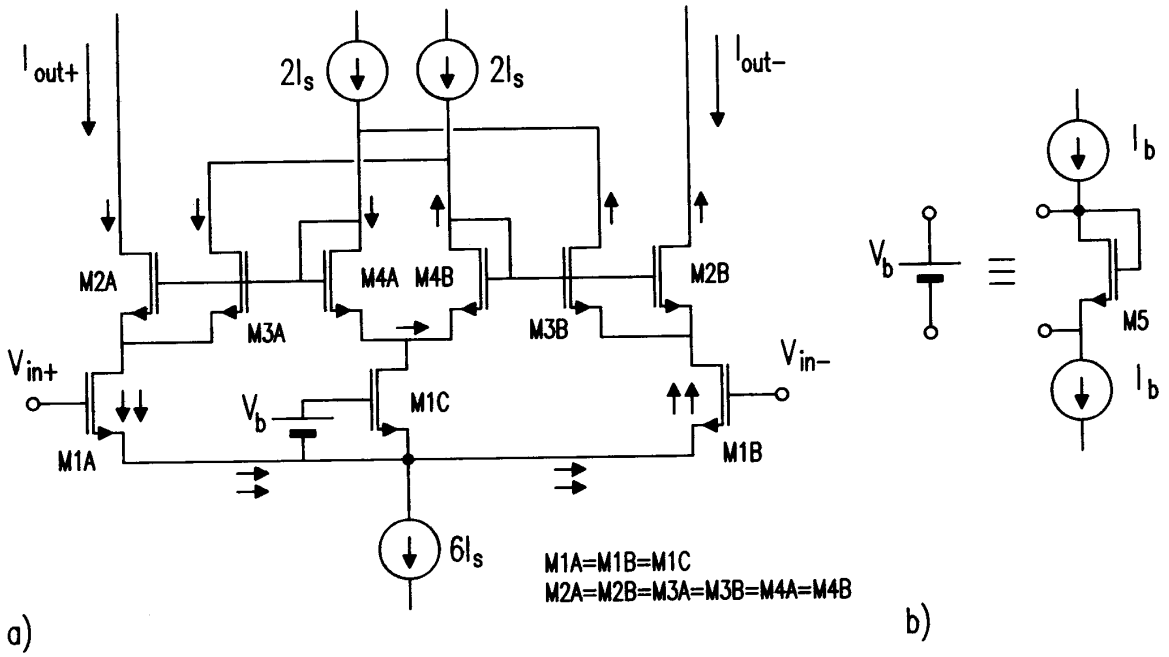


figure 2 a) The complete transconductor circuit. *b) realization of the voltage source V_b.*

expression (3) can be simplified into:

$$gm \approx \frac{I_s}{(V_b - V_t)} \qquad (4)$$

Distortion

Although the transconductor is linear according the simple MOS model of equation (1) there will be some small nonlinearities if a more sophisticated model is used. If there is *no mismatch* in the circuit the main source of distortion will be mobility reduction. (commonly modeled with θ, typically between 0.05 and 0.5 V^{-1}) The distortion is then only odd order distortion since the even harmonics are canceled in a perfect differential structure. It can be shown that the total harmonic distortion is now dominated by the third order term:

$$HD3 \approx \frac{1}{16}\left[\frac{\theta}{(1+\theta(V_b - V_t)}\right]^2 \cdot |V_{in}|^2 \qquad (5)$$

The ripple in V_{ds} of M1A and M1B depends on matching. If the matching of all transistors and current sources is ideal, V_{ds} is perfectly constant and eq. (5) is valid. A mismatch in β and V_t will result in a ripple in V_{ds}. For very low values of V_{ds} this ripple will cause additional second and third order distortion and therefore a lower limit of the V_{ds1} and transconductance is imposed. Monte Carlo simulations of the complete circuit (including current sources) show that for a typical β mismatch of 1% and V_t mismatch of 1mV the variation in V_{ds} is several millivolts depending on I_s. For larger V_{ds} levels (V_{ds}=200mV) the distortion is still mainly third order distortion (HD3 ≈ 0.5% for $6V_{pp}$ inputs). For lower V_{ds} levels (V_{ds}=10mV) the distortion consists of second and third order distortion (HD2 ≈ 0.3% and HD3 ≈ 0.2% for $6V_{pp}$ inputs)

Bandwidth

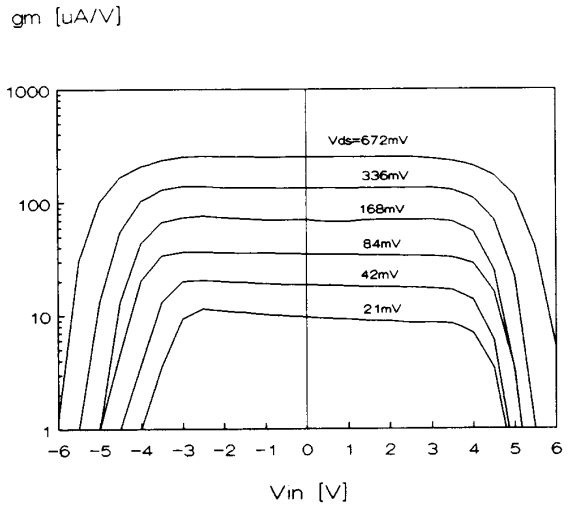
If, like in equation (4), the transistors M1 are assumed to operate in deep triode, the estimated bandwidth of the circuit becomes:

$$\omega_{-3dB} \approx \frac{2.r_{ds1}.gm_2^2}{3.C_{gs2}} \qquad (6)$$

Where r_{ds1} is the small-signal drain-source resistance of the transistors M1, gm_2 is the transconductance and C_{gs2} is the gate-source capacitance of the transistors M2-M4. Simulations using typical values for a 3μm CMOS process result in 1-70MHz bandwidth depending on I_s.

Experimental results

At this moment a test chip is being processed. The experimental results now available were obtained from a breadboard realization built with commercially available CA3600 CMOS-transistor arrays. The transconductance was measured for different tail currents I_s (19μA..600μA) and corresponding different values of V_{ds} (21mV..672mV). The voltage V_b was chosen equal to V_t+2V. The results are given in figure 3. The nonlinearities are mainly due to mobility reduction and mismatch. As expected the effects of mismatch dominate at small V_{ds} values. The transconductance was tuned from 10μA/V to 250μA/V, which is a factor 25 in transconductance. An on-chip realization will have a larger tuning range owing to the better matching on chip. Simulations, taking account of mismatch, predict a factor 100 transconductance tuning range. The measured THD was less than 0.4% for $6V_{pp}$ input voltages (V_{ds}=336mV). This THD consists of mainly second harmonics caused by mismatch.



Conclusions

A Novel transconductor is presented. The linearity is high (THD < 0.4% for $6V_{pp}$ input signals on a breadboard) The transconductance can be tuned over a wide range (factor 25 on breadboard, factor 100 expected on chip). The input voltages are not restricted to a common mode level; the transconductor has floating inputs resulting in a good CMRR.

Applications can be found in the field of OTAs, (programmable) filters, (tunable) amplifiers, automatic gain control etc.

acknowledgment

The authors wish to thank R.F. Wassenaar and H. Wallinga for fruitful discussions. This work was sponsored by the Dutch IOP (innovative research projects program) program.

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Figure 3 Measured transconductance versus differential input voltage ($V_{in} = V_{in+} - V_{in-}$) for several values of V_{ds}(Is). (breadboard)