ON THE REDUCTION OF THE THIRD ORDER DISTORTION IN A CMOS TRIODE TRANSCONDUCTOR

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ABSTRACT

This paper presents a linearisation technique which aims to cancel out the third order distortion of a CMOS triode transconductor due to the mobility reduction effect of the conversion transistors. The transconductor consist of a parallel operating voltage and current biased differential pair. It is realised in a 0.8μm CMOS process. Simulation results, obtained with state-of-the-art MOS models, show a significant deviation from the measurement results. It is shown that the third order distortion prediction of the generally used 'θ-model' for mobility reduction is rather poor in the triode region.

1. INTRODUCTION

MOS transconductors are widely used, for example in gm-C filters. Since these circuits are usually encountered on mixed-A/D integrated circuits, large and balanced input signals are required to reduce the influence of digitally induced substrate noise. To keep the distortion due to the large input signals within acceptable limits, linearisation techniques are needed. The synthesis of linear MOS transconductors is usually based on a first order strong inversion model:

Triode region ($V_{ds} < V_{gs} - V_t$):

$$I_d = K_0 \cdot V_{ds} \cdot \left(V_{gs} - V_t - \frac{1}{2} V_{ds}\right) \qquad (1a)$$

with: $K_0 = \mu \cdot C_{ox} \cdot \frac{W}{L}$

Saturation region ($V_{ds} \geq V_{gs} - V_t$):

$$I_d = \frac{K_0}{2} \cdot \left(V_{gs} - V_t\right)^2 \qquad (1b)$$

If Vds is constant in the triode region, Id is linear with Vgs [1]. In the saturation region the sum or the difference of Vgs of two transistors must be constant for a linear V to I conversion [2,3]. According to this model the synthesised circuits have a perfectly linear transfer function. However due to second order effects the linearity of such circuits is limited. In a balanced circuit the even order distortion will cancel out, however odd order distortion will not cancel out. Especially the mobility reduction effect introduces significant third order distortion. The mobility reduction effect can be modelled by the 'θ-model' which is obtained by replacing K_0 by K_{eff} in eq. 1, where:

$$K_{eff} = \frac{K_0}{1 + \theta \cdot \left(V_{gs} - V_t\right)} \qquad (2)$$

although quite simple, eq. 2 is used in state-of-the-art MOS models. The achieved linearity with known transconductor structures realised in a sub-micron process ($\theta \approx 0.4$) is much lower than in an older process with a larger oxide thickness ($\theta \approx 0.05$). The linearisation technique presented in this paper aims to reduce the third order distortion of a triode MOS transconductor. To reach this aim, the non-linearity due to the mobility reduction effect is taken into

0-7803-3073-0/96/$5.00

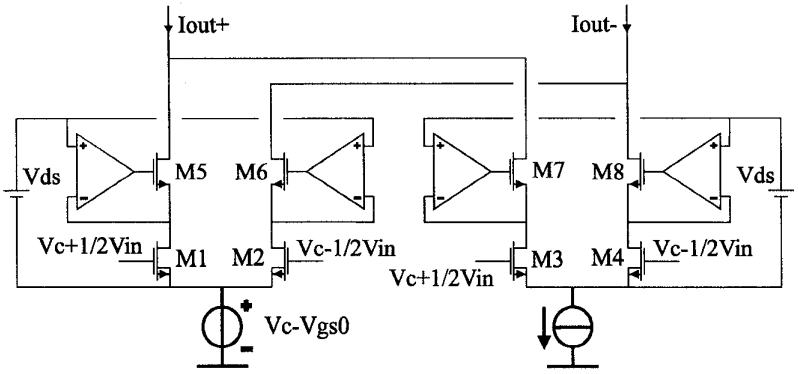

Fig. 1: Concept: The VSC (left) in parallel with the CSC (right).

account in the synthesis phase (similar as in [4]). The implementation in this paper involves parallel operation of a voltage biased and a current biased triode MOS differential pair but the linearisation technique is more widely applicable, for example for bipolar junction transistors.

2. THE LINEARISATION TECHNIQUE

Fig. 1 shows the conceptual topology of the linearised transconductor. The left-hand side of this figure presents a triode MOS differential pair biased by a tail voltage source, to be called Voltage Source Configuration (VSC). The value of the tail voltage source is determined by the common mode component of the input voltage. The biasing by a tail current source is depicted on the right-hand side, the Current Source Configuration (CSC). When all four conversion transistors M1 through M4 are identical and are biased at the same operating point, the same Taylor-series is valid for all of them:

$$I_d = a_0 + a_1 \cdot v + a_2 \cdot v^2 + a_3 \cdot v^3 \qquad (3)$$

where v is the small signal gate-source voltage and Id the output current of one transistor. The Taylor coefficients can be calculated from the 'θ-model' and are dependent on the IC process and bias point. Relying on the Taylor-series of eq. 3, the differential output current of the VSC and CSC are respectively:

$$i_{out\_diff\_VSC} = a_1 \cdot v_{in} + \frac{1}{4} \cdot a_3 \cdot v_{in}^3 \qquad (4a)$$

and

$$i_{out\_diff\_CSC} = a_1 \cdot v_{in} + \left(\frac{1}{4} \cdot a_3 - \frac{1}{2 \cdot a_1} a_2^2 \right) \cdot v_{in}^3 \qquad (4b)$$

By putting these two configurations in parallel, the first order terms $a_1 \cdot v_{in}$ will add up and the third order terms will cancel out if*:

$$a_2^2 = a_1 \cdot a_3 \qquad (5)$$

Using the 'θ-model' for the triode MOS transistor and substituting: $Vgs = Vgs_0 + v$, one can calculate the Taylor-series expansion of the drain current with respect to v. Evaluating eq. 5 results in:

$$a_2^2 = \left(-K_0 \cdot V_{ds}\right)^2 \cdot \frac{\left(1 + \frac{1}{2} \cdot \theta \cdot V_{ds}\right)^2 \cdot \theta^2}{\left(1 + \theta \cdot \left(V_{gs_0} - V_t\right)\right)^6} \qquad (6a)$$

and

$$a_1 \cdot a_3 = \left(K_0 \cdot V_{ds}\right)^2 \cdot \frac{\left(1 + \frac{1}{2} \cdot \theta \cdot V_{ds}\right)^2 \cdot \theta^2}{\left(1 + \theta \cdot \left(V_{gs_0} - V_t\right)\right)^6} \qquad (6b)$$

These two expressions are identical, which means that the linearisation condition is simply met by adding the currents of a VSC and a CSC (ratio 1:1). This condition is independent of DC biasing. Moreover, if the transistors are matched the linearisation technique does not depend on the temperature and process variations. This suggest a robust linearisation technique, provided that 'θ-model' in the triode region is valid.

* Note that by scaling the VSC and CSC a sufficient condition is that a_2^2 is proportional to $a_1 \cdot a_3$. This can be used for a BJT implementation with the VSC and CSC in the ratio 2:1.

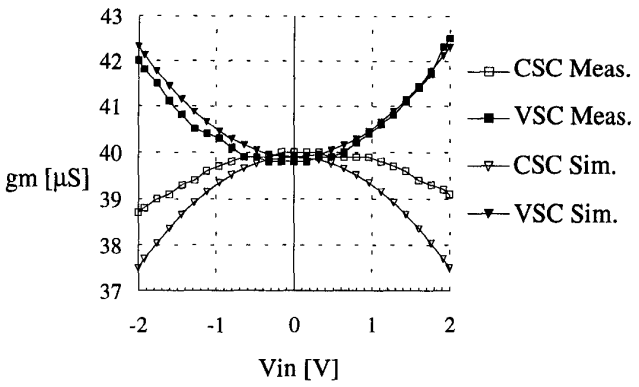

Fig 2: Measured and simulated transconductance.

3. SIMULATION AND MEASUREMENT RESULTS

In order to verify the linearisation concept described above, an experimental chip was designed and fabricated in a 0.8μm nwell process. The VSC and the CSC are implemented with PMOSTs. The transconductance for both configurations is measured. It appears that the tranconductance of the VSC is concave and the transconductance of the CSC is convex, as expected from eq. 4. This holds for the entire tuning range from 10μS up to 70μS. In fig. 2 the simulation results, using the Philips level 9 MOS model [5], and the measurement results are given for the VSC and CSC for Vds is 0.4V. The Vgs_0 of the conversion MOSTs M1 through M4 is 3.5V, the threshold voltage Vt is 1V, the transconductance factor K_0 is equal to $100\mu A/V^2$ and θ is about 0.3 V^{-1}. A closer look at the transconductance curves shows that the measured and simulated transconductance curves for the VSC are almost equal. However, the measured curve for the CSC is much more linear than the simulated curve. As a result, the non-linearity cancellation by adding the output currents of the VSC and CSC is disturbed in measurements, in contrast to the simulation results. The measured third order harmonic distortion HD3 of the VSC is -43dB and the HD3 of the CSC is -48dB for an input voltage of $4V_{ppdiff}$ at a frequency of 1kHz. The measured HD3 of the total transconductor is -56dB this is an improvement of 8dB compared to the CSC only. However, simulations predict an improvement of about 30dB. The asymmetry of the transconductance curve results in second order distortion which is about -65dB for a Vds of 0.4V.

To be sure whether the deviation of the measured CSC is a fundamental problem or dependent on the implementation*, external high quality sources are applied instead of the on-chip sources. The third order harmonic distortion in the triode region is measured and simulated [5]. The results are shown in fig. 3. Comparing the measurements and simulations results the following observations can be made:

1) The measured distortion of the VSC has a sharp minimum at a certain Vds value. This is the point where the third order non-linearity changes sign [6]. Below this transition point the non-linear terms of the VSC and the CSC have opposite signs, so that a cancellation can occur. This means that the proposed linearisation technique can only be used for Vds lower than about 1V (Vgs=3.5V). This is in accordance with the simulation results of the Philips level 9 model. However, often used models like Spice level 3 and BSIM models predict this transition point at a much higher Vds, close to $Vds_{sat.}$ [6].

2) Even if the distortion terms of the VSC and the CSC have opposite signs in the triode region, their magnitude is not equal. However, the considered circuit simulators using Spice level 3, BSIM or the Philips level 9 MOS model, predict distortion of the

* Note that a finite output resistance of a current source also leads to a more linear transfer function. In fact an optimal impedance can be found.

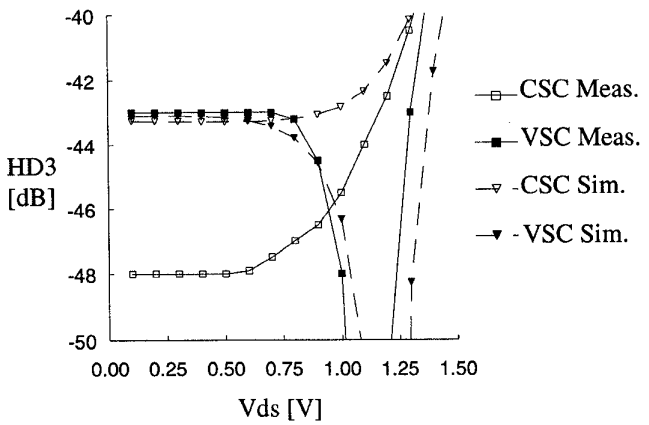

Fig 3: Measured and Simulated HD3 versus Vds.

same magnitude, because deep in the triode region they all rely on the 'θ-model'. Therefore simulations predict a perfect distortion cancellation. In practice the linearity improvement is moderate. The incorrect modelling of the 'θ-model' is recently also reported in [7].

3) A current biased triode differential pair has a more linear transfer function than a voltage biased differential pair. Nevertheless, triode differential pairs are often biased with grounded sources [1].

4. CONCLUSIONS

A linearisation technique is presented aiming at cancelling third order non-linearity's due to mobility reduction in CMOS triode transconductors. This should be achieved by parallel operating differential pairs, one biased by a tail voltage source and one biased by a tail current source. Measurements show that the third order distortion is reduced by 8dB. In simulations significantly more non-linearity reduction is found. This is due to the poor third order distortion prediction in the triode region of the widely used 'θ-model' for mobility reduction. Moreover, it also appears that current biasing of a triode MOS differential pair results in a more linear transfer function than voltage biasing.

ACKNOWLEDGEMENT

This work is supported by Philips Research Laboratories Eindhoven. The authors would like to thank E. van der Zwan for his fruitful discussions.

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