Jitter Requirements of the Sampling Clock in Software Radio Receivers

Vincent J. Arkesteijn, *Student Member, IEEE*, Eric A. M. Klumperink, *Member, IEEE*, and Bram Nauta, *Senior Member, IEEE*

***Abstract*—The effective number of bits of an analog-to-digital converter (ADC) is not only limited by the quantization step inaccuracy but also by sampling time uncertainty. According to a commonly used model, the error caused by timing jitter, integrated over the whole bandwidth, should not be bigger than the quantization noise, for a full swing input signals at the maximum input frequency. This results in unfeasible phase noise requirements for the sampling clock in software radio receivers with direct RF sampling. However, for a radio receiver not the total integrated error is relevant, but only the error signal in the channel bandwidth. This paper explores the clock jitter requirements for a software radio application, using a more realistic model and taking into account the power spectrum of both the input signal and the spectrum of the sampling clock jitter. Using this model, we show that the clock jitter requirements are very similar to reciprocal mixing requirements of superheterodyne receivers.**

***Index Terms*—Analog-to-digital converter (ADC), jitter, mixer, sampling, software radio.**

I. Introduction

UNLIKE conventional single-standard radio receivers, a software radio is designed to receive signals from multiple standards. This flexibility is achieved by performing most of the signal processing in software. Because software runs on digital hardware and radio waves are analog by nature, an analog-to-digital converter (ADC) has to be included. An example of a software radio front-end is shown in Fig. 1.

Various radio standards use different portions of the radio spectrum. Enabling reception of signals from various radio standards thus necessitates a large RF input bandwidth, and because of this, a high sampling rate.

In this large bandwidth, many signals will exist, some weak, some potentially very strong. The resolution of an ADC is determined by the difference in power levels between the strongest signal at the input and the quantization noise level. Because weak signals have to be converted in the presence of very strong ones, the required ADC resolution is very high.

ADCs combining this high bandwidth and high resolution are at present unfeasible and/or consume too much power. Nevertheless, ADCs will probably improve, and it is relevant to analyze their clock jitter requirements. Furthermore, direct RF sampling (without amplitude digitizing) is sometimes used [1], which may also be limited by sampling jitter. Therefore, we study jitter requirements of sampling clocks in this paper. Part of this work was also presented by the same authors in [2]. This works adds to that a derivation of jitter requirements (instead of only analysing the effects of jitter), a comparison with jitter in mixer-based receivers and some more examples.

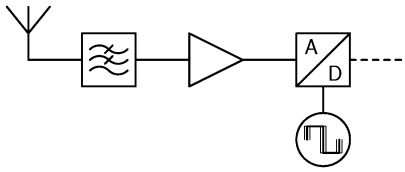

Fig. 1. Software radio receiver front-end.

As shown in Section II-A, according to a commonly used model for white ADC clock jitter [3], the resolution directly affects the clock jitter requirements, resulting in very stringent numbers. Better jitter models are available in the literature, e.g., [4]–[6]. Here, the jitter spectrum is still considered white, resulting in a white error spectrum at the output of the ADC. In [7], spectra of input signal and jitter are taken into account, but only the error signal over the full Nyquist bandwidth is considered. For a radio receiver however, only the error signal in the channel bandwidth is relevant. Therefore, [4]–[7] yield too pessimistic jitter requirements.

Section II-B shows a model comparable to that in [4]–[7]. We show that using this model, taking into account the spectra of both the input signals and the sampling clock jitter, and looking at the jitter-induced error signal only in the frequency band of interest, sampling clock jitter requirements can be relaxed. These results are compared with local oscillator (LO) jitter requirements for mixer-based receivers in Section III, showing that jitter requirements in software radio receivers are quite comparable to those for LOs in super-heterodyne receivers. Finally, Section IV presents some conclusions.

II. Jitter Effects on Sampling

In this section, effects of jitter in the sampling clock will be analyzed. First, a commonly used model will be presented. This is followed by a more precise model.

A. ADC—White-Noise Model

Consider an incoming signal $s(t)$. Ideally, the sampled version of this signal with sample rate $1/\tau$ $s_{\tau,\mathrm{ideal}}(k)$ is constructed as follows:

$$s_{\tau,\mathrm{ideal}}(k) = s(k\tau). \tag{1}$$

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The authors are with the IC-Design Group, CTIT, University of Twente, Twente NL 7500, The Netherlands (e-mail: v.j.arkesteijn@alumnus.utwente.nl).

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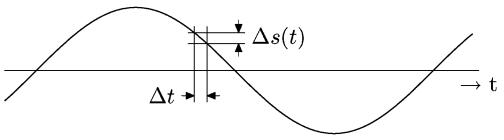

Fig. 2. Input signal as a function of time and the effect of sampling jitter.

Due to sampling jitter however, an error will be introduced, as can be seen in Fig. 2. The sampled signal can now be calculated as follows (for small absolute jitter Δt):

$$\begin{aligned} s_\tau(k) &= s\left(k\tau + \Delta t(k\tau)\right) \\ &\approx s(k\tau) + \Delta t(k\tau) \cdot \frac{\partial}{\partial t} s(t)\bigg|_{k\tau}. \end{aligned} \tag{2}$$

This signal consists of a sampled version of the input signal $s(t)$ plus an error signal. When requiring the root mean square (rms) error of $s_\tau(k)$ to be lower than the rms error due to quantization, and assuming a full swing harmonic input signal at the maximum input frequency $f_{\max}$, the following relation between required rms jitter (the rms value of the absolute jitter $\Delta t(k\tau)$) and resolution can be derived [8]

$$\Delta t_{\text{rms}} = \frac{1}{2\pi f_{\max} 2^n} \sqrt{\frac{2}{3} M}. \tag{3}$$

Here, n is the ADC resolution and M is the oversampling ratio.

For software radio applications, this equation yields jitter requirements that are not achievable with currently available integrated clock sources, as shown in Section II-C.

B. ADC—More Detailed Model

The preceding analysis only derives the rms value of the jitter induced error. This is often sufficient, especially when the signals of interest are wideband. In the case of a software radio receiver however, only a narrow portion of the converted bandwidth is of interest, and the spectral distribution of the error signal becomes relevant.

To derive the spectrum of the error signal, consider the following. As seen in (2), the error signal $\Delta s_\tau(k)$ is the time derivative of the input signal $(\partial/\partial t)s(t)$ multiplied with the sampling time error $\Delta t(k\tau)$

$$\begin{aligned} \Delta s_\tau(k) &= s\left(k\tau + \Delta t(k\tau)\right) - s(k\tau) \\ &\approx \Delta t(k\tau) \cdot \frac{\partial}{\partial t} s(t)\bigg|_{k\tau}. \end{aligned} \tag{4}$$

Taking the discrete-time Fourier transform (DTFT)

$$\mathcal{F}\left(\Delta s_\tau(k)\right) \approx \mathcal{F}\left(\Delta t(k\tau)\right) \star \mathcal{F}\left(\frac{\partial}{\partial t} s(t)\bigg|_{k\tau}\right) \tag{5}$$

where $\mathcal{F}$ denotes the DTFT and $\star$ denotes convolution. This result is also obtained in [4] and [9]. Apparently, for calculating the spectrum of the error signal, both the input signal and the spectrum of the jitter have to be known.

The input spectrum of a radio receiver is not known in general, but wireless standards normally limit the power level of interfering signals that have to be tolerated. Fig. 3 for example shows Hiperlan/2 blocking levels [10]. These form an upper limit to the input signal $s(t)$. From this power spectrum, an upper limit to $(\partial/\partial t)s(t)$ can be calculated by multiplying the corresponding amplitudes by $j\omega$. Note that interfering signals that are close in frequency to the wanted signal have far lower maximum power levels than those further away. We will see later that this greatly relaxes phase noise requirements.

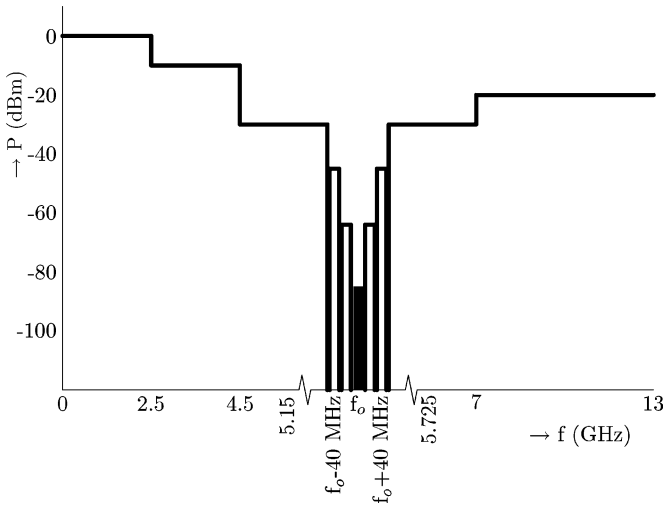

Fig. 3. In-band and out-of-band blocking levels for HiPerLAN/2 [10], together with the level of the wanted signal (solid bar at f_0) during blocking tests. Note: frequency axis is not entirely to scale.

Furthermore, the spectrum of $\Delta t(t)$ has to be known. When the sampling clock is derived from a synthesizer containing a voltage-controlled oscillator (VCO) (e.g., an *LC* or ring oscillator), $\Delta t(t)$ can be assumed to have a f^{-2} power spectrum outside the synthesizer loop bandwidth [11]. Also, because variance of the absolute jitter at the output of a first or second-order phase-locked loop (PLL) is constant when the observation time exceeds the loop time constant [12], the jitter process is assumed to be stationary.

The effect of applying (5) to the input and jitter spectra described above can best be illustrated with the example of an interfering harmonic input signal $s(t) = A_i \sin(\omega_i t)$

$$\begin{aligned} \mathcal{F}\left(\Delta s_\tau(k)\right) &\approx \mathcal{F}\left(\Delta t(k\tau)\right) \star \mathcal{F}\left(\frac{\partial}{\partial t} A_i \sin(\omega_i t)\bigg|_{k\tau}\right) \\ &= \mathcal{F}\left(\Delta t(k\tau)\right) \star \omega_i A_i \cdot \mathcal{F}\left(\cos(\omega_i k\tau)\right). \end{aligned} \tag{6}$$

Due to its f^{-2} nature, most energy in $\Delta t(k\tau)$ is at low frequencies. In the frequency domain this is convolved with the derivative of the input signal, which leads to the following.

1) The convolution operation in (5) shifts the jitter spectrum $\mathcal{F}(\Delta t(k\tau))$ to the frequencies of input signals. Therefore, the jitter-induced error in the output is concentrated around these frequencies.
2) Input signals with higher power are surrounded by more jitter-induced error in the output than those with lower power, due to the linearity of the convolution operation.
3) Input signals of higher frequencies are surrounded by more jitter-induced error in the output than signals at lower frequencies, because of the frequency dependence of $(\delta/\delta t)s(t)$. This is in accordance with the results in [6].

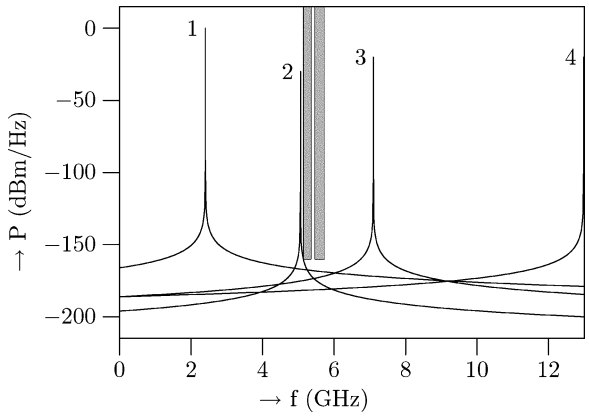

Fig. 4. ADC output signal (input referred) for four demanding interfering input signals (0 dBm @2.5 GHz, −30 dBm @5.15 GHz, −20 dBm @7 GHz and −20 dBm @13 GHz). Acceptable reception requires the in-band jitter-induced output noise to be below the shaded area. This area is delimited by the band limits (5150–5350 and 5470–5725 MHz) and the maximum acceptable in-band noise level for both Hiperlan/2 bands.

Because the error signal is concentrated around frequencies with strong input signals, it is less of a problem in the frequency band of interest, assuming that the frequency difference between the wanted signal and the strong interferers is larger than the synthesizer loop bandwidth, which is usually the case.

C. Comparison

To illustrate the significance of the difference between the two ADC models, a numeric example will be given. A software radio receiver capable of receiving different WLAN standards (including Hiperlan/2) has been chosen for this.

The RF filter at the input (see Fig. 1) will pass signals upto around 6 GHz, since most WLAN standards are in either the 2.4 or 5.5-GHz bands. We will assess the required sampling clock jitter first as estimated using the white-noise model, and then as estimated using the second model.

In order to meet Hiperlan/2 requirements, the required resolution can be calculated as follows. The largest signal level at the input at which the desired signal still has to be demodulated is 0 dBm according to the Hiperlan/2 standard [10] (see Fig. 3). The noise level that is still acceptable to the demodulator is 10 dB above thermal noise, so −164 dBm/Hz or −66 dBm in a 6-GHz bandwidth. Therefore, SNR at the ADC output has to be 66 dB. If we allow all receiver noise to be caused by quantization, this requires 11 bits resolution.

Using these numbers in (3) results in

$$\Delta t_{\rm rms} = \frac{1}{2\pi \cdot 6G \cdot 2^{11}} \sqrt{\frac{2}{3}} \approx 11 \ \text{fs}.$$

This is one or two orders of magnitude smaller than what is achieved by currently published integrated synthesizers.

If we use the more realistic ADC model however, results are different. Fig. 4 shows the output spectrum of an ADC with four different interfering input signals. The levels of these signals were taken to be the blocking levels (see Fig. 3), at the frequencies where their impact is most severe (2.4, 5.06, 7.1, and 12.98 GHz). None of these interferers cause the jitter-induced output error to exceed the maximum in-band noise level (indicated by the shaded area).

To improve readability of this figure, in-band interferers have been left out. Further analysis showed that the jitter-induced error due to in-band interferers is just below the maximum in-band noise level.

The rms jitter of the 12-GHz sampling clock used for Fig. 4 was 1.3 ps, with a flat power spectrum up to 100 kHz from the carrier and a f^{-2} roll-off above that. This corresponds to −96 dBc/Hz phase noise at 1-MHz offset. These values have been chosen to just comply with in-band noise requirements.

It is clear from Fig. 4 that the strongest signal (0 dBm at 2.4 GHz), which was the limiting factor in the first model, is not a key factor in the second model. This shows that the more realistic model yields far more feasible requirements than the first model (1.3 ps absolute rms jitter instead of 11 fs).

D. Requirements

Until here, the effects of jitter on sampling were analyzed. In this section, the converse of this analysis will be discussed. Given the input blockers and a maximum allowed in-band noise level, an upper limit to the jitter spectrum will be derived.

The convolution operation in (6) shifts the jitter spectrum $\mathcal{F}(\Delta t(k\tau))$ by the frequency of the interferer. Evaluating the jitter-induced output error at the frequency of the wanted signal ω_w therefore yields

$$\mathcal{F}\left(\Delta s_\tau(k)\right)|_{\omega_w} \approx \omega_i A_i \cdot \mathcal{F}\left(\Delta t(k\tau)\right)|_{|\omega_w - \omega_i|}. \tag{7}$$

Since both an interferer at $\omega_i - \omega_w$ above the wanted signal and an interferer at $\omega_w - \omega_i$ below the wanted signal can be shifted to the frequency of the wanted signal, the absolute value of this frequency difference is taken. Also, because $\Delta t(k\tau)$ is real, $\mathcal{F}(\Delta t(k\tau))|_{\omega_m}$ is a symmetrical function.

If we take the power-spectral density (PSD) $S_{\Delta s_\tau}(\omega_w)$ of the error signal

$$\begin{aligned} S_{\Delta s_\tau}(\omega_w) &\approx \omega_i^2 P_i \cdot S_{\Delta t}\left(|\omega_w - \omega_i|\right) \\ &= \omega_i^2 P_i \cdot \frac{1}{\omega_{\rm CLK}^2} S_\Phi\left(|\omega_w - \omega_i|\right). \end{aligned} \tag{8}$$

This error signal should be lower than the maximum allowed in-band noise density$N_{\max}$. With $P_{i,\max}(\omega_i)$ the maximum input power at a certain frequency (the blocker profile)

$$\omega_i^2 P_{i,\max}(\omega_i) \cdot \frac{S_\Phi\left(|\omega_w - \omega_i|\right)}{\omega_{\rm CLK}^2} < N_{\max} \tag{9}$$

$$S_\Phi\left(|\omega_w - \omega_i|\right) < \frac{N_{\max}\omega_{\rm CLK}^2}{\omega_i^2 P_{i,\max}(\omega_i)}. \tag{10}$$

This can be rewritten as the following set of upper bounds on the phase noise spectrum, with $\omega_m = |\omega_w - \omega_i|$ the modulation frequency of the jitter component:

$$\begin{cases} S_\Phi(\omega_m) < \frac{N_{\max}\omega_{\rm CLK}^2}{(\omega_w - \omega_m)^2 P_{i,\max}(\omega_w - \omega_m)} \\ S_\Phi(\omega_m) < \frac{N_{\max}\omega_{\rm CLK}^2}{(\omega_w + \omega_m)^2 P_{i,\max}(\omega_w + \omega_m)}. \end{cases} \tag{11}$$

There are two bounds. These correspond to the two sides of the wanted signal where an intererer might be found.

This upper bound has been calculated for the same receiver as used in the previous section. The result can be seen in Fig. 5,

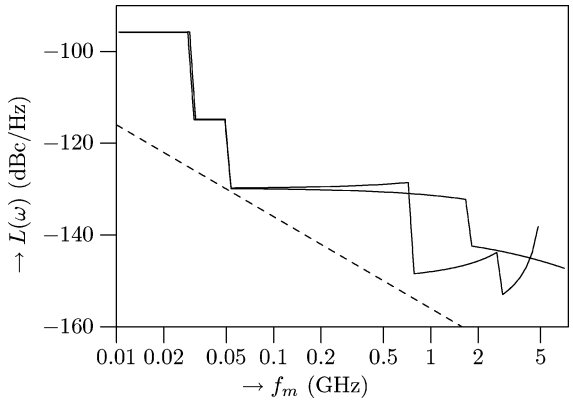

Fig. 5. Upper bound on the phase noise spectrum for the 12-GHz sampling clock of a software radio receiver capable of receiving Hiperlan/2, calculated using (11). The dashed line represents $1/f^2$ phase noise of -96 dBc/Hz at 1-MHz offset, just complying with the requirements.

where $\mathcal{L}(\omega_m) = (1/2)S_\Phi(\omega_m)$. Because both the inequalities of (11) should be satisfied, $\mathcal{L}(\omega_m)$ should be below both lines. The steps in the curve correspond to the steps in the blocker profile of Fig. 3. The deviation from horizontal lines is due to the $(\omega_w \pm \omega_m)$ factor in (11).

One phase noise spectrum that conforms to these requirements, is a $1/f^2$ spectrum with -96 dBc/Hz at 1-MHz offset. This is indicated by the dashed line in Fig. 5.

III. Jitter Effects on Mixing

Sampling and mixing are very similar operations. The first can be modeled by multiplying with a pulse train; the second can be modeled by multiplying with a sine (or square) wave.

This could lead to the idea that the effects of clock jitter in a sampler-based and a mixer-based receiver are equal. To see whether this is true, first the effect of jitter in mixer-based receivers is analyzed. Then, these results are compared to those obtained in the previous section for a sampler-based receiver. Finally, a numeric example is given.

A. Analysis

Assume an input signal $s(t)$, which is multiplied with a LO at frequency $\omega_{\rm LO}$

$$\begin{aligned} u(t) &= s(t)\cdot\sin\left(\omega_{\rm LO}\left(t+\Delta t(t)\right)\right) \\ &= s(t)\cdot[\sin(\omega_{\rm LO}t)\cdot\cos\left(\omega_{\rm LO}\Delta t(t)\right) \\ &\qquad + \cos(\omega_{\rm LO}t)\cdot\sin\left(\omega_{\rm LO}\Delta t(t)\right)] \\ &\approx s(t)\cdot\sin(\omega_{\rm LO}t) + s(t)\cdot\cos(\omega_{\rm LO}t)\cdot\omega_{\rm LO}\Delta t(t). \end{aligned} \quad (12)$$

The first term in this equation is the wanted mixing product, the second term is the unwanted product due to LO phase noise. Taking the Fourier transform of the error signal $\Delta u(t) = u(t) - s(t)\cdot\sin(\omega_{\rm LO}t)$

$$\mathcal{F}\left(\Delta u(t)\right) = \mathcal{F}\left(s(t)\right)\star\mathcal{F}\left(\cos(\omega_{\rm LO}t)\right)\star\omega_{\rm LO}\mathcal{F}\left(\Delta t(t)\right). \quad (13)$$

With a harmonic input signal $s(t) = A_{\rm in}\sin(\omega_{\rm in}t)$, the result is as follows:

$$\begin{aligned} \mathcal{F}\left(\Delta u(t)\right) = \mathcal{F}\left(\Delta t(t)\right) &\star \omega_{\rm LO}A_{\rm in}\cdot\mathcal{F}\left(\sin(\omega_{\rm in}t)\right) \\ &\star\mathcal{F}\left(\cos(\omega_{\rm LO}t)\right). \end{aligned} \quad (14)$$

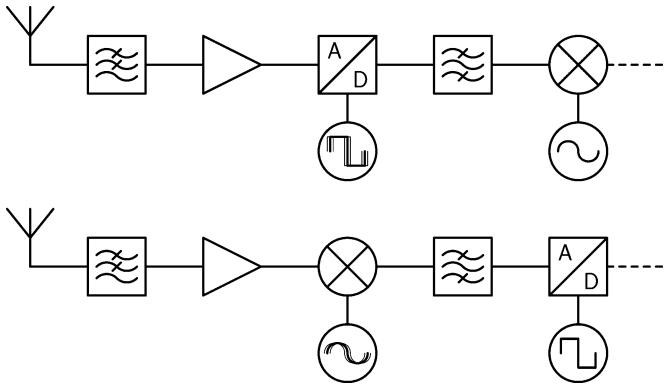

Fig. 6. Two receiver structures, used for comparing mixer-based and sampler-based receivers.

B. Sampling and Mixing Compared

A superficial comparison of (6) and (14) indicates a similarity between the effects of jitter on sampling and mixing. However, as the functional behavior of samplers and mixers is different, a direct comparison is impossible. To compare their jitter effects, we need two circuits with identical functionality.

This can be done using the two circuits in Fig. 6. Both of them output a time-discrete signal at a lower frequency than the input signal. The difference is that in the upper circuit, the downconversion is performed digitally, while in the lower circuit this is done using an analog mixer. As discrete-time signal processing is insensitive to jitter, the extra circuit blocks in the upper circuit will have no effect on jitter. Furthermore, because of the lower frequencies involved, we will ignore the sampling jitter effects in the ADC of the lower circuit.

Using derivations analogous to the ones above, the following expressions for the spectra of the jitter-induced error in the output signals of the two circuits can be derived.

Sampler-based receiver

$$\mathcal{F}\left(\Delta s_\tau(k)\right) \approx \mathcal{F}\left(\frac{\partial}{\partial t}s(t)\bigg|_{k\tau}\right)\star\mathcal{F}\left(\sin(\omega_{\rm LO}k\tau)\right)\star\mathcal{F}\left(\Delta t(k\tau)\right). \quad (15)$$

For a harmonic input signal $A_{\rm in}\sin(\omega_{\rm in})$, this becomes

$$\begin{aligned} \mathcal{F}\left(\Delta s_\tau(k)\right) \approx \omega_{\rm in}A_{\rm in}\cdot\mathcal{F}\left(\cos(\omega_{\rm in}k\tau)\right) \\ \star\mathcal{F}\left(\sin(\omega_{\rm LO}k\tau)\right)\star\mathcal{F}\left(\Delta t(k\tau)\right). \end{aligned} \quad (16)$$

Mixer-based receiver

$$\mathcal{F}\left(\Delta u_\tau(k)\right) \approx \mathcal{F}\left(s(k\tau)\right)\star\mathcal{F}\left(\cos(\omega_{\rm LO}k\tau)\right)\star\omega_{\rm LO}\mathcal{F}\left(\Delta t(k\tau)\right). \quad (17)$$

For a harmonic input signal $A_{\rm in}\sin(\omega_{\rm in})$, this becomes

$$\begin{aligned} \mathcal{F}\left(\Delta u_\tau(k)\right) \approx A_{\rm in}\cdot\mathcal{F}\left(\sin(\omega_{\rm in}k\tau)\right)\star\mathcal{F}\left(\cos(\omega_{\rm LO}k\tau)\right) \\ \star\omega_{\rm LO}\mathcal{F}\left(\Delta t(k\tau)\right). \end{aligned} \quad (18)$$

Comparing (16) and (18) shows that there is one important difference in the jitter-induced output error. For a mixer, this error is not proportional to the frequency of the input signal, but to the frequency of the LO signal.

This comparison is summarized in Table I, together with the first ADC model that was discussed. This shows the difference between the two ADC models, and also shows that the difference between the second ADC model and the mixer is a factor $\omega_{\rm LO}/\omega_{\rm in}$.

TABLE I
POWER AND SPECTRAL SHAPE OF JITTER INDUCED OUTPUT NOISE

	output noise proportional to		spectral shape
ADC I (sec. II-A)	$A_{in,max}$	$\omega_{in,max}$	white
ADC II (sec. II-B)	A_{in}	ω_{in}	same as clock, around input freqs
mixer (sec. III)	A_{in}	ω_{LO}	same as clock, around input freqs

Note that $\omega_{\rm LO}$ in a zero- or low-IF receiver is close to $\omega_{\rm in}$ of the wanted signal, and usually of the same order of magnitude as frequencies of unwanted signals. This leads to comparable in-band jitter-induced noise levels for both types of receivers.

Also note that in this comparison $\Delta t(t) = \Delta\phi(t)/\omega_{\rm LO}$ is assumed to be independent of $\omega_{\rm LO}$ (and thus, $\Delta\phi(t)$ changes with frequency). This is valid with respect to frequency division and multiplication, and also typically holds for oscillators with constant tank Q and power consumption.

C. Example

As an example of the similarity between mixer-based and sampler-based receivers, some simulations of an ADC used for Bluetooth reception have been done using Simulink.

Reciprocal mixing effects in a mixer-based receiver set an upper limit on the LO phase noise of -120 dBc/Hz at 3-MHz offset, with a -20-dB/decade (f^{-2}). Together with the specified interferer level at this offset of $+40$ dBc above the -67 dBm wanted signal, this yields in-band noise that is equal in power to the maximum in-band noise (-147 dBm/Hz). A synthesizer loop bandwidth of 100 kHz was assumed, so jitter was assumed flat below this offset frequency.

A sampler was modeled, with a sampling frequency of 2400 Ms/s. Its phase noise spectrum was the same as that for a mixer-based receiver as described above. This corresponds to an absolute rms jitter of 1.3 ps. The wanted signal was a sinewave at 2405 MHz with a level of -67 dBm. This is the sensitivity specified in the Bluetooth standard for these tests.

The effect of aliasing is not taken into account here. Normally, a software radio receiver would use a higher sampling rate than used here, so that aliasing is not an issue. The only reason for taking a lower sampling rate in this example, is for better comparison with the mixer-based receiver.

Fig. 7 shows the output spectrum of the sampler, with interfering signals. In the worst-case situation (black line), the $+40$ dBc interferer at an offset of 3 MHz) the in-band noise is exactly at its maximum allowed level. This is in line with the results for a mixer-based receiver. This illustrates that jitter-induced output noise is comparable for sampler and mixer based receivers, as noted above.

IV. CONCLUSION

When judging the effect of clock jitter on the output of samplers over the entire frequency range, knowledge of only the rms value of the time jitter, combined with knowledge of amplitude and maximum frequency of the input signal is sufficient. When one is only interested in a narrow portion of the bandwidth of the sampled signal, as in a software radio receiver, the same approach yields overly stringent requirements on the clock jitter.

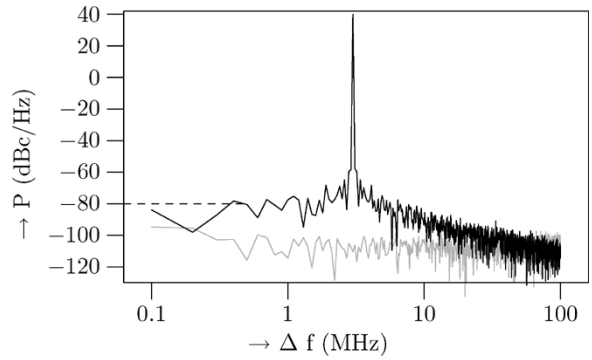

Fig. 7. Output of the sampler in two simulations. Gray: with $+57$ dBc interferer at 405-MHz offset (-10 dBm at 2000 MHz, which is the strongest possible interferer). Black: with $+40$ dBc interferer at 3-MHz offset (worst-case in-band interferer). The dashed line represents the maximum acceptable in-band noise level for Bluetooth.

Combining knowledge of the jitter spectrum with knowledge of the spectrum of the input signal, can lead to more accurate and far more relaxed estimates for clock jitter requirements, in the example shown by more than two orders of magnitude. Actually, jitter requirements for the clock of a sampler-based receiver are quite close to the requirements for the LO in a mixing receiver.

Although at present many issues stand in the way of practical software radios, we conclude that ADC clock jitter is not the severe problem it is often thought to be.

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