Wideband CMOS Receivers exploiting Simultaneous Output Balancing and Noise/Distortion Canceling

S.C. Blaakmeer[1], E.A.M. Klumperink[1], D.M.W. Leenaerts[2], B. Nauta[1]

[1] *University of Twente, CTIT Institute, IC Design group, P.O. Box 217, 7500 AE Enschede, The Netherland*
s.c.blaakmeer@utwente.nl, e.a.m.klumperink@utwente.nl, b.nauta@utwente.nl

[2] *NXP Semiconductors, Research, Eindhoven, The Netherlands*

***Abstract*— This paper deals with the problem of realizing wideband receiver front-ends in downscaled CMOS technologies, which are highly wanted for multi-standard radio receivers and cognitive radio applications. Instead of using many narrowband inductor based receivers, we prefer the use of one wideband receiver with sufficient bandwidth to cover all popular frequency bands up to 6GHz or even 10GHz. To relax RF filter requirements, high linearity is required, while high gain and low noise are important for good sensitivity. Downscaled CMOS technologies feature high speed transistors, but also decreasing supply voltages and increasing transistor non-idealities, which makes it increasingly difficult to achieve high gain and good linearity. It will be shown that a combination of a common-gate (CG) stage and an admittance-scaled common-source (CS) stage has attractive properties for implementing a wideband receiver with active balun, while simultaneously canceling the noise and distortion of the CG-stage. Example applications in a wideband Balun-LNA and combined Balun-LNA-Mixer will be shown.**

I. Introduction

Wideband receivers are required for instance in upcoming Software-Defined Radio and Cognitive Radio architectures and for Ultra Wideband Communication in the 3-10GHz bands. There are many mobile wireless communication standards that use the frequency spectrum from a few hundred MHz up to 6 GHz and they are increasingly integrated in one device. Traditionally receivers with narrowband inductor based Low Noise Amplifiers (LNAs) are used, but this becomes more and more impractical if many radio interfaces are to be integrated. Moreover, on-chip inductors do not scale much with technology downscaling, so relatively to other components they become more expensive and therefore we prefer to avoid their use. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second order distortion and to reject power supply and substrate noise. To avoid the use of an external broadband balun and its accompanying losses which add directly to the noise figure, it is advantageous to integrate a balun on chip.

In this paper we will review recently proposed circuits to realize wideband linear front-ends with no or only few inductors in CMOS [1]-[14]. The main focus is on LNAs, but we will also briefly discuss wideband I/Q down-converters. In section II we will discuss the relevance of high linearity in such receivers. In section III we will present an overview of recently proposed wideband receiver front-ends. We will discuss why a Common Gate (CG)-stage is problematic as inductor-less wideband LNA. In section IV we show that combining a CG-stage with a Common Source (CS)-stage allows for achieving more gain. Furthermore, it can implement a wideband active balun in a very compact way, while simultaneously canceling the noise and distortion contribution of the CG-transistor. If the CS-stage is carefully optimized, both the linearity and noise of the resulting combined Balun-LNA can be good. Finally section V discusses a way of increasing the gain, while maintaining a high bandwidth, by avoiding making voltage gain at RF.

II. Linearity Requirements for Wideband Receivers

Like a narrowband zero-IF, a wideband receiver is sensitive to the 2nd order intermodulation product generated by an AM modulated carrier via AM detection. However, a wideband receiver may also suffer from 2nd order intermodulation generated by interferers that have a sum or difference frequency equal to the wanted RF-input signal. The response to a modulated carrier can be suppressed by AC-coupling between the LNA-output and mixer-input and by driving and designing the mixer in a well-balanced way [15]. However, the intermodulation product generated at a frequency equal to the frequency of the wanted signal cannot be separated from the signal. Especially standards that operate on large bandwidths, like DVB-H (470–862 MHz) [16] or WiMedia UWB (3.1–10.6 GHz) [17], have a high probability that a combination of interferers renders an in-band intermodulation product. A receiver designed for these standards should have an LNA with sufficiently high IIP2 (and IIP3) in order to handle strong interferers like WLAN (IEEE 802.11a/b/g) and the GSM standards. The required intercept points depend strongly on the assumed interferer scenario and the assumed amount of pre-filtering of the interfering signals. For a WiMedia UWB receiver the required IIP2 is above +20 dBm and IIP3 above -9 dBm as derived in [18]. For a DVB-H receiver, the required IIP2 is in order of +22dBm using a GSM/WLAN interferer scenario.

III. Wideband Receivers in Literature

Table I shows an overview of recently published wideband LNAs and down-converters in CMOS with no or only a few inductors, published at the most important solid-state circuit conferences. Different types of techniques have been proposed, which will be briefly discussed below. Distributed amplifiers

are not discussed as they heavily rely on inductors or transmission lines.

With the increasing f_T of MOS transistor, multi-GHz negative feedback amplifiers are becoming feasible and some interesting results have been achieved recently [3][7][8]. Still, several trade-offs exist between impedance matching, gain, noise and linearity. Until now, relatively modest IIP3 has been achieved which also varies strongly with frequency (typically in the range of -15dBm to -4dBm). IIP2 is often not reported, despite of its importance for wideband receivers. Furthermore, these circuits don't include balun functionality.

A Common Gate amplifier can achieve wideband impedance matching and gain with good linearity, but is it difficult to achieve a noise figure below 4dB. Moreover, at low supply voltage, there is not much voltage headroom to realize high voltage gain. Furthermore, a high load resistance, required for high gain, leads to bandwidth limitations. Therefore, CG-stages are often used in combination with inductive broad-banding to increase the bandwidth. However, we would like to avoid such inductors and investigated other ways to achieve a high gain. We will discuss now two techniques to increase the gain, while using standard transistors at 1.2V supply, and without the use of inductors. In section IV we explain how one can use a parallel CG- and CS-stage to realize a noise/distortion canceling LNA which also acts as balun, as proposed originally in [1] and later exploited and extended in [2][4][5][6][10][11][12][13]. In section V we will propose a technique to avoid making voltage gain at RF, but do this only after the down-conversion to IF.

IV. SIMULTANEOUS BALANCING AND NOISE/DISTORTION CANCELING

In the sections below we will briefly derive the conditions for simultaneous balancing, noise canceling and distortion canceling. We will neglect capacitive effects for simplicity. A more detailed discussion on high frequency limitations and robustness for component variations can be found in [1] [13].

A. Balancing (balun operation)

The Common Gate stage in Figure 1, biased with a current source, has a straightforward relation between its voltage gain ($A_{v,CG}$) and its input impedance ($R_{in,CG}$). The signal current (i_{Rcg}) flowing through the load resistor R_{CG} has to be equal to the signal current flowing at the input (i_{in}), as there is no alternative path to ground. Thus,

$$i_{in} = i_{Rcg} = \frac{v_{out,CG}}{R_{CG}} = \frac{v_{in} \cdot A_{v,CG}}{R_{CG}} \quad (1)$$

As a result, the input impedance of the CG-stage can be expressed as:

$$R_{in,CG} = \frac{v_{in}}{i_{in}} = \frac{R_{CG}}{A_{v,CG}} \quad (2)$$

For an ideal transistor, having infinite output resistance, this is obvious. In that case the input impedance can be written as $R_{in,CG} = 1/g_m$ and the gain equals $A_{v,CG} = g_m \cdot R_{CG}$. However, (1) and (2) are equally valid when the finite output resistance and the body-effect of a real transistor are taken into account.

TABLE I.

RECENT WIDEBAND LNAS AND DOWN-CONVERTERS IN CMOS WITH NO OR ONLY A FEW COILS

Ref	Bandwidth [GHz]	Gain A_V [dB]	NF [dB]	IIP2 [dBm]	IIP3 [dBm]	Pcore [mW]	Process V_{supply}	# coils area[mm²]	Functionality – Z-matching Technique
Bruccoleri et al JSSC 2004 [1]	0.2 – 2.0	10 – 14	< 2.4	+12	0	35	0.25µm 2.5V	0 0.075	LNA – Transimpedance +CS Noise Canceling
Cherazi et al CICC 2005 [2]	0.9 – 5	18 – 19	< 3.5	+4 (sim)	+1 (sim)	12	0.18µm 1.8V	4 ~0.4	Balun-LNA – CG+CS Noise Canceling
Zhan et al ISSCC 2006 [3]	0.5 – 8.2	22 – 25	< 2.6	?	-4 / -16	42	90nm 2.7V	0 0.025	LNA – Transimpedance Negative Feedback
Bagheri et al ISSCC06 [4] [6]	0.8 – 6	3–36 with IF-AMP	< 5.5	?	-3.5	29	90nm 2.5V	2 0.5	Balun-LNA+I/Q Mixer – CG+CS Stage
Blaakmeer et al RFIC 2006 [5]	2.7 – 4.5	18 – 19.6	< 5	?	-8	12.6	90nm 1.2V	1 0.2	LNA – CG+trafo+CS Noise Cancelling
Borremans et al ISSCC06 [7]	DC – 6	15 – 17.4	< 3.5	?	-15 / - 8	9.8	90nm 1.2V	0 0.002	LNA – Transimpedance with Active Feedback
Blaakmeer et al ESSC06 [12] [13]	0.2 – 5.2	13 – 15.6	< 3.5	+20	0	14	65nm 1.2V	0 0.009	Balun-LNA – CG+CS Noise Canceling
Ramzan et al ISSCC2007 [8]	1 – 7	15 – 17	< 3.5	?	-4.1	25	0.13µm 1.4V	0 0.019	LNA – Transimpedance with Active Feedback
Lee et al ISSCC07 [9]	2 – 8	23 with IF-AMP	< 4.5	+18	-7	31	90nm 2.5V	1 0.09	LNA+trafo-Balun+ I/Q Mixer – Negative FB.
Liao et al JSSC 2007 [10]	1.2 – 11.9	12.7 – 15.7	< 5	+10 / +20	-6.2	20	0.18µm 1.8V	5 0.59	LNA – CG Noise Canceling
Chen et al RFIC2007 [11]	0.8 – 2.1	14.5 – 17.5	< 2.6	?	0 / +16	17.4	0.13µm 1.5V	0 0.01	LNA – nMOS+pMOS CG Noise Canceling
Blaakmeer et al ISSCC08 [14]	0.5 – 7	18 no IF-AMP	< 5.5	+20	-3	16	65nm 1.2V	0 <0.01	Balun-LNA+I/Q Mixer – Noise Canceling

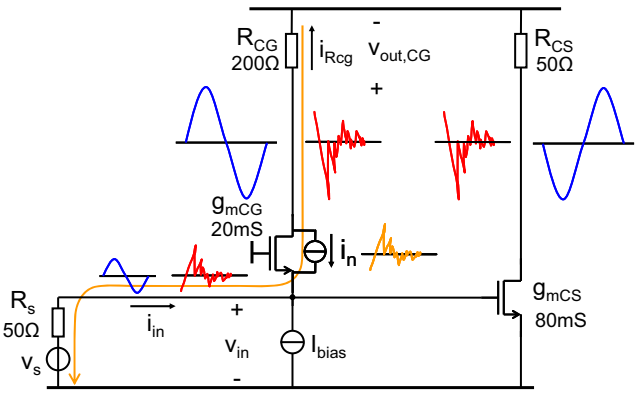

Fig. 1 The Balun-LNA, a combination of a Common Gate (CG) and admittance scaled Common Source (CS) stage to realize simultaneous output balancing, noise and distortion canceling

For an impedance match at the input, the input impedance of the CG-stage ($R_{in,CG}$) should equal the source resistance (R_S), thus the gain of the CG stage becomes:

$$A_{v,CG} = \frac{R_{CG}}{R_{in,CG}} = \frac{R_{CG}}{R_S} \tag{3}$$

To create a balun, the gain of the CS-stage in Figure 1 should be equal, but have opposite sign, thus:

$$A_{v,CS} = -A_{v,CG} = -\frac{R_{CG}}{R_S} \tag{4}$$

B. Noise Canceling

The noise generated by the CG-transistor in Figure 1 can be represented by a current source (i_n). This current generates both a voltage at the input-node ($v_{n,in} = \alpha_1 \cdot i_n \cdot R_S$) and a fully correlated anti-phase voltage at the CG-output ($v_{n,CG} = -\alpha_1 \cdot i_n \cdot R_{CG}$). The factor α_1 equals the voltage division between the input resistance ($R_{in,CG}$) and the source resistance (R_S), which equals 1/2 in case of impedance matching:

$$\alpha_1 = \frac{R_{in,CG}}{R_{in,CG} + R_S} \tag{5}$$

The noise at the CS-output equals the CG-output noise ($v_{n,CS} = v_{n.in} \cdot A_{v,CS} = v_{n,CG}$), when the CS-gain $A_{v,CS}$ satisfies (4). Thus, the noise contribution of the CG-transistor can be canceled, as it becomes a purely common-mode signal at the differential output. This proofs that simultaneously balancing of the output signal and noise canceling is obtained. As the noise of the CG-transistor is cancelled, the CS-stage mainly determines the noise. By admittance scaling this noise contribution can be reduced at the cost of power consumption.

C. Distortion Canceling

As derived in [1], not only the noise of the impedance matching device, but also its distortion, due to the non-linearity of the transconductance, is canceled. We will show that also non-linearity of the output conductance of the CG-transistor is canceled.

The source signal (v_s) causes a non-linear drain-source current (i_{ds}) which is converted into a non-linear voltage at the input (v_{in}) via the (linear) source resistor R_S. The non-linear input voltage (v_{in}) can be written as a Taylor expansion of the signal source voltage (v_s):

$$v_{in} = \alpha_1 \cdot v_s + \alpha_2 \cdot v_s^2 + \alpha_3 \cdot v_s^3 + \alpha_4 \cdot v_s^4 + \ldots = \alpha_1 \cdot v_s + v_{NL} \tag{6}$$

where the α's represent Taylor coefficients and v_{NL} contains all unwanted nonlinear terms and the first Taylor coefficient (α_1) is defined in (5).

The output voltage of the CG-stage can be written as:

$$v_{out,CG} = i_{in} \cdot R_{CG} = \frac{v_s - v_{in}}{R_S} \cdot R_{CG} = \left((1-\alpha_1) \cdot v_s - v_{NL}\right)\frac{R_{CG}}{R_S} \tag{7}$$

where (6) is used. The output voltage of the CS-stage can be written using (4):

$$v_{out,CS} = -v_{in}\frac{R_{CG}}{R_S} = -\left(\alpha_1 \cdot v_s + v_{NL}\right)\frac{R_{CG}}{R_S} \tag{8}$$

The difference in sign of the wanted signal v_s and unwanted signal v_{NL} in (7) and (8) can be exploited: after subtraction only the linear signal remains:

$$v_{out,diff} = v_{out,CG} - v_{out,CS} = v_s \cdot \frac{R_{CG}}{R_S} \tag{9}$$

In conclusion, all noise and distortion currents generated by the CG-transistor can be canceled, irrespective whether produced due to non-linearity of the transconductance or non-linearity of the output conductance. The gain required in the CS-stage to cancel the distortion products of the CG-transistor equals the gain required to obtain output balancing, leading to the conclusion that *simultaneous balancing and cancelation of unwanted noise and distortion currents of the CG transistor is possible*. As the distortion due to the CG-transistor is canceled, while R_{CG} is normally quite linear, the CS-stage will determine the overall linearity of the complete LNA. The linearity of the CS-stage has been analyzed in detail in [13]. It appears possible to realize very good IIP2 values above +20dBm, if the CS-stage is carefully optimized. The simultaneous noise canceling and distortion canceling idea has recently also been exploited to achieve high IIP3 [11].

V. Balun-LNA with I/Q Down-Converter

Although parallel operating CG and CS stages reduce the required voltage gain of the CG stage by a factor two, achieving a high bandwidth when driving a significant capacitive load is problematic. For 50Ω matching and 12dB voltage gain, a drain resistance of more than 200Ω is needed, which limits the load capacitance to 80fF for 10GHz -3dB bandwidth. To obtain more bandwidth, we propose to avoid creating voltage gain at RF, but do this at IF. Fig. 2 shows the principle: a CG-CS stage is stacked with current commutating mixer. The mixer transistors are in saturation and present a low impedance to the CG-CS stage output, therefore the bandwidth at these nodes is high. At IF, where much less bandwidth is required, the mixer output current is converted to voltage. The drain impedance is Z for the CG-stage and Z/4 for the CS-stage to realize simultaneous balancing and noise/distortion canceling at IF. By using LO square-wave signals with 25% duty-cycle, one CG-CS transconductance-stage can supply the required signal current for both a differential I- and Q- output. This results in a very power efficient down-converter. The IF-filter averages the current

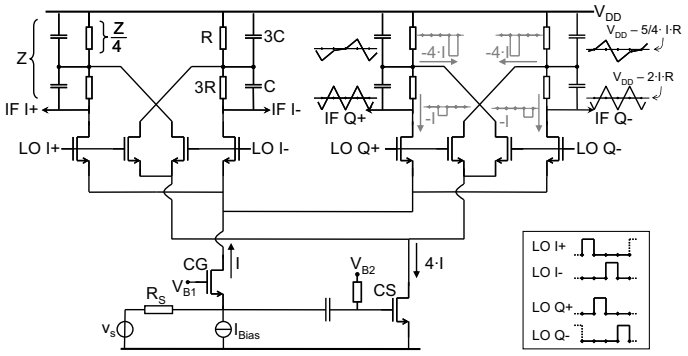

Fig. 2 A Balun-LNA with I/Q down-converter exploiting the CG-CS stage of Fig.1.

pulses through the load (see Fig. 2). As the CG/CS-bias currents do not flow continuously though the loads, the DC-drop across the loads is reduced, allowing an increased load impedance compared to the Balun-LNA of Fig. 1. This makes it possible to realize high voltage gain at IF, which remains high up to very high LO-frequencies.

Fig. 3 shows the gain, Noise Figure and S_{11} of a 65nm chip realizing the circuit of Fig. 2. Clearly it realized a very flat gain and noise figure up to 7GHz (the frequency range in simulation is actually higher, but is limited on the chip by the upper operating frequency of the LO-drivers) [14],[19].

VI. Conclusions

In this paper we reviewed recently proposed CMOS circuit techniques to realize wideband receivers. It turns out that a combination of a common gate and common source stage is an attractive option. It can implement an active balun, while it is also possible to exploit the simultaneous noise and distortion canceling property that reduces the noise and distortion of the common gate stage to negligible values. As this circuit has a gain equal to the sum of the gains of a CG and CS stage, it can realize an overall voltage gain close to 20dB even at a low supply voltage of 1.2V. It was also shown that the Balun-LNA can also be used as an RF transconductor, where a current commutation mixer I/Q mixer can be directly stacked on top of it to realize flat, very wideband gain.

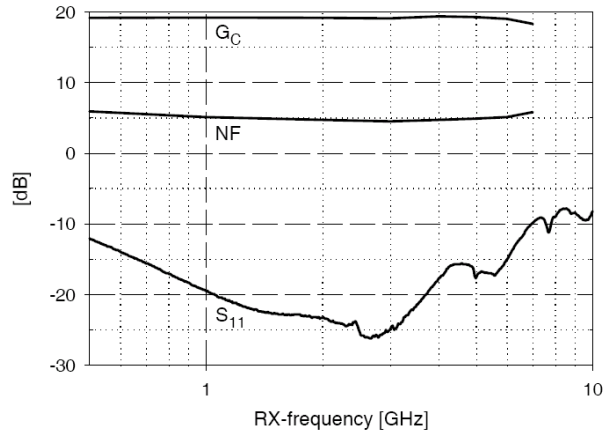

Fig. 3 Gain, Noise figure and S_{11} of a 65nm CMOS IC shown in Fig. 2. Note that the high and flat gain is achieved at only 1.2V supply.

References

[1] F. Bruccoleri, E.A.M. Klumperink, and B. Nauta, "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling," IEEE J. Solid-State Circuits, vol. 39, pp. 275-282, February 2004.

[2] S. Chehrazi, A. Mirzaei, R. Bagheri, and A. Abidi, "A 6.5 GHz Wideband CMOS Low Noise Amplifier for Multi-Band Use," Proc. IEEE Custom Integrated Circuits Conf. (CICC), pp. 801-804, Sept. 2005.

[3] J.-H.C. Zhan and S.S. Taylor, "A 5GHz Resistive-Feedback CMOS LNA for Low-Cost Multi-Standard Applications," ISSCC Dig. Tech.Papers, pp. 200-201, Feb. 2006.

[4] R. Bagheri et al, "An 800MHz to 5GHz Software-Defined Radio Receiver in 90nm CMOS", ISSCC Dig. Tech.Papers, 2006 pp. 1932 – 1941, Feb. 2006.

[5] S.C. Blaakmeer, E.A.M Klumperink, D.M.W. Leenaerts, and B. Nauta, "A wideband Noise-Canceling CMOS LNA exploiting a transformer," Dig. of papers RFIC Symposium, pp. 137-140, June 2006.

[6] R. Bagheri, A. Mirzaei, S. Chehrazi, M.E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A.A. Abidi, "An 800-MHz–6-GHz Software-Defined Wireless Receiver in 90-nm CMOS," IEEE J. Solid-State Circuits, vol. 41, pp. 2860-2876, December 2006.

[7] J. Borremans, P. Wambacq, and D. Linten, "An ESD-protected DC-to-6GHz 9.7mW LNA in 90nm digital CMOS," presented at Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007.

[8] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4V 25mW inductorless wideband LNA in 0.13µm CMOS," presented at Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007.

[9] S. Lee, et al, "A broadband receive chain in 65nm CMOS," presented at Digest of Technical Papers - IEEE International Solid-State Circuits Conference, pp. 418-419, 2007.

[10] C. F. Liao and S. I. Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receivers," IEEE Journal of Solid-State Circuits, vol. 42, pp. 329-339, 2007.

[11] W. H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," presented at Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium, pp. 61-64, 2007.

[12] S.C. Blaakmeer, E.A.M Klumperink, D.M.W. Leenaerts, and B. Nauta, "An Inductorless Wideband Balun-LNA in 65nm CMOS with balanced output," Proceedings of the 33rd European Solid-State Circuits Conference (München, Germany) , pp. 364 - 367, Sept. 2007.

[13] S.C. Blaakmeer, E.A.M Klumperink, D.M.W. Leenaerts, and B. Nauta, "Wideband Balun-LNA with Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling", IEEE J. Solid-State Circuits, vol. 43, pp. 1341-1350, June 2008.

[14] S.C. Blaakmeer, E.A.M Klumperink, D.M.W. Leenaerts, and B. Nauta, "A Wideband Balun LNA I/Q-Mixer combination in 65nm CMOS", Digest of Technical Papers - IEEE International Solid-State Circuits Conference, pp. 418-419, 2007.

[15] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters, " IEEE J. Solid-State Circuits, vol. 38, pp. 394-406, March 2003.

[16] ETSI. (2005, Nov.) Digital Video Broadcasting (DVB); DVB-H Implementation Guidelines. [Online], ETSI Document Number: TR 102 377, Version 1.2.1, Reference: RTR/JTC-DVB-175. Available: http://www.etsi.org/

[17] ECMA International. (2005, Dec.) High Rate Ultra Wideband PHY and MAC Standard. [Online], Available: http://www.ecma-international.org/publications/files/ECMA-ST/ECMA-368.pdf

[18] R. Roovers, et al, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology, " IEEE J. Solid-State Circuits, vol. 40, pp. 2563-2572, Dec. 2005.

[19] S.C. Blaakmeer, E.A.M Klumperink, D.M.W. Leenaerts, and B. Nauta, "The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology," accepted for publication in IEEE Journal of Solid-State Circuits, Dec. 2008.