Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling

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***Abstract*—Known elementary wide-band amplifiers suffer from a fundamental tradeoff between noise figure (NF) and source impedance matching, which limits the NF to values typically above 3 dB. Global negative feedback can be used to break this tradeoff, however, at the price of potential instability. In contrast, this paper presents a feedforward noise-canceling technique, which allows for simultaneous noise and impedance matching, while canceling the noise and distortion contributions of the matching device. This allows for designing wide-band impedance-matching amplifiers with NF well below 3 dB, without suffering from instability issues. An amplifier realized in 0.25-μm standard CMOS shows NF values below 2.4 dB over more than one decade of bandwidth (i.e., 150–2000 MHz) and below 2 dB over more than two octaves (i.e., 250–1100 MHz). Furthermore, the total voltage gain is 13.7 dB, the −3-dB bandwidth is from 2 MHz to 1.6 GHz, the IIP2 is +12 dBm, and the IIP3 is 0 dBm. The LNA drains 14 mA from a 2.5-V supply and the die area is 0.3 × 0.25 mm^2.**

***Index Terms*—Broadband, distortion canceling, low-noise amplifier (LNA), noise canceling, noise cancellation, wide band.**

I. Introduction

WIDE-BAND low-noise amplifiers (LNAs) are used in receiving systems where the ratio between bandwidth (BW) and its center frequency f_c can be as large as two. Application examples are analog cable (50–850 MHz), satellite (950–2150 MHz), and terrestrial digital (450–850 MHz) video broadcasting. Moreover, a wide-band LNA can replace several *LC*-tuned LNAs typically used in multiband and multimode narrow-band receivers. A wide-band solution saves chip area and fits better with the trend towards flexible radios with as much signal processing (e.g., channel selection, image rejection, etc.) as possible in the digital domain (toward "software radio").

High-sensitivity integrated receivers require LNAs with sufficiently large gain, noise figure (NF) well below 3 dB, adequate linearity, and source impedance matching $Z_{\rm IN} = R_{\rm S}$. The latter is to avoid signal reflections on a cable or alterations of the characteristics of the RF filter preceding the LNA, such as pass-band ripple and stop-band attenuation [1]. These requirements must be achieved over a wide range of frequencies while also allowing some variable gain to handle interference generated by strong adjacent channels.

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Traditional wide-band LNAs built of MOSFETs and resistors have difficulties in meeting the above-mentioned requirements. Known elementary amplifiers [2], [3] fail to achieve low NF upon $Z_{\rm IN} = R_{\rm S}$. On the other hand, amplifiers exploiting global negative feedback might achieve low NF with $Z_{\rm IN} = R_{\rm S}$, but they are prone to instability [4]. In this paper, a thermal-noise canceling technique is presented that allows for designing LNAs with low NF and source impedance matching over a wide range of frequencies without instability problems. In earlier work [2], [5], a limited form of noise cancellation was already presented. However, it does not allow for low NF $<$ 3 dB upon $Z_{\rm IN} = R_{\rm S}$. In contrast, the technique presented in this paper can reach much lower NF, as was validated through the design of a sub-2-dB noise figure wide-band LNA in a 0.25-μm CMOS [6]. This paper analyzes the noise-canceling technique and its properties in depth.

The paper is organized as follows. Section II reviews existing wide-band CMOS low-noise techniques. Section III introduces the noise-canceling technique. Section IV analyzes properties and limitations of noise canceling. Section V describes the IC design of a wide-band CMOS LNA. Section VI deals with the measurements. Finally, Section VII presents the conclusions.

II. Review of Existing Techniques

In this section, common wide-band CMOS low-noise techniques are reviewed in order to highlight their NF limitations. A MOSFET in saturation is modeled as a voltage-controlled current source with transconductance g_m. Its channel noise spectral density $4kT \cdot \text{NEF} \cdot g_m \cdot \Delta f$ is assumed the dominant source of noise. NEF $= \gamma \cdot g_{d0}/g_m$ is the noise excess factor, where g_{d0} is the channel conductance for $V_{\rm DS} = 0$ and γ is a parameter. For a submicron MOSFET, $g_{d0}/g_m > 1$ and $1 < \gamma < 2$ holds [8], resulting in an NEF well above 1.

Fig. 1(a)–(e) shows known elementary wide-band amplifiers capable of matching a real source impedance $R_{\rm S}$ (biasing not shown). These amplifiers suffer from a fundamental tradeoff between their noise factor F (NF $= 10\log_{10}(F)$) and impedance matching, $Z_{\rm IN} = R_{\rm S}$. For a sufficiently large gain, low F requires a large g_{mi} or R_i.[1] Conversely, impedance matching demands a fixed $g_{mi} = 1/R_{\rm S}$ or $R_i = R_{\rm S}$. F is larger than $1 + \text{NEF} \geq 2$ (i.e., 3 dB). This tradeoff is somewhat relaxed for the balanced common-gate LNA exploiting capacitive input cross coupling in Fig. 1(f) [3]. Still, F cannot be lower than $1 + \text{NEF}/2$ as the impedance-matching constraint still stands.

[1]For the amplifier in Fig. 1(a), low F demands the MOSFET g_m to be large as well.

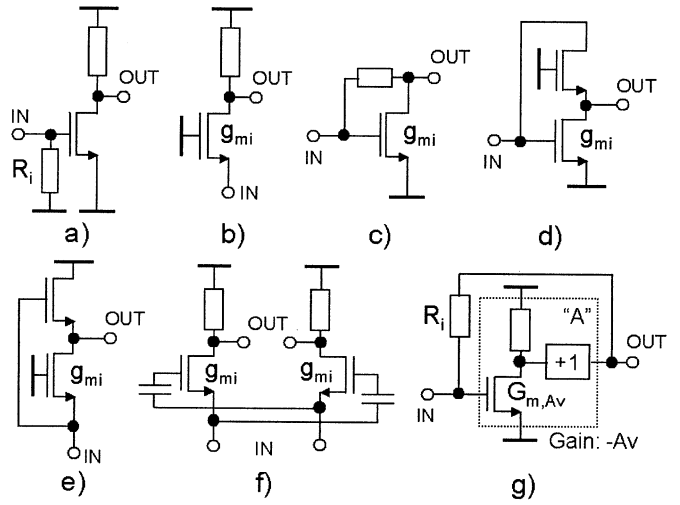

Fig. 1. Known wide-band LNAs (biasing not shown).

The tradeoff between F and source impedance matching $Z_{\rm IN} = R_{\rm S}$ can be broken, exploiting negative feedback properly. Fig. 1(g) shows a commonly used wide-band feedback amplifier capable of a low F upon $Z_{\rm IN} = R_i/(1 + A_{\rm v}) = R_{\rm S}$. In this case, the feedback resistor R_i determines the minimum noise factor[2] $F_{\rm MIN} = 1 + 1/(1 + A_{\rm v})$. The latter can be well below 2 (i.e., 3 dB), provided adequate gain $A_{\rm v}$ is available. Despite its noise performance, this amplifier suffers from important drawbacks, as follows, motivating the search for alternatives.

- Sufficient gain and gigahertz bandwidth often mandate the use of multiple cascaded stages *within* the feedback loop [2 in Fig. 1(g)], making its operation prone to instability.
- For $Z_{\rm IN} = R_{\rm S}$, the open-loop gain $A_{\rm v}/(2 + A_{\rm v})$ is lower than 1. Thus, the closed-loop linearity is not much better than that of the loop amplifier A. If A consists of cascaded stages and most of the gain is in the first one (i.e., to optimize noise), linearity can be poor [4].
- $Z_{\rm IN}$ depends on R_i and $A_{\rm v}$, so it is sensitive to process variations. Next, $Z_{\rm IN}$ and $A_{\rm v}$ are directly coupled and variable gain at $Z_{\rm IN} = R_{\rm S}$ is not straightforward.

III. Noise-Canceling Technique

In this section, a wide-band low-noise technique is presented, which is able to decouple F from $Z_{\rm IN} = R_{\rm S}$ without needing global negative feedback or compromising the source match. This is achieved by *canceling* the output noise of the matching device *without* degrading the signal transfer.

A. Noise Canceling Principle

To understand the principle of noise canceling, consider the amplifier stage of Fig. 1(c) redrawn in Fig. 2. Its input impedance is $Z_{\rm IN} = 1/g_{mi}$ and the voltage gain is $A_{\rm VF,MS} = V_Y/V_X = 1 - g_{mi}R$ where the index MS refers to the matching amplifier stage in Fig. 1(c). For $Z_{\rm IN} = R_{\rm S}$, its F is larger than 1+NEF, as discussed in the previous section. Let us now analyze the signal and the noise voltages at the input node X and output node Y, both with respect to ground, due to the noise current $I_{n,i}$ of the impedance-matching MOSFET. Depending on the relation between $Z_{\rm IN} = 1/g_{mi}$ and $R_{\rm S}$, a noise current $\alpha(R_{\rm S}, g_{mi}) \cdot I_{n,i}$, flows out of the matching MOSFET through R and $R_{\rm S}$ [Fig. 2(a)], with $0 < \alpha < 1$. This current causes two instantaneous noise voltages at nodes X and Y, which have equal sign. On the other hand, the signal voltages at nodes X and Y have opposite sign [Fig. 2(b)], because the gain $A_{\rm VF,MS}$ is negative, assuming $g_{mi}R > 1$. This *difference in sign for noise and signal* makes it possible to *cancel the noise* of the matching device, while simultaneously *adding the signal* contributions constructively. This is done by creating a new output, where the voltage at node Y is added to a scaled negative replica of the voltage at node X. A proper value for this scaling factor renders noise canceling at the output node, for the thermal noise originating from the matching device. Fig. 3(a) shows a straightforward implementation using an ideal feedforward voltage amplifier A with a gain $-A_{\rm v}$ (with $A_{\rm v} > 0$). By circuit inspection, the matching device noise voltages at node X and Y are

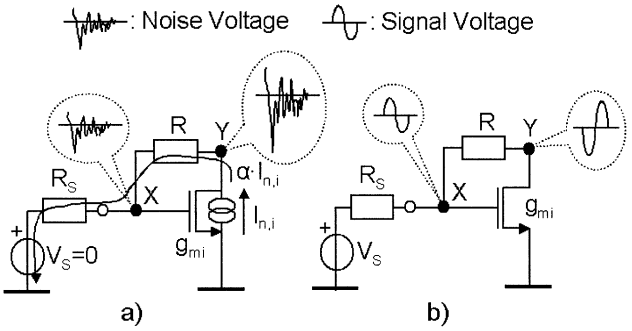

Fig. 2. Matching MOSFET (a) noise and (b) signal voltage at nodes X and Y for the amplifier in Fig. 1(c) (biasing not shown).

$$V_{X,n,i} = \alpha(R_S, g_{mi}) \cdot I_{n,i} R_S \qquad (1)$$
$$V_{Y,n,i} = \alpha(R_S, g_{mi}) \cdot I_{n,i}(R_S + R).$$

The output noise voltage due to the noise of the matching device, $V_{{\rm OUT},n,i}$ is then equal to

$$V_{{\rm OUT},n,i} = V_{Y,n,i} - V_{X,n,i} \cdot A_{\rm v} = \alpha(R_S, g_{mi}) \cdot I_{n,i}(R + R_S - A_{\rm v} R_S). \qquad (2)$$

Output noise cancellation, $V_{\rm OUT,n,i} = 0$, is achieved for a gain $A_{\rm v}$ equal to

$$A_{\rm v,c} = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R}{R_{\rm S}} \qquad (3)$$

where the index c denotes the cancellation. On the other hand, signal components along the two paths add constructively, leading to an overall gain (assuming $Z_{\rm IN} = 1/g_{mi} = R_{\rm S}$ and $A_{\rm v} = A_{\rm v,c}$)

$$A_{\rm VF,c} = \frac{V_{\rm OUT}}{V_{\rm X}} = 1 - g_{mi}R - A_{\rm v,c} = -g_{mi}R - \frac{R}{R_{\rm S}} = -2\frac{R}{R_{\rm S}}. \qquad (4)$$

[2]Since amplifier A is not constrained by matching, its contribution to F can be made arbitrarily small by increasing the $g_{m,Av}$ of its input stage at the price of power dissipation.

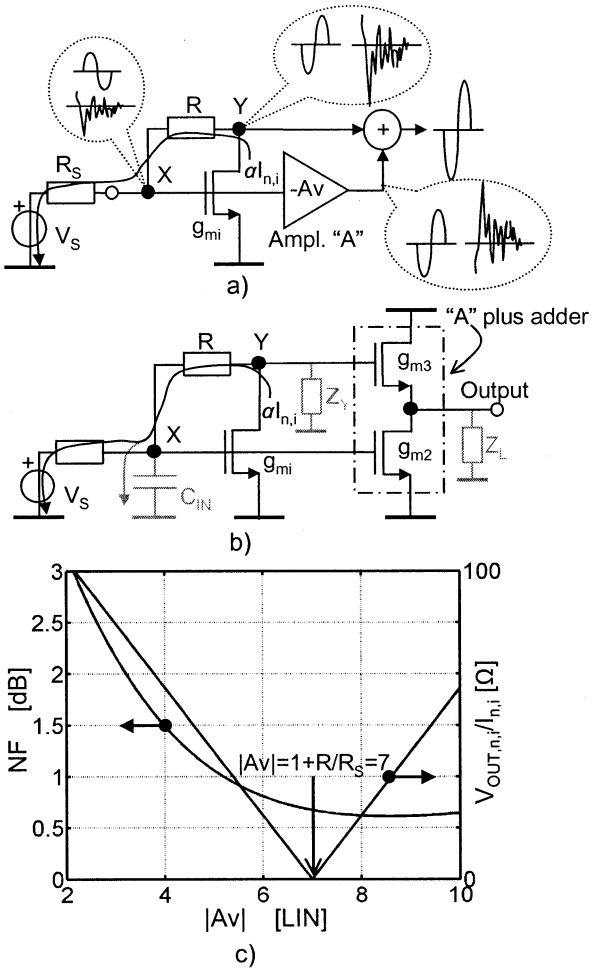

Fig. 3. (a) Wide-band LNA exploiting noise canceling. (b) Elementary implementation of amplifier A plus adder (biasing not shown). (c) Matching device noise transfer (right axis) and NF at 1 GHz (left axis) versus gain $A_{\rm v}$ for (a).

From (3), two characteristics of noise canceling are evident.

- Noise canceling depends on the absolute value of the *real* impedance of the source, $R_{\rm S}$ (e.g., the impedance seen "looking into" a properly terminated coax cable).
- The cancellation is independent on $\alpha(R_{\rm S}, g_{mi})$ and on the quality of the source impedance match. This is because any change of g_{mi} equally affects the noise voltages $V_{X,n,i}$ and $V_{Y,n,i}$.

Fig. 3(b) shows an elementary implementation of the noise-canceling LNA in Fig. 3(a). Amplifier A and the adder are replaced with the common-source stage M2–M3, rendering an output voltage equal to the voltage at node X times the gain $A_{\rm v} = g_{m2}/g_{m3}$. Transistor M3 also acts as a source follower, copying the voltage at node Y to the output. The superposition principle renders the final addition of voltages with an overall gain $A_{\rm VF} = 1 - g_{mi}R_{\rm S} - g_{m2}/g_{m3}$.

Note that *any* small signal that can be modeled by a current source between the drain and source of the matching device is cancelled as well (e.g., $1/f$ noise, thermal noise of the distributed gate resistance, and the bias noise current injected into node Y). However, the noise of R is not cancelled. This can be seen splitting its noise current $I_{n,Ri}$ in two correlated sources to ground, at the output node Y and the input node X. The former is cancelled for $A_{\rm v} = A_{\rm v,c}$, the latter is not.

B. Noise Factor

The noise factor F of the LNA in Fig. 3(a) can be written as

$$F = 1 + {\rm EF}_{\rm MD} + {\rm EF}_R + {\rm EF}_A \tag{5}$$

where the excess noise factor EF is used to quantify the contribution of different devices to F, where index MD refers to the matching device, R to the resistor R, and A to amplifier A. For the implementation in Fig. 3(b), expressions for EF for $Z_{\rm IN} = R_{\rm S}$ are (assuming equal NEF)

$$\begin{aligned} {\rm EF}_{\rm MD} &= {\rm NEF}\frac{(R + R_{\rm S} - A_{\rm v}R_{\rm S})^2}{R_{\rm S}A_{\rm VF}^2} \\ {\rm EF}_R &= \frac{1}{A_{\rm v} - 1} = -\frac{2}{A_{\rm VF}} \\ {\rm EF}_A &= {\rm NEF}\frac{8 - 6A_{\rm VF} + A_{\rm VF}^2}{g_{m2}R_{\rm S}A_{\rm VF}^2} \end{aligned} \tag{6}$$

Upon cancellation $A_{\rm v} = A_{\rm v,c}$, (6) becomes

$$\begin{aligned} {\rm EF}_{\rm MD,c} &= 0 \\ {\rm EF}_{R,{\rm c}} &= -\frac{2}{A_{\rm VF,c}} = \frac{R_{\rm S}}{R} \\ {\rm EF}_{A,{\rm c}} &= \frac{\rm NEF}{g_{m2}}\left(\frac{1}{R_{\rm S}} + \frac{3}{R} + \frac{2R_{\rm S}}{R^2}\right) \end{aligned} \tag{7}$$

The noise factor at cancellation, $F_{\rm c}$, is thus only determined by ${\rm EF}_{A,{\rm c}}$ and ${\rm EF}_{R,{\rm c}}$, neither of which are constrained by the matching requirement. ${\rm EF}_{A,{\rm c}}$ can be made arbitrarily smaller than 1 by increasing g_{m2} of its input stage, at the price of power dissipation. The minimum achievable $F_{\rm c}$ is now determined by ${\rm EF}_{R,{\rm c}}$. The latter can also be significantly smaller than 1 when the gain $|A_{\rm VF,c}|$ is large, which is desired in any case for an LNA. In practical design, $F_{\rm c}$ can be lowered below 2 (i.e., 3 dB) by increasing $g_{m2}R_{\rm S}$ until it saturates to $F_{\rm c,min} = 1 + {\rm EF}_{R,{\rm c}} = 1 + R_{\rm S}/R$.

The LNA concept in Fig. 3(a) was simulated using MOS model 9 in a 0.25-μm CMOS process using an ideal noiseless amplifier A (i.e., a voltage-controlled voltage source). The matching stage provides $Z_{\rm IN} = 1/g_{mi} \approx R_{\rm S} = 50\ \Omega$ with $R = 300\ \Omega$ and a voltage gain of $A_{\rm VF,MS} = 12.8$ dB. Fig. 3(c) shows the transfer function from $I_{n,i}$ to the LNA output $V_{\rm OUT}$ (right axis) versus $A_{\rm v}$. It is evaluated at 1 GHz, which is more than a factor of ten below the -3-dB bandwidth of the matching stage. This noise transfer is zero for $A_{\rm v} = A_{\rm v,c} = 7$, meaning that the noise from the matching device cancels at the output. On the other hand, the noise transfer rises for $A_{\rm v} \neq A_{\rm v,c}$ due to imperfect cancellation. Fig. 3(c) also shows the simulated NF versus $A_{\rm v}$ at 1 GHz (left axis). The NF drops from a maximum of 6 dB for $A_{\rm v} = 0$, (i.e., NF of the matching stage standalone) to ${\rm NF}_{\rm c} = 0.6$ dB for $A_{\rm v} = A_{\rm v,c} = 7$ (i.e., the contribution of R), which is very close to the value predicted from (3) and (7).

C. Generalization

The concept of noise canceling can be generalized to other circuit topologies according to the model shown in Fig. 4(a). It consists of the following functional blocks: 1) an amplifier stage

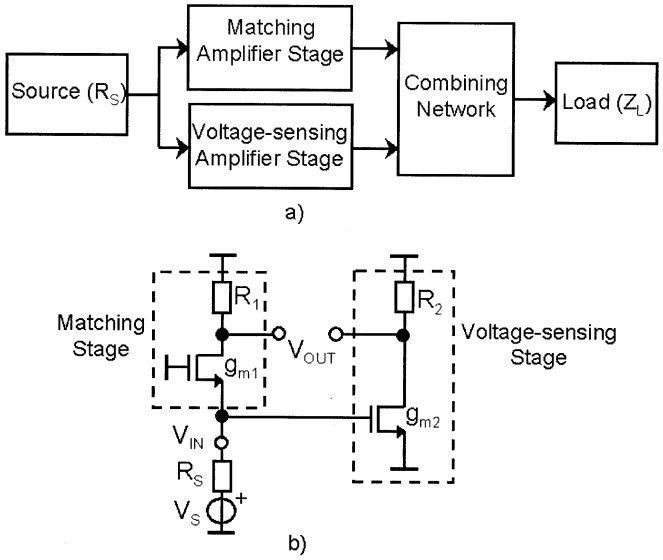

Fig. 4. (a) Block diagram of an LNA exploiting noise cancellation. (b) Alternative circuit example (biasing not shown).

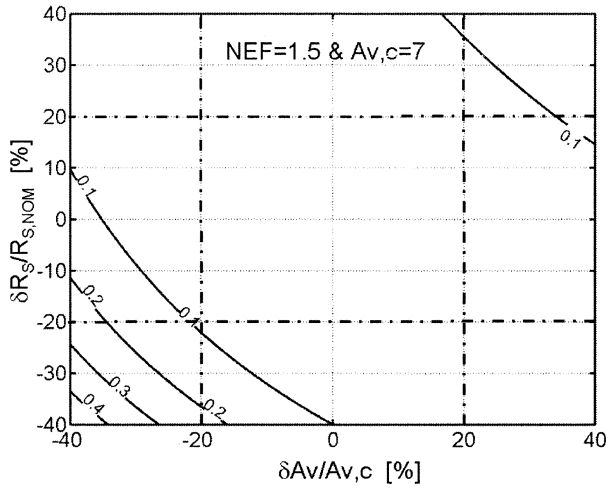

Fig. 5. Contribution to F of the matching device ($\delta\mathrm{EF_{MD}}$) versus $\delta R_\mathrm{S}/R_{\mathrm{S,NOM}}$ and $\delta A_\mathrm{v}/A_{\mathrm{v,c}}$.

providing the source impedance matching, $Z_\mathrm{IN} = R_\mathrm{S}$; 2) an auxiliary amplifier *sensing* the voltage (signal and noise) across the real input source; and 3) a network combining the output of the two amplifiers, such that noise from the matching device cancels while signal contributions add.

Fig. 4(b) shows another implementation example (biasing not shown) among several alternatives [9]. Noise cancellation occurs for $R_1 = g_{m2}R_\mathrm{S}R_2$, while low F requires high g_{m2}. The 2-MOSFETs in Fig. 4(b) is a well-known transconductor [10], also used for a double-balanced active mixer [11]. However, in both cases, noise canceling was apparently not recognized.

As shown in the previous section, the noise-canceling technique is capable of NF well below 3 dB upon $Z_\mathrm{IN} = R_\mathrm{S}$. Moreover, it offers advantages compared to feedback techniques.

- It is a feedforward technique *free* of global feedback, so instability risks are greatly relaxed.
- To first order, Z_IN depends only on g_{mi}. Thus, Z_IN is less sensitive to process spread.
- Implementing variable gain at $Z_\mathrm{IN} = R_\mathrm{S}$ is more straightforward due to the orthogonality between the gain A_VF and Z_IN (changing the value of R and A_v changes the gain, but not Z_IN).

Furthermore, it can be shown [9] that simultaneous noise and power matching is achieved.[3]

IV. Properties and Limitations

In this section, properties and limitations of noise canceling are analyzed. Although most of the conclusions of this section apply in general, for simplicity, we refer to the LNA in Fig. 3(a).

A. Robustness

The noise-canceling technique is relatively robust to device parameter variations. The cancellation depends only on a *reduced* set of device parameters. For instance, the impedance from node Y to ground Z_Y (e.g., g_d of the matching device), the load Z_L (e.g., g_d and g_{mb} of M3) and g_{mi} of the matching device in Fig. 3(b) do *not* affect the cancellation because they "load" the two feedforward paths in the same fashion. On the other hand, any deviation of the source resistance R_S and the gain A_v from their nominal values $R_{\mathrm{S,NOM}}$ and $A_{\mathrm{v,c}}$ affect the cancellation, as shown by (3). Using (6) and assuming for $Z_\mathrm{IN} = R_{\mathrm{S,NOM}}$, deviations δR_S and δA_v lead to a variation of $\mathrm{EF_{MD}}$ given by

$$\delta\mathrm{EF_{MD}} = \frac{\mathrm{NEF}}{4}\cdot\frac{\left[\frac{\delta R_\mathrm{S}}{R_{\mathrm{S,NOM}}}\left(1-\frac{1}{A_{\mathrm{v,c}}}\right)+\frac{\delta R_\mathrm{S}}{R_{\mathrm{S,NOM}}}\frac{\delta A_\mathrm{v}}{A_{\mathrm{v,c}}}+\frac{\delta A_\mathrm{v}}{A_{\mathrm{v,c}}}\right]^2}{\left(1+\frac{\delta R_\mathrm{S}}{R_{\mathrm{S,NOM}}}\right)\left(1-\frac{1}{A_{\mathrm{v,c}}}+\frac{1}{2}\frac{\delta A_\mathrm{v}}{A_{\mathrm{v,c}}}\right)^2}. \tag{8}$$

Contours of (8) are shown in Fig. 5 for $\mathrm{NEF} = 1.5$ and $A_{\mathrm{v,c}} = 7$. Clearly, $\delta R_\mathrm{S}/R_{\mathrm{S,NOM}}$ and $\delta A_\mathrm{v}/A_{\mathrm{v,c}}$ as large as $\pm 20\%$ are needed in order to raise $\delta\mathrm{EF_{MD}}$ to only 0.1, one tenth of the contribution of the input source. Thus, the sensitivity to variations of R_S and the gain A_v is low.

B. Distortion Canceling

The same mechanism leading to cancellation of the output noise due to the matching device can also be exploited to cancel its distortion components. In the following, distortion is assumed to originate only from the nonlinear memoryless voltage to current conversion of the matching device. Using a Taylor approximation, the drain-current variations of the matching device can be written as $I_\mathrm{NL} = g_{mi}V_X + I_\mathrm{NL}$, where I_NL denotes all nonlinear high-order terms. From inspection of the circuit in Fig. 3(a), the signal voltage at nodes X and Y can now be written as

$$\begin{aligned} V_X &= V_\mathrm{S} - R_\mathrm{S}(g_{mi}V_X + I_\mathrm{NL}) \\ V_Y &= V_\mathrm{S} - (R_\mathrm{S}+R)(g_{mi}V_X + I_\mathrm{NL}) \end{aligned} \tag{9}$$

Equation (9) shows that the distortion voltage at node Y has $1+R/R_\mathrm{S}$ times higher amplitudes than at node X and has *equal sign*, exactly in the same way as in (1) for the noise. Therefore, a gain $A_\mathrm{v} = A_{\mathrm{v,c}} = 1 + R/R_\mathrm{S}$ cancels all nonlinear terms

[3]This is strictly true for frequencies where parasitic capacitors can be neglected.

contributed by the matching device like it cancels its noise contribution (i.e., *simultaneous* noise and distortion cancellation). On the other hand, the nonlinearity of amplifier A increases the output distortion. Nevertheless, this distortion canceling might prove an useful asset in linear receiver designs.

C. High-Frequency Limitations

The −3-dB bandwidth $f_{-3\mathrm{dB}}$ of the amplifier in Fig. 3(b) has been analyzed using a dominant pole estimation technique. Assuming parasitic node capacitors C_{IN}, C_Y and C_L, and $Z_{\mathrm{IN}} = R_{\mathrm{S}}$, results in

$$f_{-3\mathrm{dB}} \approx \frac{1}{\pi R_{\mathrm{S}} C_{\mathrm{IN}} + 2\pi R_Y C_Y + 2\pi R_{\mathrm{OUT}} C_L} \tag{10}$$

where $R_Y \approx (R + R_{\mathrm{S}})/2$ is the resistance from node Y to ground and R_{OUT} is the amplifier output impedance. For $A_{\mathrm{v}} = A_{\mathrm{v,c}}$, (10) can be written as

$$f_{-3\mathrm{dB}} \approx \frac{1/\pi}{C_{\mathrm{IN}} R_{\mathrm{S}} + \left(C_Y R_{\mathrm{S}} + \frac{2C_L}{g_{m2}}\right)\left(1 - \frac{A_{\mathrm{VF,c}}}{2}\right)}. \tag{11}$$

Equation (11) shows how the capacitors determine the bandwidth for a given $A_{\mathrm{VF,c}}$ and g_{m2}.

Circuit parasitic capacitors not only limit the signal bandwidth but also degrade noise and distortion cancellation. In order to investigate the dominant frequency limitations of noise canceling, the simplified case of Fig. 3(b) with $C_Y = C_L = 0$ appears to be adequate. Here, C_{IN} accounts for the parasitic capacitance contributed to the input node mainly by the matching device and amplifier A. This simple model is realistic because: 1) C_Y and the load C_L in Fig. 3(b) do not affect the cancellation and 2) C_L does not affect the F of the LNA standalone. The noise current $\alpha \cdot I_{n,i}$ flowing out from the matching device "sees" a complex source impedance $Z_{\mathrm{S}}(f) = R_{\mathrm{S}}/(1 + \mathrm{j}2\pi f C_{\mathrm{IN}})$ as shown in Fig. 3(b). In this case, the output noise due to the matching device, $V_{\mathrm{OUT,n,i}}(f)$, is obtained by replacing R_{S} with $Z_{\mathrm{S}}(f)$ in (2) asfollows:

$$V_{\mathrm{OUT,n,i}}(f) = \frac{\alpha(Z_{\mathrm{S}}(f), g_{mi}) \cdot I_{n,i}(R + R_{\mathrm{S}} - A_{\mathrm{v}} R_{\mathrm{S}} + \mathrm{j}2\pi f C_{\mathrm{IN}} R_{\mathrm{S}} R)}{1 + \mathrm{j}2\pi \mathrm{f} C_{\mathrm{IN}} R_{\mathrm{S}}}. \tag{12}$$

Equation (12) shows that exact noise cancellation occurs only at dc for $A_{\mathrm{v}} = A_{\mathrm{v,c}}$. As the frequency increases, the cancellation degrades because C_{IN} (i.e., the complex source impedance $Z_{\mathrm{S}}(f)$) affects the noise voltage at node X and Y in a different manner, e.g., $V_{X,n,i}(f \to \infty) \to 0, V_{Y,n,i}(f \to \infty) \to I_{n,i} \cdot R$.

The frequency-dependent noise factor $F_{\mathrm{c}}(f)$ can now be written as

$$F_c(f) = F_c + (F_c - 1 + \mathrm{NEF}) \cdot (f/f_0)^2 \tag{13}$$

where F_{c} is the low-frequency noise factor as given in (5) and $f_0 = 1/(\pi \cdot R_{\mathrm{S}} \cdot C_{\mathrm{IN}})$ is the input pole. For F_{c} smaller than $1 + \mathrm{NEF}, F_{\mathrm{c}}(f) - F_{\mathrm{c}}$ increases with f/f_0 mainly because the cancellation degrades. However, this effect and the increase of $F_{\mathrm{c}}(f)$ with the frequency can be modest up to relatively high frequencies because of the low input-node resistance $R_{\mathrm{S}}/2$. Equation (13) shows the importance of maximizing f_0 (i.e., minimizing C_{IN}) in order to mitigate the degradation of noise factor. This can be done by increasing $V_{\mathrm{GS}} - V_{\mathrm{T0}}$ of Mi and M2, cascoding to reduce the Miller effect, by frequency compensation, e.g., so-called shunt-peaking technique or using a more advanced deep-submicron CMOS process with higher f_T.

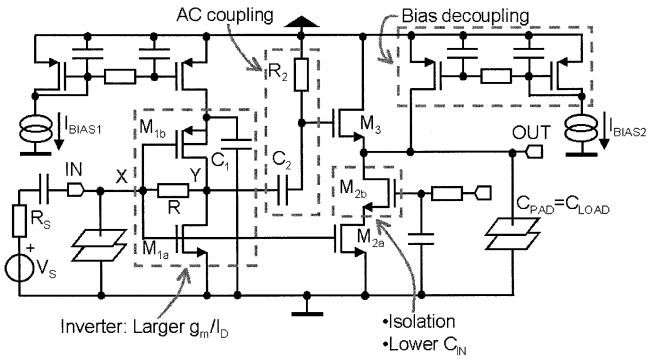

Fig. 6. Schematic of the wide-band CMOS LNA.

V. LNA IC Design

A wide-band LNA according to the concept of Fig. 3(b) was designed in a 0.25-μm standard CMOS process. The design was aimed at low NF over a wide range of frequencies. No attempt was made to optimize linearity because at the time of this design we were not aware yet of the possibility to cancel distortion. The following requirements for high-sensitivity applications were targeted: 1) signal bandwidth from a few megahertz to 2 GHz (covering most mobile communication bands); 2) voltage gain: $A_{\mathrm{VF}} = V_{\mathrm{OUT}}/V_{\mathrm{IN}} = 10 = 20$ dB; 3) $Z_{\mathrm{IN}} = R_{\mathrm{S}} = 50\ \Omega$; and 4) NF well below 3 dB over the bandwidth.

Fig. 6 shows the LNA schematic. The matching stage exploits shunt feedback around a CMOS inverter to provide the input impedance $Z_{\mathrm{IN}} \approx 1/g_{m1} = 1/(g_{m1a} + g_{m1b})$. To reduce the sensitivity of gain and Z_{IN} to variations in the supply voltage, the inverter is biased via a current mirror while a large MOS capacitor $C_1 = 13$ pF grounds the source of M1b. The matching stage is ac coupled to M3 via the high-pass filter $C_2 - R_2$ (i.e., 0.8 pF and 95 kΩ). The cascode M2b improves the isolation and reduces the input capacitance by decreasing the Miller effect due to M2a. In order to fit a supply voltage of 2.5 V, M3 conducts only part of the drain current of M2. This is done without sacrificing NF because the LNA gain is large and enough voltage headroom is available for the output mirror. The capacitance of the output bondpad $C_{\mathrm{PAD}} = 0.2$ pF is used as load. The design of the LNA was targeted to a NF of 1.9 dB for $R_{\mathrm{S}} = 50\ \Omega$. To achieve this aim, the following design procedure was followed.

- Design equations for F, A_{VF} and Z_{IN} more precise than (4), (6), and $1/g_{m1}$ were derived in order to take into account the effect of the output conductance g_{d1} of M1 and the body transconductance g_{mb3} of M3 [9].
- The noise factor was then optimized at its minimum for $Z_{\mathrm{IN}} = R_{\mathrm{S}}$ and a given gain A_{VF} and $g_{m2}R_{\mathrm{S}}$. By introducing a deliberate noise-cancellation error, $\varepsilon_{\mathrm{OPT}} = 1 + R/R_{\mathrm{S}} - g_{m2}/g_{m3}$, the optimal F, F_{OPT}, can be lower

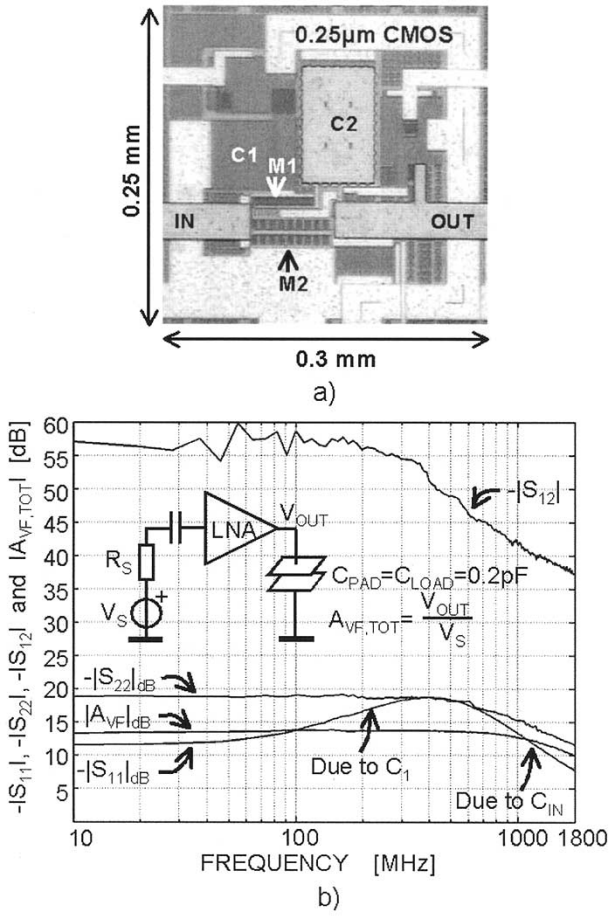

Fig. 7. (a) Chip photograph. (b) Measured S-parameters and the total voltage gain $A_{\mathrm{VF,TOT}}$.

than F_{c}.[4] This behavior occurs because, for $\varepsilon = \varepsilon_{\mathrm{OPT}}$, the increase of $\mathrm{EF}_{\mathrm{MD}}$ is compensated by a larger decrease of EF_A [9].

The following values for the design parameters were chosen for the final design: $g_{m1}R_{\mathrm{S}} = 1.35, g_{m2}R_{\mathrm{S}} = 4.9, g_{m3}R_{\mathrm{S}} = 0.96$, and $R/R_{\mathrm{S}} = 8$. The supply current is about 14 mA.

VI. Measurements

Fig. 7(a) shows the chip photograph of the wide-band LNA. On-wafer S-parameter measurements were carried out, and Fig. 7(b) shows the resulting $\mathrm{S}_{11}, \mathrm{S}_{22}, \mathrm{S}_{12}$ and the total gain $A_{\mathrm{VF,TOT}} = V_{\mathrm{OUT}}/V_{\mathrm{S}}$ from 1 to 1800 MHz. A flat gain of 13.7 dB is found over a −3-dB bandwidth between 2 and 1600 MHz. At 1800 MHz, the gain is still 10 dB. The reverse isolation $|\mathrm{S}_{12}|$ is better than −42 dB up to 1 GHz and better than −36 dB up to 1.8 GHz. The input match $|\mathrm{S}_{11}|$ is better than −10 dB for 10–1600 MHz and better than −8 dB for 10–1800 MHz. At low frequencies, $|\mathrm{S}_{11}|$ drops due to the shunt capacitor C_1 in the matching stage. At high frequencies, $|\mathrm{S}_{11}|$ rises due to C_{IN}. NF and distortion were measured with the chip die glued to a low-loss ceramic substrate with 50-Ω input/output transmission lines connected via short bondwires.

[4]This effect is also in (6) [see Fig. 3(c)], but the difference between F_{c} and F_{OPT} is larger when the output conductance of M1 and the body effect of M3 are taken into account.

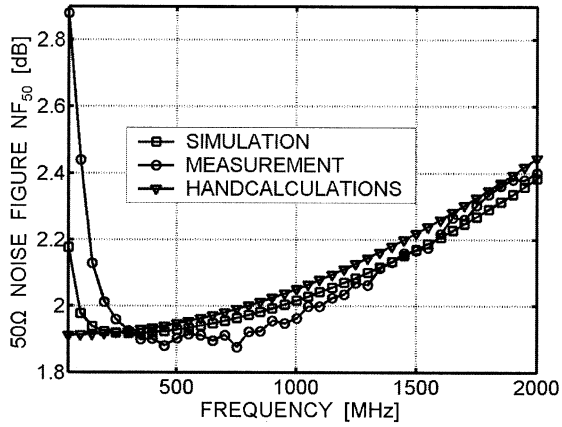

Fig. 8. Measured, simulated, and calculated NF versus frequency.

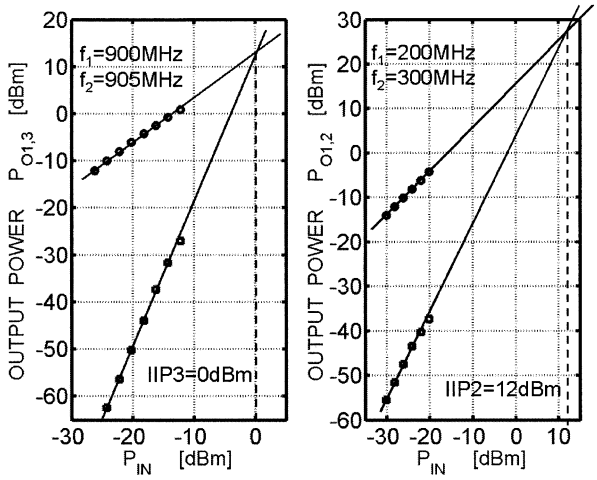

Fig. 9. Measured two-tone IIP2 and IIP3.

Fig. 8 shows the measured, simulated, and the calculated 50-Ω NF using the improved formula [9]. The measured NF is below 2.4 dB over more than one decade (150–2000 MHz) and below 2 dB over more than two octaves (250–1100 MHz). At low frequency, the NF rises due to the high-pass filter C2-R2. At high frequencies, the input capacitance mainly degrades the NF. The agreement with simulation and hand calculation is satisfactory. Fig. 9 shows a two-tone IIP2 = +12 dBm and IIP3 = 0 dBm. This distortion is due to the nonlinearity of the common-source stage M2–M3 and the matching stage as $\varepsilon_{\mathrm{OPT}} = 1 + R/R_{\mathrm{S}} - g_{m2}/g_{m3} \neq 0$ was used to lower F. Table I summarizes the measurements.

VII. Conclusion

In this paper, a wide-band noise-canceling technique was presented, which is able to break the tradeoff between noise factor F and source impedance matching without degrading the signal transfer or the quality of the source match. This is done placing an auxiliary voltage-sensing amplifier in feedforward to the matching stage such that the noise from the matching device cancels at the output, while adding signal contributions. In this way, one can minimize the LNA noise figure, at the price of power dissipation in the auxiliary amplifier. By using

TABLE I
SUMMARY OF THE MEASUREMENTS

$A_{VF,TOT}=\|V_{OUT}/V_S\|$	13.7dB
-3dB Bandwidth	2-1600 MHz
$\|S_{12}\|$	<-36dB in 10-1800 MHz
$\|S_{11}\|$	<-8dB in 10-1800 MHz
$\|S_{22}\|$	<-12dB in 10-1800 MHz
IIP3 (Input Ref.)	0dBm (f_1=900MHz & f_2=905MHz)
IIP2 (Input Ref.)	12dBm (f_1=300MHz & f_2=200MHz)
ICP1dB (Input Ref.)	-9dBm (f_1=900MHz)
$NF_{50\Omega}$	<= 2dB in 250-1100 MHz <= 2.4dB in 150-2000 MHz
$I_{DD}@V_{DD}$	14mA@2.5Volt
Area	0.3x0.25 mm^2
Technology	0.25µm CMOS

this technique in an LNA, low noise figures over a wide range of frequencies can be achieved, greatly relaxing the instability issues that are typically associated with wide-band amplifiers exploiting global negative feedback. Other attractive assets of the technique are:

- simultaneous cancellation of noise and distortion terms due to the matching device;
- simultaneous noise and power matching for frequencies where the effect of parasitic capacitors can be neglected;
- orthogonality of design parameters for input impedance and gain, allowing for an easier implementation of variable gain while maintaining input impedance matching;
- robustness to variations in device parameters and the external source resistance R_S;
- applicability in other IC technologies and amplifier topologies.

Measurement results of a wide-band LNA realized in 0.25-μm standard CMOS show 1.6-GHz bandwidth, NF values below 2.4 dB over more than one decade of bandwidth, and below 2 dB over more than two octaves. Table I provides a more complete summary of the measurements.

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