SYSTEMATIC GENERATION OF WIDE BAND CMOS LOW-NOISE AMPLIFIER TOPOLOGIES

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Alternative wide band Low-Noise Amplifier (LNA) topologies to be used for highly integrated CMOS transceivers are investigated. A methodology that systematically generates all the LNA topology options with 2 Voltage Controlled Current Sources (VCCS) is presented. Next to well-known circuits such as the common gate stage and shunt series feedback common source stage, 2 alternative LNA topology are found. Hand calculations indicate that these topologies have promising noise and intermodulation properties.

1 Introduction

Deep sub-micron digital CMOS is nowadays fast enough to enable the realization of RF circuits in the low GHz region. Moreover, unlike traditional bipolar, CMOS is a better candidate towards the low cost single-die radio goal. On the road towards full monolithic integration, a key issue is the development of high-performance CMOS analogue building blocks. The Low-Noise Amplifier (LNA) in the receiver path is one of these blocks. The LNA (thermal) noise fundamentally limits the sensitivity of the receiver, whereas its intermodulation distortion affects the inter-channel interference. Moreover, accurate input match and high operation frequency are desired, while only low power consumption is acceptable for portable devices. Such high performance can be achieved boosting the transistor performance by means of resonant LC tank. However, the price to be paid is a frequency operation confined within a *narrow band*. In contrast, we address *wide band* LNAs. The latter are needed for simultaneous processing of several signal channels in cable TV receivers, high-data rate communications systems and base stations. Wide band LNAs can not enjoy the benefits associated to "working around the resonance frequency", which makes their design rather challenging in CMOS. Many LNA designs rely on the re-use of *few* consolidated circuit topology concepts (e.g. common gate -CG- and the shunt-series feedback common source -SSFCS- stages) to achieve the required performance. This leads to a design philosophy aimed at squeezing as much performance as possible out of well-known circuits. However, this approach can be difficult to apply due to:

- Low-voltage constraint. A circuit topology can become obsolete if it does not fit within the supplies.
- Fundamental limits. Circuit performance is basically limited by the topology concept it self. Thus, the desired performance may be achieved only using alternative circuits.

Moreover, the availability of a large arsenal of circuit topologies would greatly help designers enlarging the number of the valuable design options. In this perspective, this paper aims to search for alternative high-performance LNA circuit topologies suited for highly integrated CMOS transceivers, focusing mainly on the methodological aspects that are beside it. To generate LNA topologies a systematic approach is adopted, which is thought to be effective in minimising the chance to overlook useful design options.

LNAs are typically simple circuits with few active devices in the signal path. Modelling the MOS transistor (in saturation) as a Voltage Controlled Current Source -VCCS- (see Fig.1), simple LNA circuits can be seen as circuits with 2 VCCSs [1,2]. This step back from the transistor level is at the base of a developed systematic *top-down* methodology that, starting from properly defined *top*-level LNA functional requirements and boundary conditions for the allowed source and load impedance, generates *all* the (2VCCSs) LNA topologies *down* at transistor level. To pursue this aim a recently generated database of graphs of *all* the circuits with 2 VCCSs (see Fig. 2) is used as a starting point [1]. The paper is divided in two main parts: first the methodology to generate *all* the wide band LNA

topology alternatives is described then, selected topologies are compared by means of proper figures of merit in order to highlight their specific strong and weak points.

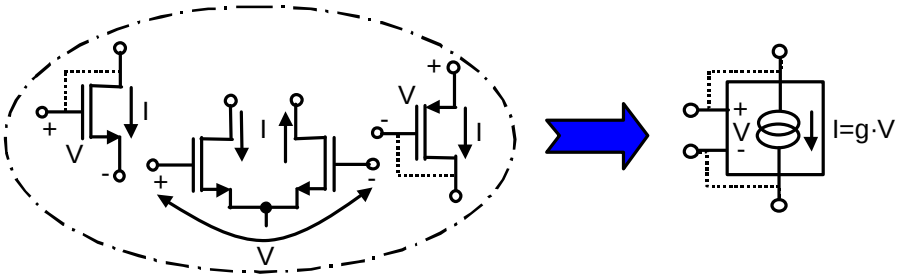

Fig.1: VCCS representation of simple MOS circuits.

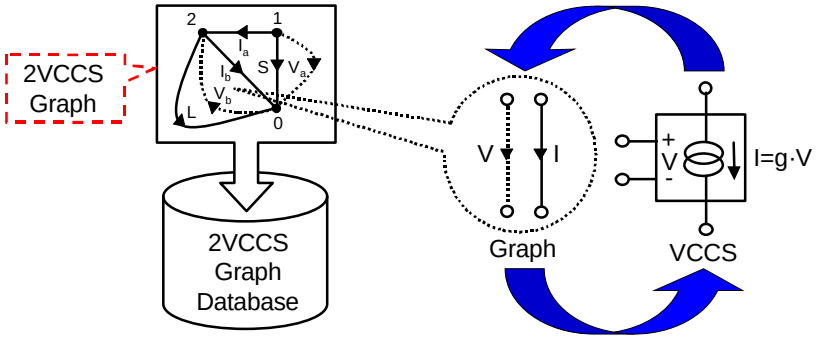

Fig.2: Graph of a 2VCCS circuit.

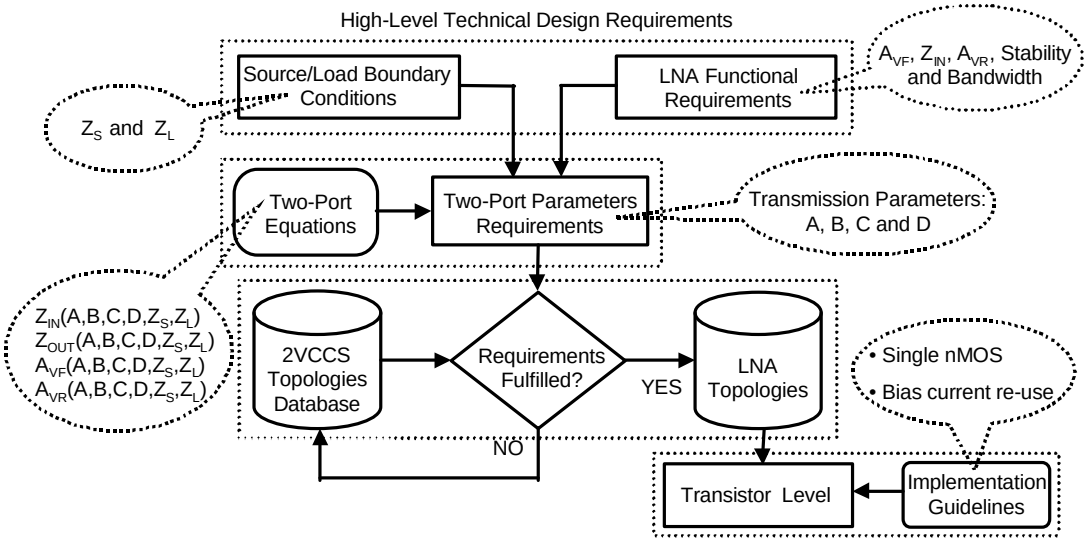

Fig.3: Block diagram of the generation methodology.

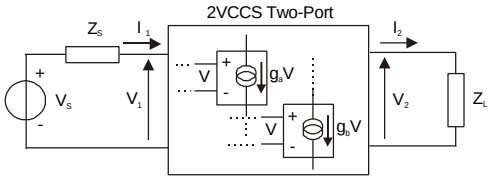

Fig.4: 2VCCS two-port model.

2 The method

A LNA can be seen as a two-port circuit. Any commonly used set of two-port parameters (e.g. admittance parameters $\{y_{ij}\}$) can be used to determine its small signal operation. Thus, the functional behaviour of the LNA is fully determined if the two-port parameters are known upon properly defined boundary conditions for the source and load impedance. This simple task is at the base of the developed methodology (see Fig.3), which generates *all* the 2VCCS LNA topologies suitable for highly integrated CMOS receivers. The latter proceeds along the following steps.

1. Boundary conditions for the source and load impedance as well as high-level LNA functional requirements suitable for highly integrated CMOS transceivers are established.
2. LNA functional requirements are translated into requirements for the two-port small signal parameters: (a)Useful combinations of parameters. (b)Constraints on their value.
3. The 2VCCS topologies database is then explored. The 2VCCS circuits that do not meet the previously defined requirements are rejected. The remaining topologies are the output of the generation methodology: the 2VCCS LNA topologies database.
4. Guidelines are then defined to obtain implementations at (MOS)transistor level.

In the sections below the blocks of Fig.3 are discussed.

2.1 2VCCS topologies database

The 2VCCS topologies database contains the circuit topologies to be used as input for the developed methodology (see Fig. 2). The main database characteristics are:

- It contains *all* (145) the graphs of circuits with 2 VCCS ($VCCS_a$ and $VCCS_b$), a source and a load providing a non-zero signal transfer. We will refer to these graphs as the 2VCCS graphs.
- The 2VCCS circuits are modelled as a two-port (see Fig.4) described in term of transmission parameters {A, B, C, D}, which are defined as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \Rightarrow \begin{array}{ll} \frac{1}{A} = \frac{V_2}{V_1}(I_2 \equiv 0) & \frac{1}{B} = \frac{I_2}{V_1}(V_2 \equiv 0) \\ \frac{1}{C} = \frac{V_2}{I_1}(I_2 \equiv 0) & \frac{1}{D} = \frac{I_2}{I_1}(V_2 \equiv 0) \end{array}$$

  Transmission parameters are assumed to be *real* functions of *positive* transcoductances g_a and g_b of the 2 VCCS.
- The 2VCCS circuits are classified with respect to: (a)Combinations of transmission parameters. (b)Transmission parameters expressions of g_a and g_b.

2.2 Source and load boundary conditions

For different receiver architectures, different types of LNA source impedance Z_S and load impedance Z_L can occur. In traditional heterodyne-based architectures the LNA drives and is driven by an off-chip passive band-pass filter providing a standard $R_{50\Omega}$ input and output resistance, so $Z_L=Z_S=R_{50\Omega}$. In highly integrated CMOS receivers, the pre-select duplex filter driving the LNA is still required [3]. Thus, Z_S remains constrained to be 50Ω, but now designers may have the freedom to choose *character* and *value* of the on-chip load impedance. For CMOS, particularly interesting is the case when the load is capacitive (e.g. the gate capacitance of a MOS transistor). In the following analysis we assume the following boundary conditions for the source and load impedance: $\{Z_S \equiv R_{50\Omega}$ & $Z_L \equiv 1/(S \cdot C_L)\}$.

2.3 LNA functional requirements

To perform topology rejection the following LNA functional requirements are defined:

- **Forward Gain.** The LNA primarily provides a certain amount of forward (voltage) gain A_{VF} ($\equiv V_2/V_1$, see Fig.4) in order to boost the signal above the noise floor, so $|A_{VF}| > 1$ must hold.

- **Input Impedance.** Accurate matching of the LNA source impedance is needed for the sake of maximum transfer of power from the source or to terminate correctly the external duplex filter. Thus, $Z_{IN} \equiv R_{50\Omega}$ must holds.
- **Reverse Gain.** Negligible reverse gain A_{VR} ($\equiv V_1/V_2$ for $V_S=0$, Fig.4) is required to prevent signal leakage through the mixer to the antenna and consequent spurious emissions, so $|A_{VR}| \ll 1$ must hold. In direct conversion receivers for instance, very low reverse gain is required as the leakage to the antenna may be solely limited by the LNA reverse gain [4].
- **Stability.** Stability is a crucial requirement in order to establish the correct small signal operation of the LNA. In RF circuit design stability is typically required to be unconditional. The latter means a stable LNA whatever are the -passive- source and load impedance terminations [5].
- **Bandwidth.** The LNA must perform well within the assigned frequency-band. For wide band operation, the LNA output impedance is limited to $Z_{OUT} \in \{0, << Z_L\}$. This is because for $Z_{OUT} = \infty$ the LNA output current is converted to voltage through the capacitive load, resulting in a integrator-like transfer function. Thus, a wide-band LNA is assumed to be a two-port circuit with (maximum) power sensing input and (maximum) voltage delivering output ports.

$$\begin{aligned} Z_{IN} &= \frac{A + B \cdot SC_L}{C + D \cdot SC_L} \\ Z_{OUT} &= \frac{D \cdot R_{50W} + B}{C \cdot R_{50W} + A} \\ A_{VF} &= \frac{1}{A + B \cdot SC_L} \\ A_{VR} &= \frac{A \cdot D - B \cdot C}{D + \dfrac{B}{R_{50W}}} \end{aligned} \qquad (1)$$

2.4 Two-port parameters requirements

The LNA functional requirements are translated to requirements for the transmission parameters using the two-port equations in (1). We are interested in: a)Useful combination of {A,B,C,D} parameters. b)Constraints on their value.

According to the Z_{IN} in (1), 9 combinations of transmission parameters provides $Z_{IN} \neq \infty$: {AD, AC, BD, BC, ABC, ABD, BCD, ACD, ABCD}, where AD indicates a two-port with transmission parameters {A, 0, 0, D}. Within these cases, combinations {AD, BD, BC, ABD, BCD} can not simultaneously meet the wide-band input match and output impedance requirements. Thus, useful two-port have transmission parameters from the set {AC, ACD, ABC and ABCD}. Using the forward gain condition $|A_{VF}| > 1$ it can be easily shown that $|A| < 1$ must hold. Reverse gain is also an important issue. If very low reverse gain is required, a further restriction to cases {AC, ABCD for AD=BC} may be needed as they do provide $A_{VR}=0$. This is because cases ACD and ABC have a reverse gain that can never be lower than $1/|A_{VF}|$. Necessary and sufficient conditions for unconditional stability of a two-port network can be expressed in term of transmission parameters as [6]:

$$\begin{aligned} \Re\{Z_{IN}\} &= \Re\left\{\frac{A + B \cdot SC_L}{C + D \cdot SC_L}\right\} = \frac{A \cdot C + D \cdot B \cdot w^2 C_L^2}{C^2 + D^2 \cdot w^2 C_L^2} \geq 0 \quad , \forall w C_L \\ \Re\{Z_{22}\} &= \frac{D}{C} \geq 0 \end{aligned} \qquad (2)$$

where $\Re\{\cdot\}$ means real part of $\{\cdot\}$. This is equivalent to require transmission parameters to have *all the same sign.* Moreover, unconditional stability and the input matching impose a fundamental constraint on the forward-reverse gain product:

$$|A_{VF} \cdot A_{VR}| < \left| \frac{1 - \dfrac{B}{D \cdot R_{50W}}}{1 + \dfrac{B}{D \cdot R_{50W}}} \right| < 1 \qquad (3)$$

LNA FUNCTIONAL REQUIREMENT	TWO-PORT {A, B, C, D} PARAMETERS REQUIREMENTS
$Z_{IN} \equiv R_{50\Omega}$	Useful cases: • {AC, ACD, ABC, ABCD} OR {AC, ABCD*} • |A| < 1 and A, B, C, D *all the same sign*
$Z_{OUT} \in \{0, << Z_L\}$	
Stability: Unconditional $\Rightarrow \lvert A_{VR} \cdot A_{VF} \rvert < 1$	
$\lvert A_{VF} \rvert > 1$	
$\lvert A_{VR} \rvert << 1$	

Tab.4: LNA functional requirements, useful two-port and related constraints for: $Z_S=R_{50\Omega}$ and $Z_L \in \{R_L, 1/SC_L\}$(* indicates AD=BC).

3 The results

Wide-band LNA topologies are now generated using the two-port transmission parameter requirements summarised in Tab.4. Starting from an initial set of 145 2VCCS graphs, 4 LNAs have been generated according to Tab.5 (No AC 2VCCS topology is available and all the ACD topologies have |A|=1). The main functional properties of the selected LNA topologies are shown in Tab.6.

TWO-PORT	2VCCS GRAPHS	$\lvert A_{VF} \rvert > 1$	$\lvert A_{VR} \rvert << 1$	STABLE
AC	0	-	-	-
ACD	9	0	-	-
ABC	3	1	1	**1**
ABCD	7	3	3*	**3***

Tab.5: 2VCCS LNAs Generation (* 2 AD=BC cases).

2VCCS TOPOLOGY	TRANSMISSION PARAMETERS				$Z_{IN,V}$
	A	B	C	D	
LNA1	g_a/g_b	$1/g_b$	g_a	0	$1/g_b$
LNA2	g_a/g_b	$1/g_b$	g_a	1	$1/g_b$
LNA3	$g_a/(g_a+g_b)$	$1/(g_a+g_b)$	$g_ag_b/(g_a+g_b)$	$g_b/(g_a+g_b)$	$1/g_b$
LNA4	$g_a/(g_a-g_b)$	$1/(g_a-g_b)$	$g_ag_b/(g_a-g_b)$	$g_a/(g_a-g_b)$	$1/g_b$

Tab.6: {A,B,C,D} parameters and $Z_{IN,V}$ for the 4 selected 2VCCS LNAs.

3.1 The MOS transistor implementation

The 4 LNA topologies are implemented at transistor level according to the following guidelines:

- *VCCS circuits.* The simplest implementation is preferred: a linear resistor (i.e. does not require biasing and is less noisy than a MOST) and a nMOS transistor respectively for a diode connected and a "3" terminal VCCS.
- *Bias current re-use*. Circuit implementations are arranged in such a way to allow MOS transistors to share the same bias current source. This can be effective to reduce the power consumption.

Fig.5 shows graph, VCCS and nMOST description for the 4 selected LNAs. Next to 2 well-known circuits such as the CG-stage (⇒LNA2) and SSFCS-stage (⇒LNA4), 2 alternative LNA circuits are found: LNA1 and LNA3. The latter, as far as the authors are aware, are novel LNA topologies.

4 LNA Topologies comparison

Two fundamental aspects of the LNA performance are analysed: (thermal)noise and intermodulation distortion. To gain insight about the operation of the LNA topologies, proper simple VCCS symbolic macro-models are used. The ongoing analysis assumes these reference conditions:

1. Voltage sensing load: $Z_{OUT} << Z_L$.
2. Input source matching: $Z_{IN}=R_{50\Omega}$.
3. Fixed minimum LNA power $P_{LNA,min}$.

The LNA power consumption is:

$$P_{LNA} = V_{DD} \cdot I_{VCCS,b} = V_{DD} \cdot \left(\frac{I_{VCCS,b}}{g_b} \right) \cdot g_b \qquad (4)$$

A simple $VCCS_i$ large signal model is ($i \in \{a, b\}$):

$$I_{VCCS,i} = \frac{K_i}{1 + q_i \cdot V_{eff,i}} \cdot V_{eff,i}^2 \qquad (5)$$

while the current $VCCS_i$ efficiency is:

$$\frac{g_i}{I_{VCCS,i}} = c_i \cdot \frac{2}{V_{eff,i}} \cdot \frac{1 + 0.5 \cdot q \cdot V_{eff,i}}{1 + q \cdot V_{eff,i}} \qquad (6)$$

where, $V_{eff,i} = V_i - V_{T0}$ is the effective input voltage, $\chi_i \in \{1, 1+\delta\}$ is a parameter depending on the VCCS implementation, θ_i models the saturation of the $VCCS_i$ transconductance for increasing values of $V_{eff,i}$ and δ MOS transistor's slope factor that is defined as ratio between beck-gate and gate transconductances. Realising that g_b is constrained to be $1/R_{50\Omega}$ for input matching reasons, equation (4) can be rewritten as:

$$P_{LNA} = \frac{V_{DD} \cdot V_{eff,b}}{2 \cdot R_{50W} \cdot c_b} \cdot \frac{1 + q \cdot V_{eff,b}}{1 + q \cdot \frac{V_{eff,b}}{2}} \qquad (7)$$

Equation (7) says that power consumption of *all* 4 the LNA topologies solely depends on the effective voltage $V_{eff,b}$ –assuming $R_{50\Omega}$, V_{DD} and θ_i fixed. For V_{DD} =3.3V, θ=0.7V^{-1}, χ_b=1 and $V_{eff,b} \cong$0.25V for instance, a minimum power $P_{LNA,min}$ = 7mW is obtained.

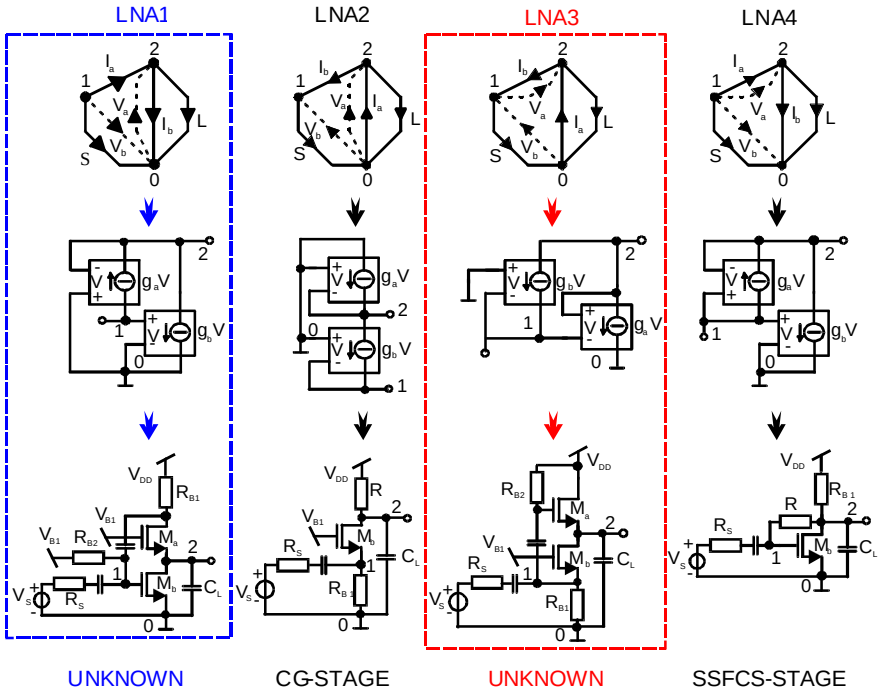

Fig.5: Graph, VCCS and nMOST representation of the 4 selected 2VCCS LNAs.

TOPOLOGY	NOISE FACTOR FOR $Z_{IN,V}=R_{50\Omega}$
LNA1	$1+NEF_b+4NEF_a/A_{VF,V}$
LNA2	$1+NEF_b+4NEF_a/A_{VF,V}$
LNA3	$1+NEF+4\Delta NEF(A_{VF,V}-1)/A_{VF,V}^2$
LNA4	$1+NEF_b(1-1/A_{VF,V})^2+4NEFa(1-1/A_{VF,V})^2/(1-A_{VF,V})$

Tab.7: Expressions for LNAs Noise factor.

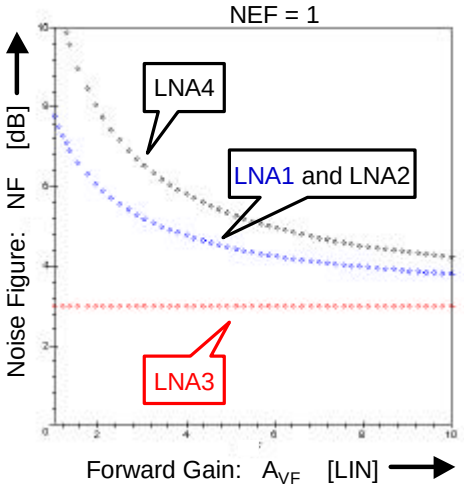

Fig. 6: LNA Noise figure $F_{dB}=10Log_{10}(F)$.

4.2 Noise figure

The noise properties of the 4 LNA topologies are analysed applying the following procedure:

1. A noisy VCCS is modelled adding an *independent* noise current source $I_{n,gi}=(4KT\cdot NEF_i\cdot g_i\cdot\Delta f)^{1/2}$ in parallel at the output of the VCCS.
2. The LNA noise factor F is calculated as [4]:

$$F=1+\frac{\sum_i \overline{\left(V_{n,eq,i}+R_{50W}\cdot I_{n,eq,i}\right)^2}}{4KTR_{50W}Df} \qquad (9)$$

where $V_{n,eq,I}$ and $I_{n,eq,i}$ are the two-port input-referred equivalent noise sources.

The result of this procedure is shown in Tab.7. It can be seen that the noise factor of all the LNAs exhibit the same bottom limit 1+NEF due to the input matching requirement. Nevertheless, there are differences in the way the 4 LNAs approach this limit. In Fig.6 the noise figure F_{dB} is plotted versus the gain $A_{VF,V}$ (=A_{VF} for $Z_{OUT}<<Z_L$) for NEF=1. Topologies LNA1 and LNA2 basically provide the same noise behaviour. Topology LNA3 indeed exhibits a more interesting feature*: the lowest and gain-independent noise figure*. This property is useful in wireless applications where variable gain is required but noise figure degradations at low gains are to be avoided [7].

4.3 Intermodulation distortion.

The intermodulation properties of the 4 LNAs are described in terms of Input referred Intercept Points –IIPs. Depending on the receiver architecture, both 2nd and 3rd order IIP_s -IIP2 and IIP3- are useful [4]. The latter are calculated applying the following procedure:

1. The $VCCS_i$ large signal model is approximated by a third order series:

$$DI_{VCCS,i}\cong g_{i,1}\cdot DV_{eff,i}+g_{i,2}\cdot DV_{eff,i}^2+g_{i,3}\cdot DV_{eff,ii}^3 \qquad (10)$$

2. The input/output Taylor's coefficient g_1, g_2 and g_3 are determined by inspection circuit topology.

3. Intercept points IIP2 and IIP3 are calculated according to the following formulas:

$$V_{IIP\,2} = \left|\frac{g_1}{g_2}\right| \quad \Rightarrow \quad IIP\,2 = \frac{V_{IIP\,2}^2}{2 \cdot R_{50\,W}}$$
$$V_{IIP\,3} = \sqrt{\frac{4}{3} \cdot \left|\frac{g_1}{g_3}\right|} \quad \Rightarrow \quad IIP\,3 = \frac{V_{IIP\,3}^2}{2 \cdot R_{50\,W}} \qquad (11)$$

The resulting IIP2 and IIP3 are plotted versus the forward gain $A_{VF,V}$ Fig.7. LNA2 and LNA4 exhibit IIP2 and IIP3 independent on the forward gain. They can be increased only with a larger input $V_{eff,b}$, which in turn increases the power consumption (7). In contrast, LNA1 and LNA3 exhibit IIPs that do depend on the gain. LNA3 exhibits the largest IIP2 > 18dBm over the whole gain range and IIP2 = ∞ for $A_{VF,V}$ = 6. LNA1 indeed exhibits rather good value of IIP3 > 9 dBm with IIP3 = ∞ for $A_{VF,V}$ = 3 .

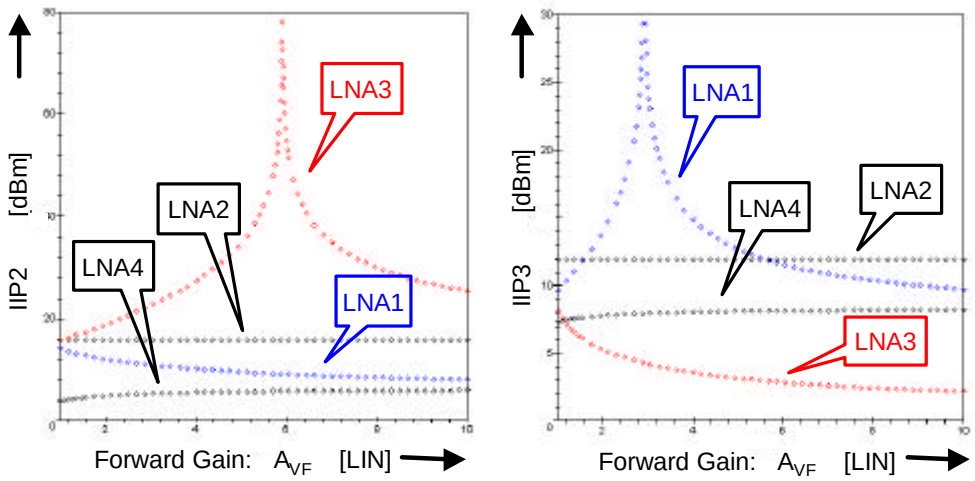

Fig.7: $IIP2_{dBm}$ and $IIP3_{dBm}$ versus the forward gain $A_{VF,V}$ upon min $P_{LNA,min}$.

5 Conclusions

A top-down methodology that systematically generates at transistor level *all* the wide band LNA topologies with 2 VCCS suitable for highly integrated transceivers has been presented. Next to well-known circuits (CG-stage and shunt series feedback CS-stage), two alternative LNA topologies – LNA1 and LNA3- have been found. These topologies, as far the authors are aware, have not previously been reported in literature. A preliminary analysis of the LNA performance based on hand calculations indicate these topologies to have promising noise and intermodulation properties. The methodology can be applied to generate LNA topologies that could be used for other applications (e.g. the SKA project).

6 References

[1] E.A.M. Klumperink, “Transconductance based CMOS circuits: Circuit Generation, Classification and analysis”, Ph.D. Thesis, University of Twente the Netherlands, 1997.
[2] E.A.M. Klumperink, A. J. M. v. Tuijl, "Systematic Generation of Transconductance based Variable Gain Amplifier Topologies", The 1998 International Symposium on Circuits and Systems, May 31-June 3, Monterey, USA, CD-ROM Paper TAA8-3, 1998.
[3] J.C. Rudell, J.J. Ou, R. S. Narayanaswami, G. Chien, J.A. Weldon, L. Lin, K.C. Tsai, L. Tee, K. Khoo, D. Au, T. Robinson, D. Gerna, M. Otsuka, and P. R. Gray, “Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems ”, 1998 International Symposium on Low-Power Electronics, Monterey, California.

[4] B. Razavi, “RF Microelectronics” Prentice-Hall Communications Engineering and Emerging Technologies Series, 1997.
[5] G. Gonzalez, “Microwave Transistor Amplifiers” Prentice-Hall, 2nd edition.
[6] M.Ohtomo, “Proviso on the Unconditional Stability Criteria of Linear Two-port” IEEE Trans. On Microwaves Theory and Thechniques, vol. 43, No 5, pp., May 1995.
[7] K.L. Fong, ”Dual-Band High-Linearity Variable-Gain Low-Noise Amplifiers for Wireless Applications”, IEEE ISSCC, digest of tech. paper, pp.224-225, February 16, 1999.