A 10-bit Charge-Redistribution ADC Consuming 1.9 μW at 1 MS/s

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***Abstract*—This paper presents a 10 bit successive approximation ADC in 65 nm CMOS that benefits from technology scaling. It meets extremely low power requirements by using a charge-redistribution DAC that uses step-wise charging, a dynamic two-stage comparator and a delay-line-based controller. The ADC requires no external reference current and uses only one external supply voltage of 1.0 V to 1.3 V. Its supply current is proportional to the sample rate (only dynamic power consumption). The ADC uses a chip area of approximately 115×225 μm^2. At a sample rate of 1 MS/s and a supply voltage of 1.0 V, the 10 bit ADC consumes 1.9 μW and achieves an energy efficiency of 4.4 fJ/conversion-step.**

***Index Terms*—ADC, analog-to-digital converter, asynchronous, charge-redistribution, CMOS, comparators, DAC, digital-to-analog converter, dynamic power dissipation, figure of merit, low noise, low power, low static current, sense amplifiers, sensors, smart dust, step-wise charging, successive approximation, wireless sensor networks, wireless sensors.**

I. Introduction

NANOSCALE CMOS ICs are at the heart of a plethora of networked communication devices, and also play a key role in wireless sensor networks to create a "network of things" [1]. Extremely power-efficient CMOS chips are needed, both for the sensor interfaces and for the radio transceivers. The required low average power is typically only possible via low duty-cycle operation. In general, circuits that only dissipate power when they do something useful are highly wanted, whereas the standby power consumption should be small compared to the (duty-cycled) active power. This paper presents an analog-to-digital converter (ADC) that satisfies the requirements of a very low active power and virtually no standby power consumption.

CMOS feature-size reduction is beneficial for digital circuits, but not necessarily for analog circuits. The key advantages of CMOS downscaling are smaller area, faster transistors and lower digital power consumption. However, feature-size reduction can pose significant disadvantages for many analog circuits. Examples are the reduced voltage headroom related to the reduced breakdown voltage of nanoscale MOS devices, the leaky gates caused by thinner gate oxide and the lower intrinsic voltage gain of a transistor due to its low output resistance. On the positive side, feature-size reduction also results in improved matching and density of some passive components like metal capacitors. Overall there is a trend in literature that feature-size reduction is accompanied by improved ADC energy efficiency [2].

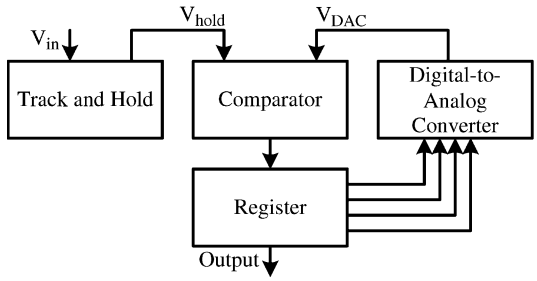

Fig. 1. Block diagram of a successive approximation register analog-to-digital converter (SAR ADC; clock and supply not shown).

This paper describes a successive approximation ADC [3] (Fig. 1) in 65 nm CMOS that uses a charge-redistribution digital-to-analog converter (DAC) designed to achieve a good accuracy, while achieving low power consumption [4]. It exploits the improved matching of metal capacitors in nanoscale CMOS technologies to obtain 10 bit resolution while dissipating little power. Step-wise charging is used to further reduce the power consumption. High/low decisions are made by a low-power dynamic two-stage comparator that does not suffer from the low intrinsic voltage gain of nanoscale transistors. The (successive approximation) register (SAR) contains the well-known Successive Approximation search algorithm. In order to minimize clocking power and to only dissipate energy when performing a conversion, the Register contains a delay-line-based controller. Compared to our earlier publication [4], this paper provides more detailed analysis of the operation and accuracy of the ADC and its building blocks, reflected in several design equations.

Section II discusses using step-wise charging in a charge-redistribution DAC. Section III discusses how the SAR ADC uses the charge-redistribution DAC. Section IV discusses its delay-line-based controller and Section V describes the dynamic two-stage comparator. In Section VI, the overall integration and biasing of the ADC is described. Section VII contains simulation results, Section VIII contains measurement results, and Section IX contains conclusions.

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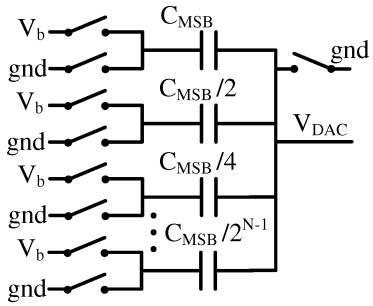

Fig. 2. Charge-redistribution digital-to-analog converter.

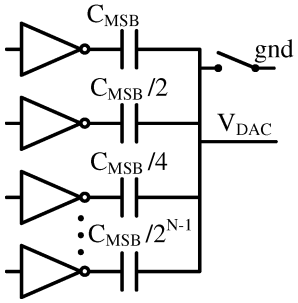

Fig. 3. Charge-redistribution digital-to-analog converter with inverters.

II. Charge-Redistribution DAC With Step-Wise Charging

The operation of the DAC in the SAR ADC presented here is based on capacitive voltage division or charge-redistribution [5]. This section first shows the basic DAC as it is used and next explains how its energy dissipation is reduced by applying step-wise charging.

A. Charge-Redistribution DAC

A charge-redistribution DAC and its application in a SAR ADC are well known from literature [5], [6]. A simplified version of the DAC as it is used in this SAR ADC is shown in Fig. 2. In this SAR ADC the positive supply voltage V_b is directly used as a reference voltage and a pair of switches is implemented as a digital inverter, as shown in Fig. 3. The DAC is not fully binary weighted but uses a split-capacitor array for better efficiency [6].

Limiting factors to the accuracy of the DAC are sampled noise and nonlinearity due to mismatch. The minimum capacitance value to reduce nonlinearity due to mismatch to a certain level depends on the matching properties of capacitors, which is good in nanometer-scale CMOS. In this design mismatch is dominant oversampled noise and a total DAC capacitance of 500 fF is used.

B. Application of Step-Wise Charging

Every DAC dissipates energy both in its digital part and in its analog part. Often the dissipation in the analog part is dominant. In a charge-redistribution DAC the dissipation in the analog part is related to the charging and discharging of capacitors. If ideal switches are used to fully charge C_MSB from gnd to V_b and fully discharge it again, the total energy dissipation is

$$E_\mathrm{DAC} = C_\mathrm{MSB} \cdot V_b^2 [J]. \tag{1}$$

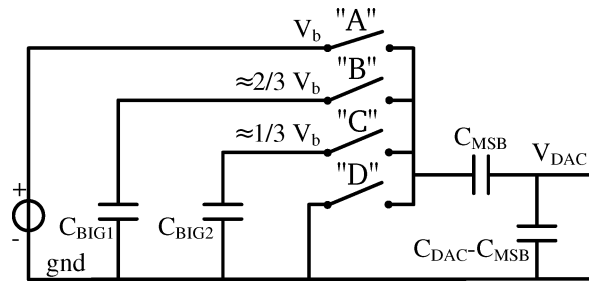

Fig. 4. Detail of step-wise charging in the charge-redistribution DAC.

Step-wise charging with one or multiple intermediate steps in between gnd and V_b can be used to reduce this energy dissipation. In literature a method specifically for a charge-redistribution DAC in a SAR ADC has been explored with one intermediate step [6]. This method is less efficient than a split-capacitor array and cannot be combined with a split-capacitor array [6].

In a different context, a method for step-wise charging has been proposed, using multiple intermediate steps [7]. When overhead is not taken into account, step-wise charging in S equidistant steps reduces the energy dissipation by a factor S [7]:

$$E_\mathrm{DAC,step-wise} = \frac{C_\mathrm{MSB} \cdot V_b^2}{S} [J]. \tag{2}$$

We propose to use this method in a charge distribution DAC (with a split-capacitor array) and store intermediate voltages on big auxiliary capacitors, which are not used in [6]. Such step-wise charging with auxiliary capacitors has been proposed to lower the energy-dissipation of a flash DAC that is driving a capacitive load. However, the flash DAC requires all intermediate voltages to be accurate and requires additional low-impedance voltage reference sources to achieve that [8]. In our SAR ADC step-wise charging with auxiliary capacitors is applied in such a way that there is no strong requirement on the accuracy of the intermediate voltages. Fig. 4 shows how this is done for the most significant bit (MSB) divider branch with C_MSB in the DAC.

Fig. 4 shows how a capacitive divider can be charged to V_b and discharged to gnd with two intermediate extra steps. When the left plate of C_MSB is discharged from V_b to gnd, the two intermediate steps are used. Assume the two "big" capacitors C_BIG1 and C_BIG2 have an initial voltage approximately equal to 2/3 V_b and 1/3 V_b respectively. First only switch "B" is closed to discharge into C_BIG1, then only switch "C" to discharge into C_BIG2 and finally only switch "D" to discharge to gnd. This way charge is stored on C_BIG1 and C_BIG2 for re-use during charging. When the left plate of C_MSB is charged from gnd to V_b the two intermediate steps are used to reuse the charge stored during discharge by first closing only switch "C" and then "B" and finally "A". This way, a significant part of the charge that is required to charge the left plate of C_MSB is delivered by C_BIG2 and C_BIG1 instead of by the supply. When C_BIG1 and C_BIG2 are used repeatedly to help charge and discharge the DAC capacitors the voltages on C_BIG1 and C_BIG2 will converge indeed towards the values indicated in Fig. 4 [7].

Switches "A" and "B" in Fig. 4 are implemented as pMOS transistors and switches "C" and "D" are implemented as nMOS

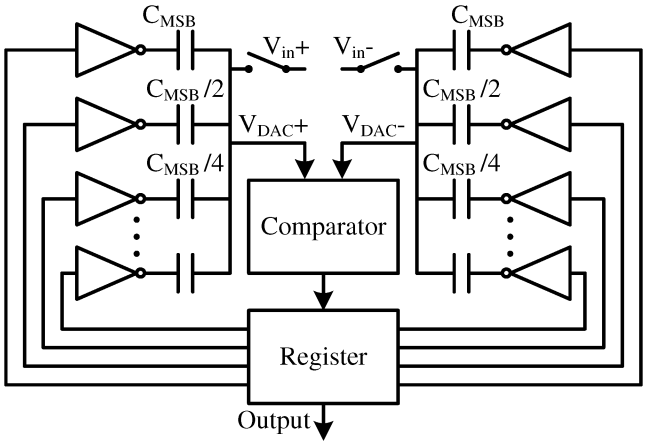

Fig. 5. Semi-differential charge-redistribution ADC realized on chip.

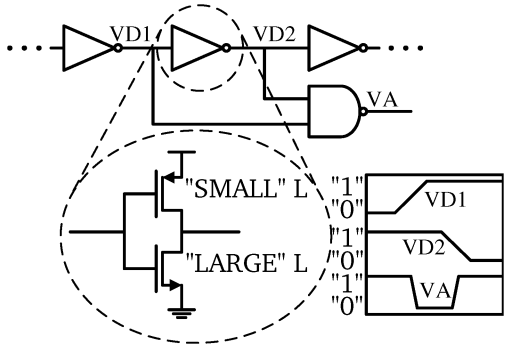

Fig. 6. Detail of delay-line-based controller.

transistors. The accuracy with which the voltages on C_{BIG1} and C_{BIG2} converge towards their ideal values is limited by leakage currents and imperfect settling during the intermediate steps. The impact of small inaccuracies in the voltages at C_{BIG1} and C_{BIG2} on the energy-saving is small.

During an intermediate step the output voltage V_{DAC} also has an intermediate value. This intermediate value is not very accurate because the voltages on C_{BIG1} and C_{BIG2} are not very accurately known. When the left plate of C_{MSB} has been fully charged or discharged to the accurate reference voltage V_{b} or gnd then V_{DAC} is accurate again. This is because it is a property of charge-redistribution that the intermediate voltage values are not relevant for the end result. In this step-wise charging charge-redistribution DAC the intermediate steps are only used to lower the energy dissipation and not to increase the resolution. This means that the comparator in the SAR ADC only samples V_{DAC} when either switch "A" or switch "D" has been closed long enough for V_{DAC} to settle. This is unlike the flash DAC of [8] that requires additional low-impedance voltage reference sources for the intermediate voltages, which all need to be accurate.

There is always overhead in the digital part of the DAC and more overhead is added when more intermediate steps are used. Therefore, the energy dissipation of the DAC cannot be reduced to an arbitrarily low level. In the charge-redistribution DAC for this ADC the three most significant bits are charged with two intermediate steps, like in Fig. 4. Feature-size reduction as a result of technology scaling reduces the overhead losses because of the smaller parasitic capacitances, and therefore feature-size reduction is beneficial for this DAC.

III. Integration of Charge-Redistribution DAC Into the SAR ADC

Fig. 5 shows how a semi-differential charge-redistribution DAC has been integrated into this SAR ADC (see also Fig. 1). A track-and-hold (T/H) circuit is implemented as a switch, followed by a hold capacitor. Combining the hold function with the output capacitance of a charge-redistribution DAC offers the opportunity to implement a simple semi-differential version of a charge-redistribution ADC. The switches are bootstrapped nMOS transistors [9] and sample the differential input voltage V_{in} onto the output of the DAC. During the conversion, the SAR algorithm controls V_{DAC} from V_{in} towards zero. This makes the ADC sensitive to parasitic (nonlinear) capacitances at the DAC output. In literature, the input voltage is usually sampled at the other side of the capacitors while keeping the output of the DAC at a fixed voltage [5]. This method is not sensitive to (nonlinear) capacitances at the DAC output [5], at the expense of a switching scheme that is more complex and requires more energy.

The nominal supply voltage V_{b} of this 10 bit SAR ADC is 1 V. This means that the peak-to-peak input voltage range is approximately 2 V and the value of an LSB is approximately 2 mV.

IV. Delay-Line-Based Controller

A SAR ADC often requires an external control clock at a multitude of the sample rate because the successive approximation algorithm operates at a multitude of the sample clock as well. This requirement facilitates the ADC implementation but can make its integration more difficult because such a fast external control clock is not always readily available in for example a wireless sensor node. Making it available can well require more power than the ADC itself in ultra-low-power applications. This ADC does not require such a fast external control clock and instead contains a delay-line-based controller that is tightly integrated with the SAR. The controller consists of an inverter-based delay line with logic gates connected to taps of the delay line in such a way that sequentially the required pulses for the SAR algorithm are generated. A representative detail is shown in Fig. 6.

The delay line uses a string of inverters that alternately delays a rising or falling edge, generated by a PMOST or NMOST, respectively. Therefore, alternately the PMOST or the NMOST has a large L and all devices have a minimum W. When the ADC is ready for the next conversion voltage VD1 in Fig. 6 is low and VD2 is high. Initiated by the external sample clock after a certain delay VD1 rises and becomes high. This triggers VA to become low (active low), which triggers a part of the SAR algorithm. When VD1 is high the PMOST in the inverter does not conduct and the conduction of the NMOST is kept small by its large L. The parasitic capacitance at node VD2 is slowly discharged and VD2 becomes low. This in turn makes VA inactive (high) again. In the next inverter the PMOST has a large L and the NMOST has a small L because it only needs to delay its rising edge starting from the falling edge of VD2.

The last section of the controller generates an external "ready" signal, indicating that the digital output is valid and the ADC is ready for a next conversion. When the external sample clock puts the T/H back into tracking mode the controller is reset to its ready state as well.

The actual delay of an element in the delay line is not accurate. There is a large dependency on process variations, mismatch, temperature, and noise. However, this does not need to affect the accuracy of the ADC because both the charge-redistribution DAC and the comparator rely on settling. The delay-line is simply dimensioned such that the guaranteed minimum delay is sufficient for settling. This way the controller determines the maximum sample rate of the ADC, which is significantly slower than the minimum time needed by the DAC and the comparator.

Both the inverters in the delay line and the logic gates over the inverters use transistors with high threshold voltages. Still, when the input voltage is near half the supply voltage, PMOST and NMOST devices within a cell are somewhat conducting at the same time. Because of the inherently slow transitions, cross-conduction currents dominate the total active supply current of the controller. When the ADC is not active there is virtually no current in the string of inverters, which means that there is virtually no quiescent power dissipation in the control of the ADC.

For a low-power ADC optimum power scaling of the delay line can be expressed as obtaining as much guaranteed delay per energy as possible. The on-resistance of a transistor responsible for delay should be high. In addition to the long L this can be achieved by a high threshold voltage, a low supply voltage and a small W. In a full ADC with only one supply voltage, this single supply voltage influences both the time that the various building blocks need to settle and the delay in the controller. In this ADC, a nominal supply voltage of 1 V has been chosen as a compromise. The smallest W that is available improves with smaller technology nodes.

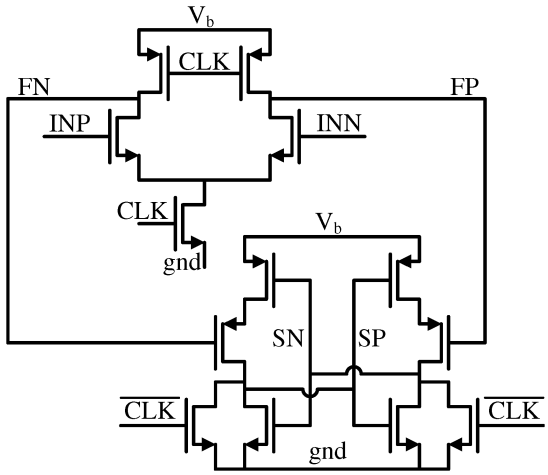

Fig. 7. Energy-efficient dynamic two-stage comparator.

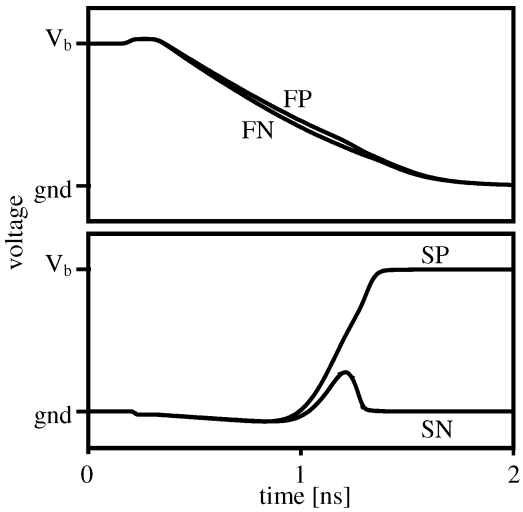

Fig. 8. Simulated comparator node voltages during a comparison.

V. Dynamic Two-Stage Comparator

An energy-efficient SAR ADC relies heavily on an energy-efficient comparator. This ADC uses a dynamic two-stage design. First, the overall operation of the comparator and its efficiency are discussed. Next, the input-equivalent noise of the first stage is derived.

A. Operation

The comparator is shown in Fig. 7. It has some similarities with the comparator in [10], which is focused on speed rather than energy efficiency.

The first stage is a voltage amplification stage with INP and INN as differential input and FP and FN as differential output. The second stage contains both a simple voltage amplifier and a positive-feedback amplifier to obtain the rail-to-rail digital output SP and SN. To illustrate the functionality, Fig. 8 contains a simulated comparison action. Prior to the comparison, the nodes have been pre-charged by a low clock voltage to the situation shown during the first 100 ps. A rising clock edge stops the pre-charging state and starts the amplification in the first stage. In the first stage, the differential output voltage increases while the common-mode output voltage decreases towards gnd. When the common-mode voltage approximates the threshold voltage of the input pair of the second stage, the voltage amplification in the second stage takes over. In the second stage, the differential output voltage increases while the common-mode output voltage increases. As the common-mode output voltage increases gradually the positive-feedback mechanism takes over and provides the rail-to-rail output.

The power dissipation in the first stage stops when its (parasitic) capacitances have been fully discharged. The power dissipation in the second stage stops when the positive-feedback amplifier has settled. When the clock signal becomes low again, all (parasitic) capacitances are pre-charged to their original values. Therefore, this comparator has virtually no power dissipation when the comparator is not active.

Especially during a critical comparison with small differential input signal, the positive-feedback amplifier in the second stage needs to provide a large gain for the required rail-to-rail output. To obtain this output within a reasonable time, it is helpful that the relevant devices are biased in strong inversion. This strong inversion is one reason that the positive-feedback amplifier is not energy efficient by itself. Another reason is that its noise

performance is relatively constant during the amplification period, while the best noise performance is only required when the overall voltage gain is still low.

The first stage of the two-stage comparator serves to improve the energy efficiency of the comparator. According to simulation, the (differential) voltage gain of the first stage at the moment the second stage takes over is approximately 5. This is a suitable gain because it both significantly reduces the input-equivalent noise of the second stage and it is a feasible gain for an energy-efficient amplifier. The factor of 5 in input-equivalent noise voltage corresponds to a factor of 25 in power and therefore the power dissipation in the second stage can be (up to) a factor 25 lower than without the first stage. The voltage amplification of 5 is also below the intrinsic voltage gain of a short-channel CMOS transistor and therefore no energy-inefficient measures to achieve a high gain are required. The first stage of the comparator can benefit from weak inversion operation of the input transistors to achieve a low equivalent input noise.

B. Equivalent Input Noise of the First Stage

Because of the significant voltage amplification in the first stage, the noise and therefore the energy efficiency of the comparator depends largely on the first stage. The dominant noise source in the first stage is its input pair. The thermal noise of a single MOS transistor can be estimated with an equivalent noise resistor $R_{\mathrm{n,MOST}}$ at its gate:

$$R_{n,MOST} \approx \frac{\gamma}{gm_{\mathrm{MOST}}} \tag{3}$$

where the noise excess factor γ is close to 1. The equivalent noise resistor of each input transistor appears in series with the DAC voltage. The equivalent noise resistor of the input pair $R_{\mathrm{n,FS}}$ is approximately

$$R_{n,FS} \approx \frac{2}{gm_{\mathrm{MOST}}}. \tag{4}$$

The first stage of the comparator simultaneously integrates the input signal and the noise from the equivalent noise resistor. The input-equivalent integrated noise can be estimated by

$$\sigma_{\mathrm{v}} \approx \sqrt{4 \cdot k \cdot T \cdot R_{n,FS} \cdot \mathrm{NBW}} \approx \sqrt{4 \cdot k \cdot T \cdot \frac{2}{gm_{\mathrm{MOST}}} \cdot \mathrm{NBW}}. \tag{5}$$

The noise bandwidth (NBW) for noise integrated over integration time T_{int} is

$$\mathrm{NBW} = \frac{1}{2 \cdot T_{\mathrm{int}}}. \tag{6}$$

A short derivation of this expression can, for example, be found in the Appendix of [11]. A more general discussion of NBW in amplifiers can be found in [12]. Integration is discussed as a special case (in the form of an amplifier that has not settled yet) and results in the same expression.

The second stage samples the output voltage of the first stage when the common mode voltage on nodes FP and FN has changed by approximately the threshold voltage of its input pair $V_{\mathrm{threshold}}$. The current through each input transistor in the first stage I_{MOST} is integrated on the (parasitic) capacitances C_{FP} and C_{FN} at nodes FP and FN. The integration time T_{int} can be approximated by

$$T_{\mathrm{int}} \approx \frac{V_{\mathrm{threshold}} \cdot C_{\mathrm{FP}}}{I_{\mathrm{MOST}}} \approx \frac{V_{\mathrm{threshold}} \cdot C_{\mathrm{FN}}}{I_{\mathrm{MOST}}}. \tag{7}$$

Inserting (6) and (7) into (5) gives

$$\sigma_{\mathrm{v}} \approx \sqrt{4 \cdot k \cdot T \cdot \frac{1}{V_{\mathrm{threshold}} \cdot C_{\mathrm{FP}}} \cdot \frac{I_{\mathrm{MOST}}}{gm_{\mathrm{MOST}}}}. \tag{8}$$

For an energy-efficient amplification, the input pair is biased in weak inversion. The transconductance of a MOS transistor in weak inversion depends on the subthreshold slope. According to simulations for the 65 nm process that was used the transconductance can be approximated by

$$gm_{\mathrm{MOST}} \approx \frac{I_{\mathrm{MOST}}}{2 \cdot V_{\mathrm{thermal}}} \tag{9}$$

where V_{thermal} is

$$V_{\mathrm{thermal}} = \frac{k \cdot T}{q}. \tag{10}$$

In a SAR ADC based on a charge-redistribution DAC, the thermal noise from the DAC switches sampled by the comparator can potentially also be significant. The equivalent noise resistor of the DAC $R_{\mathrm{n,DAC}}$ is determined by the on-resistances of the switches. The first stage of the comparator is relatively slow because it is biased in weak inversion. This makes the NBW relatively small and at the same time its equivalent noise resistor $R_{\mathrm{n,FS}}$ relatively large, therefore

$$R_{\mathrm{n,FS}} \gg R_{\mathrm{n,DAC}}. \tag{11}$$

As a consequence $R_{\mathrm{n,DAC}}$ contributes relatively little noise.

Inserting (9) into (8) gives

$$\sigma_{\mathrm{v}} \approx \sqrt{\frac{k \cdot T}{C_{\mathrm{FP}}}} \cdot \sqrt{8 \cdot \frac{V_{\mathrm{thermal}}}{V_{\mathrm{threshold}}}}. \tag{12}$$

For example at $T = 300$ K with $C_{\mathrm{FP}} = 10$ fF and $V_{\mathrm{threshold}} = 0.4$ V, the value for σ_{v} is approximately 0.5 mV. Based on a desired maximum noise level, the required minimum value of C_{FP} and C_{FN} can be approximated by

$$C_{\mathrm{FP}} = C_{\mathrm{FN}} \geq \frac{k \cdot T}{\sigma_{\mathrm{v}}^2} \cdot 8 \cdot \frac{V_{\mathrm{thermal}}}{V_{\mathrm{threshold}}}. \tag{13}$$

A level of 0.5 mV is suitable because it puts the thermal noise of the comparator in the same order as the quantization noise of this ADC. In this comparator C_{FP} and C_{FN} mostly consist of parasitic MOST capacitances and are somewhat larger than 10 fF each. The energy dissipation of the first stage depends mostly on C_{FP} and C_{FN} being discharged and charged for every comparison (1). According to simulation at a supply voltage V_{b} of 1.0 V the average energy per comparison of this comparator is approximately 60 fJ.

VI. Integration and Biasing

All ADC building blocks share one common supply voltage V_{b} of 1.0 V to 1.2 V which also serves as the reference for the DAC. For the accuracy of the ADC it is important that V_{b} is

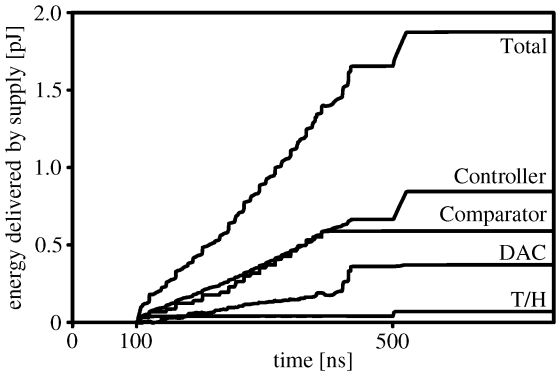

Fig. 9. Simulated energy delivered by the 1 V supply voltage source during one conversion: about 1.9 pJ is needed for a complete 10 bit conversion; ADC operation starts at 100 ns.

accurate during sampling and during the start of each comparison. Immediately prior to and during these critical moments the ADC draws very little supply current and does therefore hardly deteriorate $V_{\rm b}$. If $V_{\rm b}$ is shared with other components outside of the ADC it is important that these do not deteriorate $V_{\rm b}$ either. In a low-power environment this can be under control. The ADC does not use any (external) bias current.

VII. Simulation Results

Simulations have been performed to qualitatively verify the operation of the ADC and to quantitatively estimate its energy dissipation. The example in Fig. 9 is obtained from a transient simulation over one conversion with an active edge of the sample clock after 100 ns and a reset edge after 500 ns. The figure contains the simulated cumulative energy delivered by the 1 V supply voltage to the various parts of the ADC.

The actual conversion happens between approximately 100 ns and 400 ns and the power consumption is relatively constant during this time. In fact more energy is used for the first bits, but because of the step-wise charging also more time is used. When the conversion has finished after approximately 400 ns step-wise charging is used to reset the DAC to its initial state.

During the conversion, the active current of the (delay-line-based) controller is dominated by cross-conduction currents because of the slow transitions. The controller is reset to its initial state after the reset edge at 500 ns. The reset transitions are much faster than the transitions during the conversion and the active current is dominated by parasitic capacitances instead. A significant amount of the total energy is delivered to the controller. It can be concluded that for a low-power ADC it is important to use a very simple power-efficient controller.

A relatively small amount of the total energy is delivered to the DAC. When step-wise charging would not have been applied the energy delivered to this 10 bit DAC would still be relatively small because the total DAC capacitance is only 500 fF. Therefore, in this ADC step-wise charging only results in a small improvement in the overall energy efficiency. An ADC with a higher resolution would need a larger DAC capacitance. In such an ADC, a larger part of the total energy would be delivered to the DAC and step-wise charging would result in a larger improvement in the overall energy efficiency.

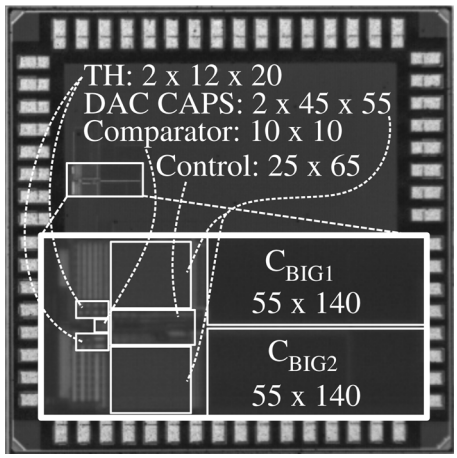

Fig. 10. Die micrograph of the 65 nm CMOS test chip, dimensions in μm^2. The ADC itself measures approximately 115×225 μm^2.

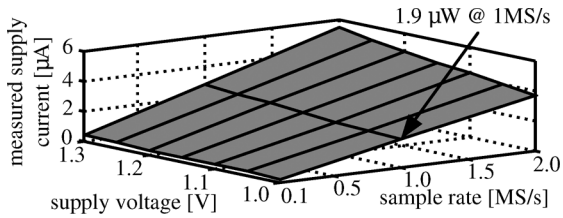

Fig. 11. Measured supply current as a function of supply voltage and sample rate.

It can be seen that a certain time after each edge of the sample clock, the ADC is not active and virtually no additional energy is delivered until the next edge. The total energy delivered during one conversion is approximately 1.9 pJ. As in any circuit that contains energy-storing elements the moment that energy is delivered by the supply voltage source is not necessarily the moment that it is dissipated. A part is initially stored in capacitors and dissipated later.

VIII. Measurement Results

A. Die Micrograph

Fig. 10 shows the test chip that has been manufactured in a low-power 65 nm CMOS process. The chip size including bondpads is approximately 1.4×1.4 mm^2 while the ADC itself including the "big" capacitors is only approximately 115×225 μm^2. Various parts of the ADC are indicated in the zoomed box. It can be seen that the "big" capacitors that are used for the step-wise charging use a significant part of the area. Reducing the size of the capacitors optimizes the circuit more towards area and less towards energy efficiency.

B. Supply Current and Sample Rate

Fig. 11 shows the supply current which has been measured as a function of supply voltage and sample rate. At a constant supply voltage the current is proportional to the sample rate, which indicates that the energy dissipation per conversion does not depend on sample rate and that there is virtually no quiescent current. The measured total supply current at 1 V and 1 MS/s of

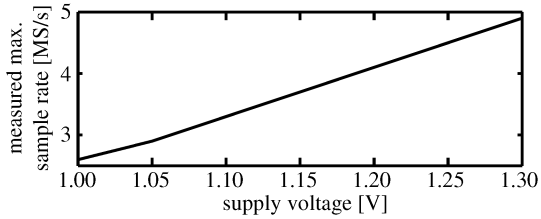

Fig. 12. Maximum sample rate as a function of supply voltage measured in steps of 50 mV.

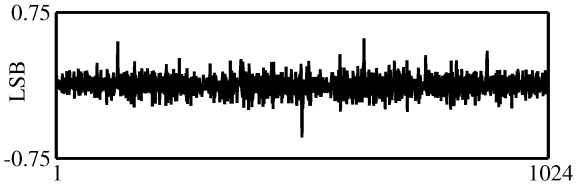

Fig. 13. DNL measured over the input range of one of the ADC samples.

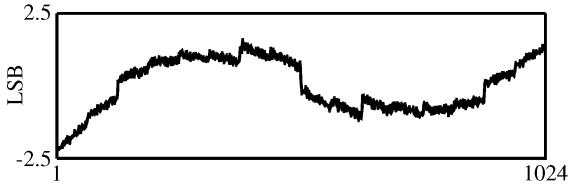

Fig. 14. INL measured over the input range of one of the ADC samples. Unfortunately during design nonlinear capacitances have been underestimated.

1.9 μA indicates a power dissipation of 1.9 μW, which corresponds to the simulated 1.9 pJ/conversion.

The maximum sample rate of this ADC depends on the delay in the controller, which depends on the supply voltage. The intended supply voltage range is 1.0 V to 1.2 V, although measurements indicate that at 1.3 V the ADC is still functional. As can be seen in Fig. 9, more time is required after the active edge than after the reset edge and therefore the maximum sample rate has been measured with a duty cycle of the sample clock of 20%. Fig. 12 shows the measured maximum sample rate as a function of supply voltage. At 1 V supply voltage the measured sample rate is in line with what can be expected based on the simulation result in Fig. 9. The relatively large increase from 2.6 MS/s at 1.0 V to 4.9 MS/s at 1.3 V is because transistors with a high threshold voltage have been used in the delay line.

C. Accuracy

Accuracy measurements have been performed with a supply voltage of 1.0 V, a sample rate fs of 1 MS/s and an input sine wave with a frequency of 499968.75 Hz. Fig. 13 shows the measured DNL. A well-known artifact of a binary-weighted DAC is a high DNL at transitions that involve one of the more significant bits. These are clearly visible in Fig. 13. The same binary-weighted artifacts that are present in the DNL are also present in the INL, as visible in Fig. 14.

In the INL also a third-order nonlinearity is visible, which is similar for all samples. This is attributed to nonlinear parasitic capacitances on node $\mathrm{V_{DAC}}$ which have been underestimated during the design. These nonlinear capacitances include the parasitics to substrate and the comparator. When the resolution of an ADC is increased or decreased, these parasitic capacitances scale at roughly the same rate as the DAC capacitance and therefore the absolute amount of nonlinearity due to the nonlinear capacitances is roughly independent of resolution. The relative amount of nonlinearity, expressed in LSB, would be more appropriate for an 8 bit ADC than for this 10 bit ADC because in an 8 bit ADC an LSB is four times as large. The sensitivity to (nonlinear) parasitic capacitances has been avoided in [5] at the expense of a switching scheme that is more complex and requires more energy. The switching scheme of [5] would have been more suitable for this 10 bit ADC or for a similar ADC with a higher resolution. Step-wise charging as it is used in this ADC can be combined with the switching scheme of [5].

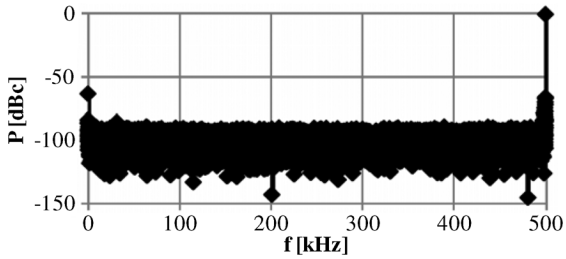

Fig. 15. FFT of the measured ADC output, fin $= 499.96875$ kHz, 16001 bins.

TABLE I
NOMINAL MEASUREMENT CONDITIONS

	Value
Supply voltage	1V
Sample frequency	1MS/s
Input frequency	499968.75Hz
Input amplitude	$1.25\mathrm{V_{pp}}$

Because of the relatively large third-order nonlinearity, the ADC achieves its best accuracy with an input signal of approximately $1.25\mathrm{V_{pp}}$ differential, which is slightly more than half the input range. Under these conditions the ADC does not achieve its maximum SNR but the DAC is more linear. Fig. 15 shows the FFT of the measured ADC output under the measurement conditions in Table I. Because the input frequency is near the Nyquist frequency, all odd harmonics fold to near the Nyquist frequency and all even harmonics fold to near DC. Fig. 16 shows the relevant details of the FFT.

Measurements do not indicate a significant improvement in effective resolution when an input frequency significantly below the Nyquist frequency is used. Therefore, the effective resolution bandwidth $\mathrm{BW_{eff}}$ is $\mathrm{fs}/2$ and the well-known equation for the figure of merit (FOM) simplifies to

$$\mathrm{FOM} = \frac{\mathrm{P}}{2 \cdot \mathrm{BW_{eff}} \cdot 2^{\mathrm{ENOB}}} = \frac{E_{\mathrm{CONVERSION}}}{2^{\mathrm{ENOB}}}. \qquad (14)$$

Table II contains a summary of the performance based on 12 chips, all measured under the conditions in Table I. Fig. 17 shows an overview of FOM achieved by ADCs published at ISSCC and VLSI, based on the data in [13] (includes [14]–[25]). The FOM compares favorably to the FOM of all the ADCs in [13], and is more than twice as low as [15]. The effective number

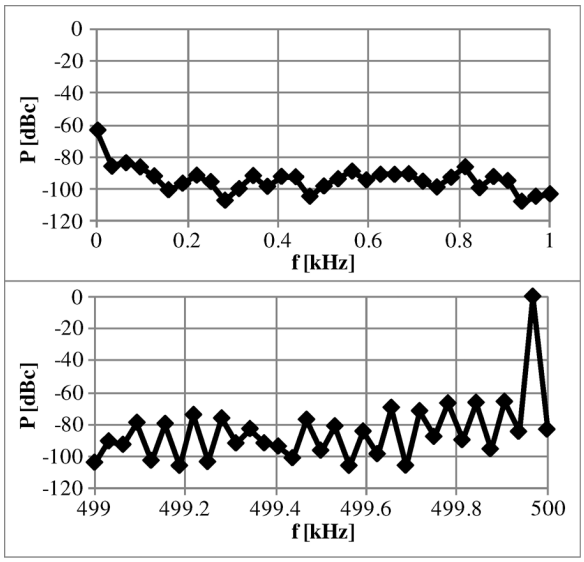

Fig. 16. Details of FFT of the measured ADC output, $f_{in} = 499.96875$ kHz, 16001 bins.

TABLE II
SUMMARY OF PERFORMANCE MEASURED UNDER THE CONDITIONS IN TABLE I

	Average	Standard deviation
SNR [dB]	55.6	0.58
THD [dB]	-61.1	1.95
DNL [LSB]	0.49	0.06
INL [LSB]	2.24	0.18
SNDR [dB]	54.4	0.47
ENOB [bit]	8.75	0.08
I_{supply} [μA]	1.9	
$E_{conversion}$ [pJ / 10-bit conversion]	1.9	
Figure Of Merit [fJ / conversion-step]	4.42	0.24

of bits (ENOB) decreases if the sample rate or the supply voltage is increased. At a supply voltage of 1.3 V and a sample rate of 4.9 MS/s the ENOB is reduced to approximately 8.

IX. CONCLUSION

This paper presents a SAR ADC that has been implemented in 65 nm CMOS for which technology scaling is advantageous. The charge-redistribution DAC of this ADC uses CMOS switches and benefits from improved matching of metal capacitors. A multi-step charging technique is used for the three most significant bits, resulting in power saving in the DAC. The energy efficiency of the delay-line-based controller benefits from the small minimum width of transistors. The dynamic two-stage comparator benefits from reduced parasitic capacitances and requires little intrinsic voltage gain from a transistor. Especially for an ADC with a higher resolution than this 10 bit ADC, step-wise charging can significantly improve the overall energy efficiency. The delay-line-based controller and the dynamic two-stage comparator can be applied to any resolution.

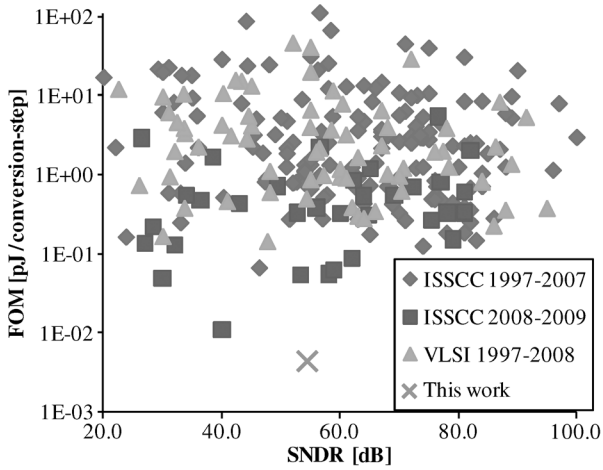

Fig. 17. Comparison of the FOM versus SNDR of ADCs published at ISSCC and VLSI based on the data in [13].

When the ADC is not active there is virtually no power dissipation and when it is active the energy dissipation is only 1.9 pJ/conversion for 8.75 ENOB. This translates into an ADC FOM of 4.4 fJ/conversion-step, which compares favorably to all published ADCs in the overview of [13] (see Fig. 17).

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