23.2 A 2.2GHz 7.6mW Sub-Sampling PLL with –126dBc/Hz In-Band Phase Noise and 0.15ps$_{rms}$ Jitter in 0.18µm CMOS

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A clock with low phase-noise/jitter is a prerequisite for high-performance ADCs, wireline and optical data links and radio transceivers. This paper presents a 2.2GHz clock-generation PLL. It uses a phase-detector/charge-pump (PD/CP) that sub-samples the VCO output with the reference clock. The PLL does not need frequency divider in locked state and achieves a low in-band phase noise values at low power.

In a classical PLL, a VCO is locked to a reference clock *Ref* by a feedback loop with a divider, PD/CP, and loop filter. Both the VCO and the loop components contribute to PLL phase noise, the VCO noise dominating out-of-band and the loop noise in-band. In an optimized PLL, the two types of noise contribute equally to the output jitter [1, 2] and thus, are equally important. This work focuses on the loop noise and presents a technique to reduce it significantly. In most PLLs, the CP and the divider are the main sources of loop noise. The in-band CP noise, when transferred to the PLL output, is suppressed by the feedback gain from the PLL output to the CP output [1,2], denoted as β_{CP}. A larger β_{CP} is preferred as it suppresses more CP noise. In a PLL using a conventional 3-state PFD/CP, the CP feedback gain is: $\beta_{CP,3state}=I_{CP}/(2\pi\cdot N)$, with I_{CP} the CP current and $N=f_{VCO}/f_{Ref}$.

The sampling-based PD was known for its high detection gain [3]. However, drawbacks like difficulty of integration (big filter capacitor) and limited pull-in range have prevented it from being widely used in PLLs [3]. Figure 23.2.1 shows the concept of the sub-sampling PD (SSPD) with a CP added. The key idea is to exploit the high dV/dt of the high-frequency VCO. The sine-wave VCO with amplitude A_{VCO} and DC value V_{DC} is directly sub-sampled by *Ref*, without using divider. The sampler output V_{sam} controls a current $I_{UP}=g_mV_{sam}$, while a reference voltage V_{DC} controls another current $I_{DN}=g_mV_{DC}$. If N is an integer and the VCO and *Ref* are phase aligned, the sub-sampling renders $V_{sam}=V_{DC}$. The CP then outputs no current, and phase locking is achieved. If there are phase errors, they will be converted to voltage changes in V_{sam} around V_{DC}, and then to current changes by the *voltage-controlled* CP. The ideal characteristic of the SSPD/CP has the same shape as the VCO output (see Fig. 23.2.1). In a PLL with this SSPD/CP, the CP feedback gain becomes $\beta_{CP,SSPD}=A_{VCO}\cdot g_m$. Assuming, for simplicity, square-law MOS transistors equations can be used to calculate g_m, then: $\beta_{CP,SSPD}=A_{VCO}\cdot(2I_{CP}/V_{gs,eff})$, where $V_{gs,eff}$ is the effective gate-source voltage of the transistor. Comparing to $\beta_{CP,3state}=I_{CP}/(2\pi\cdot N)$, $\beta_{CP,SSPD}$ can easily be one order of magnitude larger as usually $N>>1$ and $A_{VCO}>V_{gs,eff}$. In other words, *for the same I_{CP}, a PLL using a SSPD/CP has a much larger β_{CP} than a PLL using a 3-state PFD/CP and thus suppresses CP noise more*. Moreover, a PLL using a SSPD/CP does not need a divider in the locked state, which eliminates the noise and power contribution of the divider. As a result, the loop noise is greatly improved, which leads to a PLL design with low in-band phase noise at low power.

In a PLL, the optimal bandwidth for minimum jitter $f_{c,opt}$ is where the spectrum of the VCO and the loop noise intersects [1,2]. For lower loop noise, $f_{c,opt}$ is higher, requiring smaller loop-filter capacitors. Therefore, a larger β_{CP} could also reduce chip area if the CP dominates the loop noise. However, if other loop components start dominating or if $f_{c,opt}$ reaches $f_{Ref}/10$, increasing β_{CP} further can not increase $f_{c,opt}$, but does require a larger filter capacitor to stabilize the PLL. Such "unnecessarily high" β_{CP} will not improve the loop noise but will make full integration difficult. In a PLL using a SSPD/CP, β_{CP} can easily be "unnecessarily high". Therefore, some way of gain control is desired.

Figure 23.2.2 shows the SSPD/CP, now extended with pulse-width control. It uses differential sampling of anti-phase VCO outputs to eliminate the reference voltage V_{DC} and alleviate charge-injection and charge-sharing issues. A block called "pulser" is added. It generates a pulse with a duty ratio of DR_{pul}, which connects or disconnects the current sources from the CP output. In this way, the effective CP output current and thus β_{CP} is reduced by DR_{pul}. By a careful choice of DR_{pul}, the high gain feature of the SSPD/CP can be explored without using unnecessary filter capacitor area. The pulser can be designed to have no overlap with the sampling clock, so that the sampler can simply be a track and hold.

Figure 23.2.3 shows the sub-sampling PLL architecture using the presented SSPD/CP. Since a SSPD has limited pull-in range and may lock to any possible integer multiple of f_{Ref}, a frequency-locked-loop (FLL) is added to ensure correct PLL locking over the entire VCO tuning range. Similar to the classical PLL, the FLL uses a divider and a 3-state PFD/CP, except that a dead-zone creator (DZ) is inserted between the PFD and CP. During locking, the FLL has higher gain than the core loop and overrules it. In the locked state, the phase error between *Ref* and the divider output *Div* is small and falls inside the dead zone. The CP in the FLLoutputs no current. The FLL and the divider then have no influence on the PLL and do not add noise. After locking is achieved, the FLL can be disabled to save power.

In a sub-sampling PLL, where CP noise is greatly suppressed and divider noise is eliminated, the sampling clock noise becomes critical. Figure 23.2.4 shows the schematic of the SSPD/CP. The differential sampler simply consists of two NMOS transistors and two 60fF capacitors. An inverter chain is used to boost the *Ref* sampling-edge steepness. Two source-follower buffers isolate the sampler from the LC VCO. The sampling path is made as short and clean as possible. The SSPD/CP characteristic (sine-shape) is fairly linear, when phase error is small in the locked state. The pulser is implemented with a delay cell and an AND gate, with a 1.5ns pulse width.

The PLL chip is fabricated in a standard 1.8V 0.18µm CMOS process and occupies an active area of 0.4×0.45mm^2 (see Fig. 23.2.7). The IC is tested in a 24-pin LLP package with a 1.8V$_{p\text{-}p}$ 55MHz sine-wave *Ref* from a crystal oscillator. Figure 23.2.5 shows the measured phase noise of the 2.2GHz output from an Agilent E5501B phase-noise-measurement setup. The in-band phase noise at 200kHz offset is –126dBc/Hz. The total phase noise integrated from 10kHz to 40MHz is –56.8 dBc, which translates to an rms jitter of 0.15ps at 2.2GHz. The –46dBc reference spur at 55MHz is caused by insufficient isolation between the VCO and the sampler, and can be improved in a re-design. Excluding the 50Ω CML buffer for measurement and disabling the 0.8mA FLL, the PLL core draws 4.2mA, with 1mA in the VCO. Figure 23.2.6 summarizes the PLL performance. Compared with [4-6], this design achieves the lowest jitter while consuming several times less power as well as active area. To make a fair comparison between in-band phase noise $L_{in\text{-}band}$ in PLL designs, the dependency of $L_{in\text{-}band}$ on f_{Ref} and N should be normalized out [7]. The normalized $L_{in\text{-}band}$ of this design is >12dB lower than that of [4-6], at a low loop power.

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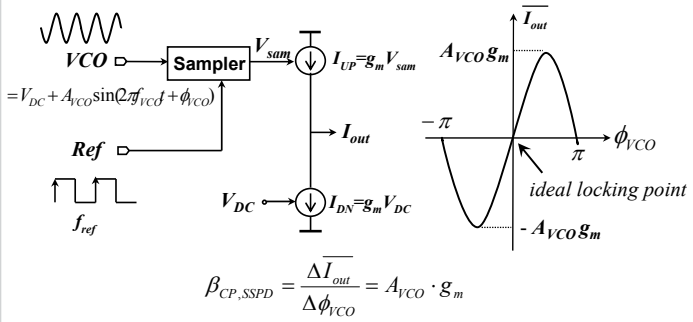

Figure 23.2.1: Principle and characteristic of a sub-sampling-based voltage-controlled PD/CP.

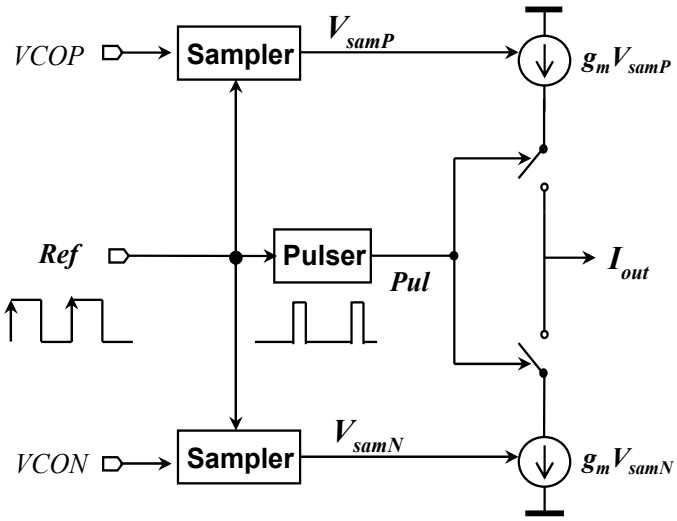

Figure 23.2.2: Sub-sampling PD/CP with pulse-width control.

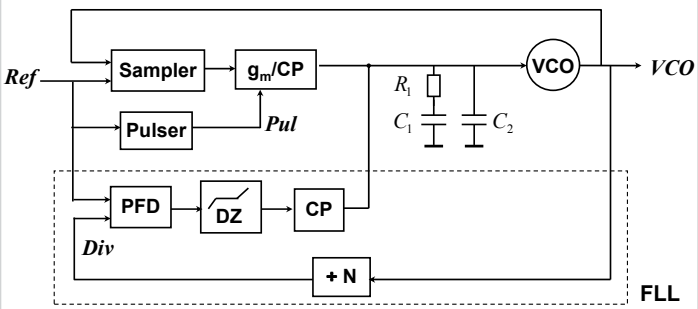

Figure 23.2.3: Block diagram of the sub-sampling PLL.

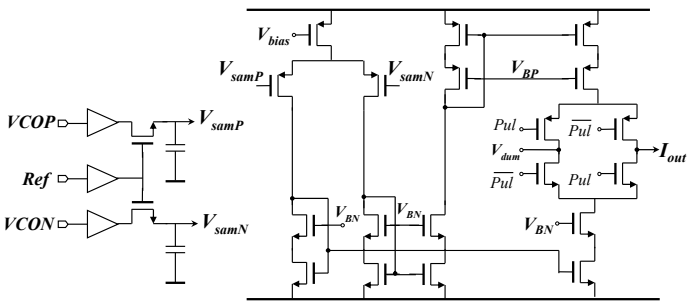

Figure 23.2.4: Schematic of the sub-sampling PD/CP.

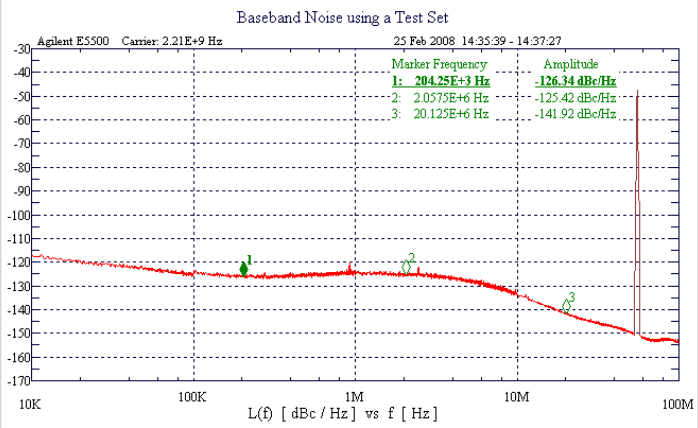

Figure 23.2.5: Measured PLL output phase noise. Reference spur at 55MHz is –46dBc, measured from a spectrum analyzer.

	This Work	[6]	[5]	[4]
Output Frequency	2.2 GHz	3.67 GHz	3.125 GHz	10 GHz
Ref. Frequency f_{Ref}	55 MHz	50 MHz	62.5 MHz	2.5 GHz
RMS Output Jitter	0.15ps(10k-40M)	0.2ps(1k-40M)	0.56ps(1k-50M)	0.22ps(10k-20M)
In-band Phase Noise $\mathcal{L}_{in\text{-}band}$	-126 dBc/Hz @ 200kHz	-108 dBc/Hz @ 400kHz	-108 dBc/Hz @ 100kHz	-109 dBc/Hz @ 600kHz
Normalized In-band Phase Noise [6] $=L_{in\text{-}band}-20\log N-10\log f_{Ref}$	-235 dBc/Hz² @ 200kHz	-222 dBc/Hz² @ 400kHz	-220 dBc/Hz² @ 100kHz	-215 dBc/Hz² @ 600kHz
Power Consumption	7.6 mW	39 mW	25 mW	81 mW
Active Area	0.18 mm²	0.95 mm²	0.43 mm²	0.71 mm²
Technology	0.18-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	0.18-μm CMOS

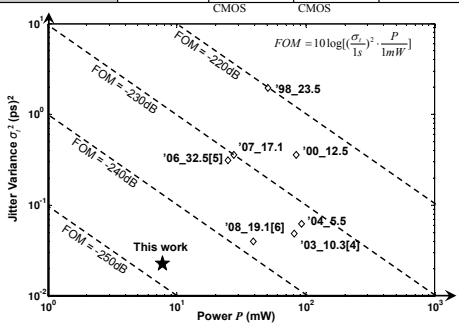

Figure 23.2.6: PLL performance summary and comparison with low-jitter PLL designs.

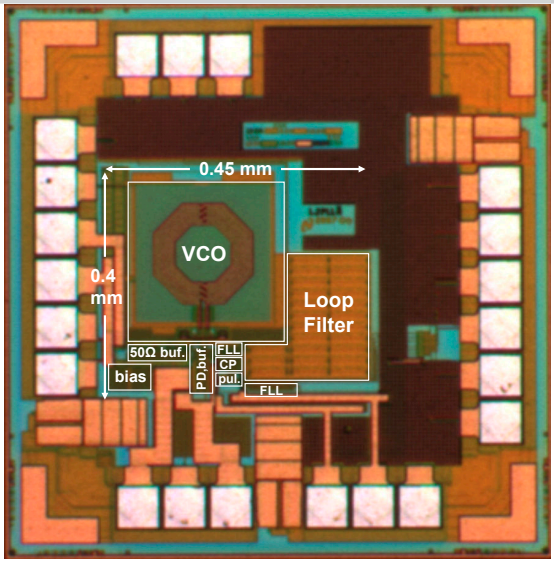

Figure 23.2.7: Chip micrograph.

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