Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops

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***Abstract*—This brief analyzes the jitter as well as the power dissipation of phase-locked loops (PLLs). It aims at defining a benchmark figure-of-merit (FOM) that is compatible with the well-known FOM for oscillators but now extended to an entire PLL. The phase noise that is generated by the thermal noise in the oscillator and loop components is calculated. The power dissipation is estimated, focusing on the required dynamic power. The absolute PLL output jitter is calculated, and the optimum PLL bandwidth that gives minimum jitter is derived. It is shown that, with a steep enough input reference clock, this minimum jitter is *independent* of the reference frequency and output frequency *for a given PLL power budget*. Based on these insights, a benchmark FOM for PLL designs is proposed.**

***Index Terms*—Clock generation, clock multiplier, figure-of-merit (FOM), frequency synthesizer, jitter, low jitter, low noise, phase-locked loop (PLL), phase noise, timing jitter.**

I. Introduction

PHASE-LOCKED loops (PLLs) are commonly used in almost every electronic system that needs timing of some kind, which is in the form of a clock or reference frequency. The timing jitter or phase noise of the PLL output is generally used as the main quality criterion. This brief aims at defining a benchmark figure-of-merit (FOM) to evaluate the PLL jitter performance in relation to the consumed power. A FOM can be instrumental for comparing designs, in a similar way as for analog-to-digital converters (ADCs) [1] or voltage-controlled oscillators (VCOs) [2], [3], and can stimulate the development of power-efficient high-performance PLLs.

To date, many different PLL architectures have been developed [4], [5]. However, the core of most PLLs is the same, i.e., the "classical PLL" architecture, as shown in Fig. 1(a). It consists of a VCO that is locked to a reference clock by a feedback loop with the following "loop components": a phase detector/charge pump (PD/CP), a loop filter (LF), and a frequency divider that divides by N. The VCO and the loop components all add noise and contribute to jitter at the PLL output.

The PLL jitter has been the topic of numerous studies [6]–[9]. Different from previous works, this brief focuses on finding a systematic relation between the PLL jitter and key design parameters like the reference frequency, output frequency, loop bandwidth, and power consumption. As changing these parameters largely affects the timing error in a systematic way, it makes sense to define a benchmark FOM that normalizes for this systematic dependency. This makes it possible to compare PLLs that are designed for different applications and get an indication of their relative merits.

This brief is arranged as follows. Section II analyzes the phase noise of the classical PLL. Section III estimates the noise contribution and power consumption of the VCO, and Section IV does this for the loop components. Section V discusses the PLL output jitter and how it can be optimized. Based on the insights developed, a benchmark FOM for PLL designs is proposed. Section VI draws the conclusions.

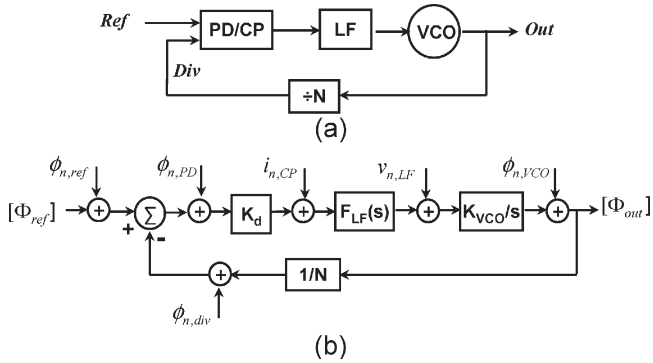

Fig. 1. Classical PLL (a) architecture and (b) phase domain model.

II. Classical PLL Phase Noise

A linear phase-domain model for the classical PLL is shown in Fig. 1(b), where K_d is the PD/CP detection gain, $F_{\rm LF}(s)$ is the loop filter transimpedance transfer function, and $K_{\rm VCO}$ is the VCO tuning gain. Various noise sources are also shown. Similar to [7] and [8], we focus on the fundamental limitations due to the thermal noise that normally dominates the jitter and neglects the $1/f$ noise. Therefore, the VCO phase noise has a $1/f^2$ shape due to the integration of white noise, whereas the spectrum of the other noise sources is flat. The noise transfer function from the VCO to the PLL output can be calculated as

$$H_{\rm VCO}(s) = \frac{1}{1+\frac{1}{N}\cdot K_d \cdot F_{\rm LF}(s)\cdot \frac{K_{\rm VCO}}{s}} = \frac{1}{1+G(s)} \quad (1)$$

where $G(s)$ is the PLL open-loop transfer function, and $s = j2\pi f$.

The rest noise originates from the loop components and is called the loop phase noise. When referred to the divider

Manuscript received June 3, 2008; revised September 9, 2008. Current version published February 25, 2009. This work was supported in part by National Semiconductor. This paper was recommended by Associate Editor A. Dec.

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Digital Object Identifier 10.1109/TCSII.2008.2010189

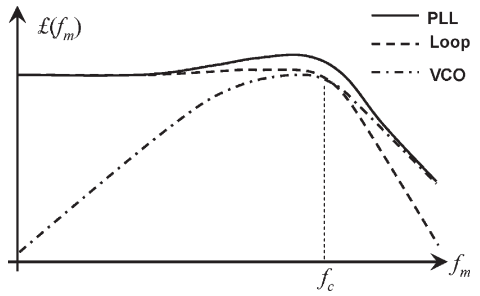

Fig. 2. Overall PLL output phase noise with $1/f$ noise neglected.

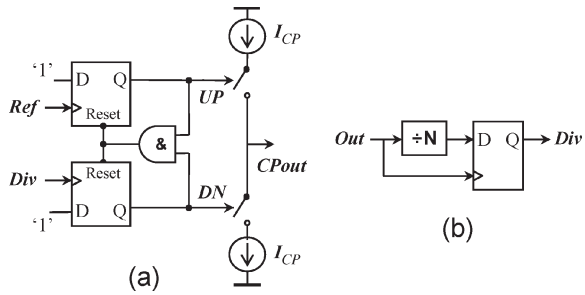

Fig. 3. Schematic of (a) a three-state PD/CP and (b) a divider with synchronization.

input,[1] the loop phase noise can be calculated as

$$\mathcal{L}_{\rm loop} \approx \frac{S_{\phi,\rm loop}}{2} = \frac{1}{2}\cdot N^2 \cdot \left(S_{\phi,\rm ref} + S_{\phi,\rm div} + S_{\phi,\rm PD} + \frac{S_{i,\rm CP}}{K_d^2} \right) \tag{2}$$

where the phase noise is expressed with the often used single-sideband noise power to carrier power ratio $\mathcal{L}$, which is half of the power spectral density S. In (2), we neglected the loop filter noise $S_{v,\rm LF}$ since it can be made negligible without adding power by either properly sizing the filter components [10] or lowering $K_{\rm VCO}$ by design [11]. The reference clock is commonly generated by crystal oscillators whose phase noise is usually also negligible. The reference phase noise $S_{\phi,\rm ref}$ is mainly contributed by reference dividers or reference buffers.

The noise transfer function from the (divider input referred) loop phase noise to the PLL output can easily be calculated as

$$H_{\rm loop}(s) = \frac{G(s)}{1+G(s)} = 1 - H_{\rm VCO}(s). \tag{3}$$

Comparing (1) and (3), the VCO phase noise is high-pass filtered, whereas the loop phase noise is low-pass filtered. Moreover, the 3-dB bandwidth for the two transfer functions is the same and determined by $G(s)$. We define their 3-dB bandwidth as the PLL bandwidth f_c. Fig. 2 shows the overall PLL output phase noise when a first-order low-pass loop filter is used. The loop phase noise is also referred to as PLL in-band phase noise since it dominates when the offset frequency $f_m < f_c$.

III. VCO Phase Noise and Benchmarking

The VCO phase noise has been the topic of numerous studies [3], [12]. It is found that the phase noise of a VCO is often systematically dependent on design parameters like oscillation frequency $f_{\rm VCO}$, power dissipation $P_{\rm VCO}$, and offset frequency f_m, at which the phase noise is measured. To compare the quality of VCO designs, the following benchmark FOM [2], [3] is widely used:

$$\text{FOM}_{\rm VCO} = 10\log\left(\mathcal{L}_{\rm VCO}(f_m) \cdot \frac{f_m^2}{f_{\rm VCO}^2} \cdot \frac{P_{\rm VCO}}{1\ \text{mW}} \right). \tag{4}$$

The unit of $\text{FOM}_{\rm VCO}$ is dBc/Hz ($\mathcal{L}$ times a dimensionless factor). A smaller $\text{FOM}_{\rm VCO}$ corresponds to a better VCO design.[2] The VCO phase noise can thus be expressed using $\text{FOM}_{\rm VCO}$ as

$$\mathcal{L}_{\rm VCO}(f_m) = \frac{10^{\text{FOM}_{\rm VCO}/10}}{P_{\rm VCO}/1\ \text{mW}} \cdot \frac{f_{\rm VCO}^2}{f_m^2}. \tag{5}$$

IV. Loop Phase Noise and Benchmarking

In [13], Banerjee found that the (in-band) loop phase noise is related to N and the frequency of the reference clock (which was measured at the PD input) $f_{\rm ref}$ as

$$\mathcal{L}_{\rm loop} \propto N^2 \cdot f_{\rm ref}. \tag{6}$$

He proposed a normalized phase noise floor $PN_{1\,\rm Hz}$ to benchmark the quality of a loop design, i.e.,

$$PN_{1\,\rm Hz} = \frac{\mathcal{L}_{\rm loop}}{N^2 \cdot f_{\rm ref}}. \tag{7}$$

The Banerjee model was applied to a wide range of PLLs in the industry and was supported by measurement results [13]. However, the theoretical basis for (6) is not clear in [13]. Moreover, (7) does not suffice as a benchmark FOM for the PLL loop since it does not take into account the power consumption. The analysis hereinafter addresses these issues.

To analyze the loop phase noise, we assume that the popular three-state PD/CP, as shown in Fig. 3(a), is used. In divider designs, synchronization is often used to minimize the divider noise, as shown in Fig. 3(b). The only noise source of the divider is then the retiming D-FlipFlop (DFF). The divide-by-N block only acts as an edge selector and does *not* contribute to noise. Its power consumption can thus be progressively scaled down [14]. As we aim to model the power needed to meet a certain phase noise/jitter requirement, we will subsequently ignore the divide-by-N block and only model the power of the retiming DFF.[3]

A. Phase Noise Due to the Reference Path, Divider, and PD

Among the loop noise sources, $S_{\phi,\rm ref}$, $S_{\phi,\rm div}$, and $S_{\phi,\rm PD}$ are caused by circuits like the reference buffer, retiming DFF, and PD, which all (effectively) run at the frequency $f_{\rm ref}$ and all

[1]Here, the loop phase noise is referred to the divider input (not to the PD input!), so that its level can directly be measured at the PLL output.

[2]Sometimes the negative of (4), i.e., a $\text{FOM}_{\rm VCO}$ with plus sign, is used [3], but this leads to very strange units for $\text{FOM}_{\rm VCO}$.

[3]There can be occasions where the power of the divide-by-N block becomes significant, e.g., to make it fast enough to cover very high VCO frequencies. However, this is not because of jitter or noise requirements.

respond to zero crossings at their inputs with zero crossings at their outputs. The output phase noise can be calculated from the absolute output jitter σ_t as [14]

$$S_\phi = 8\pi^2 \cdot f_{\rm ref} \cdot \sigma_t^2. \tag{8}$$

The output jitter of circuits like DFFs or inverters is related to the output noise voltage $\overline{v_n^2}$ and the slope of the output voltage at its zero crossing $SL_{\rm out}$ as [14], [15]

$$\sigma_t^2 = \frac{\overline{v_n^2}}{SL_{\rm out}^2} = \frac{F_n \cdot kT/C_{\rm out}}{SL_{\rm out}^2} \tag{9}$$

where F_n is the noise factor, and $C_{\rm out}$ is the capacitance at the output node. In the analysis below, we assume that the slope of the circuit input $SL_{\rm in}$ is big enough and does not limit $SL_{\rm out}$. Thus, (9) calculates the minimum achievable jitter of the circuit.

The minimum power consumed by a circuit is the dynamic power, which can be calculated as

$$P = f_{\rm ref} \cdot C_{\rm tot} \cdot V_{\rm dd}^2 \tag{10}$$

where $C_{\rm tot}$ is the total capacitance of the circuit.

Combining (9) and (10), we get

$$\sigma_t^2 = \frac{f_{\rm ref}}{P} \cdot \left\{ \frac{F_n \cdot kT \cdot V_{\rm dd}^2 \cdot C_{\rm tot}/C_{\rm out}}{SL_{\rm out}^2} \right\}. \tag{11}$$

To minimize the output jitter, designers can optimize the circuit by choosing the relative sizes of components, e.g., to maximize $SL_{\rm out}$. Once this optimization has been done, the jitter can always be reduced on a system level via admittance level scaling [16]. Admittance level scaling puts n identical circuits in parallel. As a result, the power consumption is n times higher and $\overline{v_n^2}$ is n times lower while the voltage slope at every node does not change [16]. Thus, $C_{\rm tot}/C_{\rm out}$ as well as F_n remains the same as all the node admittances scale together. Therefore, on the system level, we can treat the bracketed part in (11) as a design-dependent constant and get

$$\sigma_t^2 \propto f_{\rm ref}/P. \tag{12}$$

For the loop noise contributions $S_{\phi,\rm div}$, $S_{\phi,\rm ref}$, and $S_{\phi,\rm PD}$, we can conclude with (8) and (12) that

$$S_\phi \propto f_{\rm ref}^2/P. \tag{13}$$

B. Phase Noise Due to the CP

Different from the circuits in Section IV-A, the CP outputs current/charge instead of crossing moments. Assuming for simplicity that the CP up and down current sources have the same properties, the power spectral density of the (thermal) noise current generated by the CP is

$$S_i = 2 \times 4kT\gamma \cdot g_{m,\rm CP} = 8kT\gamma \cdot (\alpha I_{\rm CP}/V_{\rm eff,CP}) \tag{14}$$

where γ and $V_{\rm eff,CP}$ are, respectively, the noise factor and the effective gate voltage of the transistors in the current sources, $I_{\rm CP}$ is the CP current, α is the transistor model parameter that is equal to 2 for the square-law model, and $\alpha I/V_{\rm eff}$ represents the transconductance g_m.

In steady state, the CP is switched on only for a fraction of time $\tau_{\rm PD}$ of each period $T_{\rm ref}$ to avoid the dead zone. The equivalent CP (thermal) noise current can be calculated as [9]

$$S_{i,\rm CP} = S_i \cdot (\tau_{\rm PD}/T_{\rm ref}). \tag{15}$$

The minimum power needed by a CP is related to the charge delivered in steady state

$$P_{\rm CP} = I_{\rm CP}V_{\rm dd} \times (\tau_{\rm PD}/T_{\rm ref}) = I_{\rm CP}V_{\rm dd}\tau_{\rm PD} \cdot f_{\rm ref}. \tag{16}$$

For a three-state PD/CP, it is well known that $K_d = I_{\rm CP}/2\pi$. With (14)–(16) and some manipulations, we get

$$\frac{S_{i,\rm CP}}{K_d^2} = \frac{f_{\rm ref}^2}{P_{\rm CP}} \cdot \left\{ \tau_{\rm PD}^2 \cdot \frac{32\pi^2\alpha\gamma \cdot kT \cdot V_{\rm dd}}{V_{\rm eff,CP}} \right\} \propto \frac{f_{\rm ref}^2}{P_{\rm CP}} \tag{17}$$

where the bracketed part is treated as a design- and process-dependent constant.

C. Loop Phase Noise Benchmarking

When admittance level scaling is applied to the whole loop, the relative power contribution of each block is kept the same since all the blocks equally scale. Based on (2), (13), and (17) and the previously mentioned assumptions, we can conclude that

$$\mathcal{L}_{\rm loop} \propto N^2 \cdot f_{\rm ref} \cdot \frac{f_{\rm ref}}{P_{\rm loop}} = \frac{f_{\rm out}^2}{P_{\rm loop}} \tag{18}$$

where $P_{\rm loop}$ is the power consumption of the PLL loop as a whole, excluding the VCO.

Note that we assumed dynamic power consumption, i.e., $P_{\rm loop}$ scales with $f_{\rm ref}$, so (18) shows the same proportionality as the Banerjee model in (6). In addition to (6), (18) also takes into account the power dissipation. For a given $f_{\rm out}$, using a larger $f_{\rm ref}$ not only reduces the (in-band) loop phase noise but also increases the power consumption.

Based on (18), we propose to define a benchmark FOM for PLL loop designs as

$$\text{FOM}_{\rm loop} = 10\log\left[\mathcal{L}_{\rm loop} \cdot \left(\frac{1\text{ Hz}}{f_{\rm out}}\right)^2 \cdot \frac{P_{\rm loop}}{1\text{ mW}}\right] \tag{19}$$

where $f_{\rm out}$ and $P_{\rm loop}$ are normalized to 1 Hz and 1 mW, respectively, so that the unit of $\text{FOM}_{\rm loop}$ is dBc/Hz, which is the same as for $\text{FOM}_{\rm VCO}$. A smaller $\text{FOM}_{\rm loop}$ corresponds to a better loop design. The loop phase noise can now be expressed with $\text{FOM}_{\rm loop}$ as

$$\mathcal{L}_{\rm loop} = 10^{\text{FOM}_{\rm loop}/10} \cdot \left(\frac{f_{\rm out}}{1\text{ Hz}}\right)^2 \cdot \frac{1\text{ mW}}{P_{\rm loop}}. \tag{20}$$

V. PLL Jitter and Benchmarking

A. PLL Output Jitter

Jitter can be characterized in several different ways [6]. This brief chooses to use absolute jitter as it is often used in the PLL design literature. The relation with other jitter measures can be

found in [6]. The variance of the long-term PLL absolute jitter is related to the phase noise as

$$\sigma^2_{t,\mathrm{PLL}} = \frac{2\int_0^\infty \mathcal{L}_{\mathrm{PLL}}(f_m)df_m}{(2\pi f_{\mathrm{out}})^2} = \frac{1}{2\pi^2 f^2_{\mathrm{out}}} \cdot \int_0^\infty \mathcal{L}_{\mathrm{PLL}}(fm)df_m. \tag{21}$$

The PLL output jitter variance $\sigma^2_{t,\mathrm{PLL}}$ is the sum of the jitter variance caused by the VCO $\sigma^2_{t,\mathrm{VCO}}$ and the loop $\sigma^2_{t,\mathrm{loop}}$. The jitter variance due to the VCO can be calculated as

$$\sigma^2_{t,\mathrm{VCO}} = \frac{1}{2\pi^2 f^2_{\mathrm{out}}} \cdot \int_0^\infty \mathcal{L}_{\mathrm{VCO}}(f_m) \cdot |H_{\mathrm{VCO}}(j2\pi f_m)|^2 df_m. \tag{22}$$

The value of (22) is dependent on the bandwidth and shape (related to phase margin) of $H_{\mathrm{VCO}}(s)$. Assuming a given open-loop transfer function $G_0(s)$ that results in a close-loop transfer function $H_{\mathrm{VCO},0}(s)$ with a 3-dB bandwidth of $f_{c,0}$, scaling the bandwidth to f_c while keeping the same shape (thus the phase margin) results in a new transfer function [17]

$$H_{\mathrm{VCO}}(s) = H_{\mathrm{VCO},0}\left(s \cdot \frac{f_{c,0}}{f_c}\right). \tag{23}$$

Substituting (23) into (22) yields

$$\sigma^2_{t,\mathrm{VCO}} = \frac{1}{2\pi^2 f^2_{\mathrm{out}}} \cdot \int_0^\infty \mathcal{L}_{\mathrm{VCO}}(f_m) \cdot \left| H_{\mathrm{VCO},0}\left(j2\pi f_m \cdot \frac{f_{c,0}}{f_c}\right)\right|^2 df_m. \tag{24}$$

Since the VCO phase noise has a $1/f^2$ shape, the VCO phase noise can also be expressed as

$$\mathcal{L}_{\mathrm{VCO}}(f_m) = \frac{\mathcal{L}_{\mathrm{VCO}}(f_r) \cdot f_r^2}{f_m^2} \tag{25}$$

where $\mathcal{L}_{\mathrm{VCO}}(f_r)$ is the VCO phase noise measured at a certain offset frequency f_r. We can then rewrite (24) as

$$\begin{aligned}\sigma^2_{t,\mathrm{VCO}} &= \frac{\mathcal{L}_{\mathrm{VCO}}(f_r)\cdot f_r^2}{2\pi^2 f^2_{\mathrm{out}}} \cdot \int_0^\infty \left| H_{\mathrm{VCO},0}\left(j2\pi f_m \cdot \frac{f_{c,0}}{f_c}\right)\right|^2 \frac{df_m}{f_m^2} \\ &= \frac{\mathcal{L}_{\mathrm{VCO}}(f_r)\cdot f_r^2}{2\pi^2 f^2_{\mathrm{out}}} \cdot \frac{f_{c,0}}{f_c} \cdot \int_0^\infty |H_{\mathrm{VCO},0}(j2\pi f)|^2 \frac{df}{f^2}. \end{aligned} \tag{26}$$

Substituting (1) into (26) and using $s = j2\pi f$ yields

$$\sigma^2_{t,\mathrm{VCO}} = \frac{2\mathcal{L}_{\mathrm{VCO}}(f_r)\cdot f_r^2}{f^2_{\mathrm{out}}} \cdot \frac{f_{c,0}}{f_c} \cdot \int_0^\infty \left| \frac{1}{s\cdot[1+G_0(s)]}\right|^2 df. \tag{27}$$

Using a similar analysis as for the VCO, the PLL output jitter variance due to the loop can be calculated as

$$\sigma^2_{t,\mathrm{loop}} = \frac{\mathcal{L}_{\mathrm{loop}}}{2\pi^2 f^2_{\mathrm{out}}} \cdot \frac{f_c}{f_{c,0}} \cdot \int_0^\infty \left| \frac{G_0(s)}{1+G_0(s)}\right|^2 df. \tag{28}$$

B. PLL Jitter Optimization

It is clear from (27) and (28) that a larger value of f_c will lower the output jitter due to the VCO while raising the jitter contribution of the loop. The optimum PLL bandwidth $f_{c,\mathrm{opt}}$ that gives the minimum PLL output jitter can be calculated with (27) and (28) as

$$f_{c,\mathrm{opt}} = \sqrt{\frac{\mathcal{L}_{\mathrm{VCO}}(f_r)\cdot f_r^2}{\mathcal{L}_{\mathrm{loop}}}} \cdot 2\pi \cdot \sqrt{f_{c,0}^2 \cdot \frac{\int_0^\infty \left|\frac{1}{s\cdot[1+G_0(s)]}\right|^2 df}{\int_0^\infty \left|\frac{G_0(s)}{1+G_0(s)}\right|^2 df}}. \tag{29}$$

Given $f_{c,\mathrm{opt}}$, the minimum PLL output jitter variance $\sigma^2_{t,\mathrm{PLL,min}}$ is

$$\begin{aligned}\sigma^2_{t,\mathrm{PLL,min}} &= \frac{1}{\sqrt{P_{\mathrm{loop}}\cdot P_{\mathrm{VCO}}}} \cdot 10^{\frac{\mathrm{FOM_{loop}}+\mathrm{FOM_{VCO}}}{20}} \\ &\cdot \sqrt{\int_0^\infty \left|\frac{G_0(s)}{1+G_0(s)}\right|^2 df \cdot \int_0^\infty \left|\frac{1}{s\cdot[1+G_0(s)]}\right|^2 df} \cdot \frac{2}{\pi} \cdot \frac{1\ \mathrm{mW}}{1\ \mathrm{Hz}} \end{aligned} \tag{30}$$

where the VCO and the loop phase noise are represented with $\mathrm{FOM_{VCO}}$ and $\mathrm{FOM_{loop}}$ by using (5) and (20). Substituting $f_{c,\mathrm{opt}}$ into (27) and (28), it can be shown that $\sigma^2_{t,\mathrm{VCO}} = \sigma^2_{t,\mathrm{loop}} = \sigma^2_{t,\mathrm{PLL,min}}/2$. This means that *the VCO and the loop components contribute equal jitter in an optimized PLL design*. Substituting (29) with typical values of $G_0(s)$ and $f_{c,0}$ into (25), it can be shown that $\mathcal{L}_{\mathrm{VCO}}(f_{c,\mathrm{opt}}) \approx \mathcal{L}_{\mathrm{loop}}$, which means that $f_{c,\mathrm{opt}}$ is approximately where the spectrum of the VCO and the loop noise intersects. These conclusions are similar to the conclusions drawn in [5].

For a given PLL power budget P_{PLL}, it is easy to show that the minimum value of (30) occurs when $P_{\mathrm{loop}} = P_{\mathrm{VCO}} = P_{\mathrm{PLL}}/2$, when the other conditions are kept the same. This means that *the VCO and the loop components consume equal power in an optimized PLL design*. With this observation, the minimum PLL jitter variance in (30) evolutes to

$$\begin{aligned}\sigma^2_{t,\mathrm{PLL,min}} &= \frac{1}{P_{\mathrm{PLL}}} \cdot \left\{ 10^{\frac{\mathrm{FOM_{loop}}+\mathrm{FOM_{VCO}}}{20}} \cdot \frac{4}{\pi} \cdot \frac{1\ \mathrm{mW}}{1\ \mathrm{Hz}} \right\} \\ &\cdot \left\{ \sqrt{\int_0^\infty \left|\frac{G_0(s)}{1+G_0(s)}\right|^2 df \cdot \int_0^\infty \left|\frac{1}{s\cdot[1+G_0(s)]}\right|^2 df} \right\}. \end{aligned} \tag{31}$$

It should be noted that the optimal PLL bandwidth for minimum jitter may not meet the stability or locking time requirements, and spending equal power on the loop and the VCO may also have practical difficulties. However, they are still the theoretical optimum under the conditions mentioned. Practically, they provide designers the directions for PLL jitter and power optimization.

C. PLL Benchmarking and Discussion

In (31), the first bracketed part is a constant that is determined by the quality of the VCO and loop design. The second bracketed part, i.e., the integration, is related to the phase margin of the loop transfer function. The optimum phase margin for minimum jitter is different for different PLL types and orders [8]. For example, the phase margin in a second-order type-II PLL is preferred to be large [8]. When the phase margin is close to 90°, the value of the integration is about 0.25, and we get

$$\sigma^2_{t,\mathrm{PLL,min}} = \frac{1}{P_{\mathrm{PLL}}} \cdot 10^{\frac{\mathrm{FOM_{loop}}+\mathrm{FOM_{VCO}}}{20}} \cdot \frac{1}{\pi} \cdot \frac{1\ \mathrm{mW}}{1\ \mathrm{Hz}}. \tag{32}$$

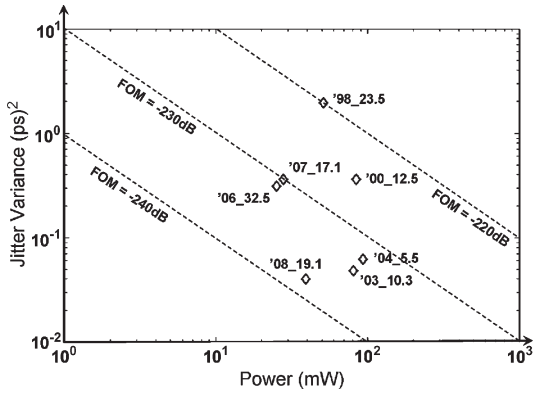

Fig. 4. ISSCC low-jitter PLL designs (Year_PaperNumber).

When the integration part in (31) is treated as a (PLL type and order dependent) constant, we can conclude that

$$\sigma^2_{t,\mathrm{PLL,min}} \propto 1/P_{\mathrm{PLL}}. \tag{33}$$

We can see that when a PLL design is optimized, i.e., when (31) holds (equal loop and VCO power, and optimal PLL bandwidth), the minimum PLL jitter is *independent* of f_{ref}[4] and f_{out}, *given a fixed PLL power budget*. Note that for a higher f_{out}, the loop and VCO phase noise is higher according to (5) and (20). However, the output clock period is smaller with a higher f_{out}. When the phase noise is converted to jitter using (21), these two factors cancel out. A similar observation was also made in [18]. Based on (33), we define a PLL benchmark FOM as

$$\mathrm{FOM_{PLL}} = 10\log\left[\left(\frac{\sigma_{t,\mathrm{PLL}}}{1s}\right)^2 \cdot \frac{P_{\mathrm{PLL}}}{1\ \mathrm{mW}}\right]. \tag{34}$$

The unit of $\mathrm{FOM_{PLL}}$ is decibels. A smaller $\mathrm{FOM_{PLL}}$ corresponds to a better PLL design.

Comparing (31) and (34), we can see that

$$\mathrm{FOM_{PLL}} \propto \mathrm{FOM_{loop}} + \mathrm{FOM_{VCO}}. \tag{35}$$

Therefore, the design quality of the loop and VCO is equally important. This is intuitive since the loop and the VCO have equal contribution to both power and jitter in an optimized PLL design.

With the defined PLL FOM, different PLL designs can be compared by using a single number. Fig. 4 shows the performance of some PLL designs in the recent years' International Solid State Circuits Conference (*ISSCC*) along with the $\mathrm{FOM_{PLL}}$ lines. We can see that the $\mathrm{FOM_{PLL}}$ improves over the years, as we would expect for a conference that claims to present the state-of-the-art work. The state-of-the-art $\mathrm{FOM_{PLL}}$ is close to -240 dB.

VI. Conclusion

The phase noise and the power consumption of the VCO and loop components in a classical PLL have been analyzed. A benchmark FOM for loop designs ($\mathrm{FOM_{loop}}$) has been proposed, complementary to the existing VCO FOM. The absolute PLL output jitter has been calculated, and an expression for the minimum jitter has been derived. It has been shown that, to minimize the output jitter for a given power budget, designers should aim at the following: 1) spending equal power on the loop and the VCO; and 2) setting the loop bandwidth such that the loop and the VCO equally contribute to the total jitter. In such an optimized PLL, the minimum jitter is independent of the reference frequency and output frequency for a given power budget. Based on these insights, a benchmark FOM for PLL designs ($\mathrm{FOM_{PLL}}$) has been proposed. It can be used to compare various PLL designs in applications where jitter is important. Moreover, system designers can use it to predict and tradeoff jitter and power during system-level design.

[4]Note that we assumed a steep enough input clock. If the reference input is a low-frequency sine wave, then SL_{in} is low and limits SL_{out}. In that case, SL_{out} is typically proportional to SL_{in}. Increasing f_{ref} then could reduce the jitter.

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