

26.4 Spur-Reduction Techniques for PLLs Using Sub-Sampling Phase Detection

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In PLL designs, a wide loop bandwidth is often desired as it offers fast settling time, reduces on-chip loop filter area and sensitivity of the VCO to pulling. The reference spur is a major issue when the bandwidth is increased, because ripples on the VCO control line undergo less filtering by the loop filter. This paper proposes design techniques based on sub-sampling phase detection to reduce the reference spur of a 2.2GHz PLL to -80dBc at a high loop-bandwidth-to-reference-frequency ratio (f_{BW}/f_{ref}) of 1/20.

In a charge-pump (CP) PLL, the mismatch between the CP up current source I_{UP} and down current source I_{DN} is often the major source of reference spur. In a conventional phase-frequency-detector (PFD)/CP as shown in Fig. 26.4.1(a), the PFD converts the VCO phase error into the I_{UP} and I_{DN} switch-on time difference ($t_{UP,on} - t_{DN,on}$). I_{UP} and I_{DN} thus have a *variable on-time* but *constant amplitude* fixed by biasing. In case of I_{UP} and I_{DN} mismatch, one of them has to be on for a longer time in order to reach the steady state condition that the net CP output charge is zero. This causes CP output current ripple as shown in Fig. 26.4.1(a), and thus reference spurs.

The sub-sampling PLL (SSPLL) in [1] achieves very low in-band phase noise at low power. We will show now that it is intrinsically insensitive to CP mismatch which can be exploited to also achieve a very low spur. The sub-sampling phase detector (SSPD)/CP in the SSPLL is displayed in Fig. 26.4.1(b) [1]. The SSPD samples the VCO with a reference clock Ref and converts the VCO phase error into sampled voltage difference ($V_{sam+} - V_{sam-}$), which controls the amplitude of I_{UP} and I_{DN} . A block Pulser generates a pulse Pul , non-overlapping with Ref , and switches on/off I_{UP} and I_{DN} *simultaneously*. This Pulser controls the SSPD/CP gain and functions as the second track-and-hold for the VCO sampling action. Therefore, I_{UP} and I_{DN} have a *variable amplitude* but a *constant on-time* equal to the width of Pul . Since I_{UP} and I_{DN} have equal on-time, the steady state condition of zero net CP output charge is met only if I_{UP} and I_{DN} also have equal amplitude. In other words, there will be no I_{UP} and I_{DN} mismatch. Actually, the PLL loop tunes the amplitudes of I_{UP} and I_{DN} until they match, by shifting the locking point away from the ideal point (VCO zero-crossing), see Fig. 26.4.1(b). The current source switches still suffer from mismatch but their contribution to CP current ripple is small.

Although the CP in Fig. 26.4.1(b) produces small ripple, the SSPD driving the CP samples the VCO and thus can cause spurs. The sampler switching activity disturbs the VCO operation in three ways: 1) charge sharing between the VCO and sampling capacitors C_{sam} since the voltages on C_{sam} and VCO output may not be equal when they are connected at the switch-on moment; 2) variation in the VCO capacitive load and thus f_{VCO} when the switches connects/dis-connects the SSPD/CP to the VCO; 3) charge injection from the sampling switches to the VCO. Due to these effects, a poor reference spur of -46dBc was measured in [1] although a buffer was used to isolate the VCO and SSPD.

Figure 26.4.2 shows the proposed architecture which overcomes the aforementioned spur issues. The core is a SSPLL similar to [1]. It uses a SSPD that utilizes the Ref rising edge to sample the VCO. In steady state, the sampling edge, i.e. Ref rising edge, is aligned with a VCO zero-crossing by the SSPLL loop. If we can tune the Ref falling edge such that it is also aligned to a VCO zero-crossing, the VCO voltages at the Ref rising/falling edges will be the same and there is ideally no charge sharing between VCO and C_{sam} at the SSPD switch-on moment. This is achieved by using a duty cycle controlled Ref buffer and a sub-sampling DLL (SSDLL), see Fig. 26.4.2. In the Ref buffer, the crystal oscillator (XO) directly controls the NMOS N1 while a pulse V_{GP} generated from the XO with a delay Δt and a timing control circuit (TCC) controls the PMOS P1. The timing is set such that the conduction time of P1 and N1 is non-overlapping. In

this way, the Ref rising edge is defined by XO via N1 (and the inverter thereafter) while the Ref falling edge is independently defined by V_{GP} via P1. The Ref falling edge can then be tuned by the DLL via tuning Δt , without affecting the Ref rising edge. The DLL uses the same SSPD/CP as the PLL, but its sampling clock \overline{Ref} is the inverse of Ref . A transmission gate compensates the inverter delay. The DLL thus uses the \overline{Ref} rising edge to sample the VCO and aligns the \overline{Ref} rising edge, i.e., the Ref falling edge to the VCO zero-crossing. Now, both the Ref rising and falling edges are aligned with the VCO zero-crossings and the condition for no charge sharing is achieved. Moreover, since there are now two identical SSPD/CP switched by complementary clocks, the VCO is either connected to one or the other SSPD/CP and its capacitive load is kept constant. The complementary way of switching also cancels the charge injection from the sampling switches to the VCO. Therefore, all the three aforementioned SSPD related spur mechanisms are largely suppressed. Since the DLL only controls the Ref falling edge which is not the sampling edge for the PLL, it will not disturb the PLL operation nor add noise to the PLL output.

Figure 26.4.3 shows a detailed schematic of the SSPD/CP with Pulser. Since I_{UP} and I_{DN} mismatch will be tuned out by the PLL loop, the current sources' output impedance is not an issue and single transistors are used, which saves voltage headroom. To achieve low CP ripple, the charge sharing between I_{UP} and I_{DN} drain nodes (d1 and d2 in Fig. 26.4.3) and the loop filter (LF) is another concern. The CP thus uses a current steering topology, where I_{UP} and I_{DN} are either connected to LF or dumped to a capacitor C_{dump} . Ideally, there is no charge sharing if the voltages on d1 and d2 are kept constant during switching, i.e., if we can set $V_{LF} = V_{dump}$. In a conventional CP, this requires a unity-gain buffer. Here, this is achieved for free as explained below. In steady state, the net charge into the LF and C_{dump} should be both zero. Since I_{UP} and I_{DN} have equal on-time in both 'connected to LF' and 'dumped to C_{dump} ' cases, they must also have equal amplitude in both cases. This condition is met only if $V_{LF} = V_{dump}$, where the finite current source output impedance is actually the equalizing mechanism.

The chip fabricated in a standard 0.18- μ m CMOS process occupies an active area of 0.2 mm² (Fig. 26.4.7). All circuitry uses 1.8V supply, while separate supply domains provide isolation. The 2.2GHz PLL tested with package consumes 3.8mW with <0.2mW in the DLL. The in-band phase noise is -121dBc/Hz at 200kHz as shown in Fig. 26.4.4. It is 5dB higher than that of [1], mainly because here we used a several times smaller C_{sam} which helps reducing the spur level but raises the noise contribution of the SSPD and its buffer. Fig. 26.4.5 shows the reference spur measured from 20 samples. The worst case is -80dBc, 34dB better than [1], and the best case is -85dBc. Fig. 26.4.6 displays a comparison with other low spur PLLs in [2-5]. This design has the lowest spur, combined with the lowest in-band phase noise as well as the lowest power consumption, while using a high f_{BW}/f_{ref} of 1/20.

Acknowledgements:

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References:

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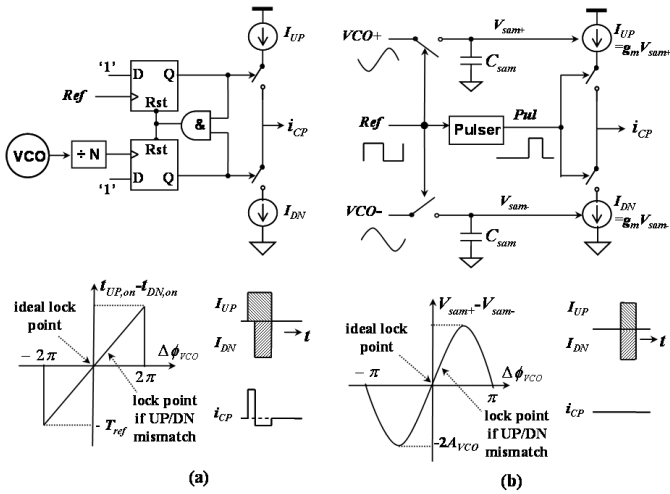


Figure 26.4.1: (a) Conventional 3-state PFD and timing controlled CP, (b) Sub-sampling PD and amplitude controlled CP.

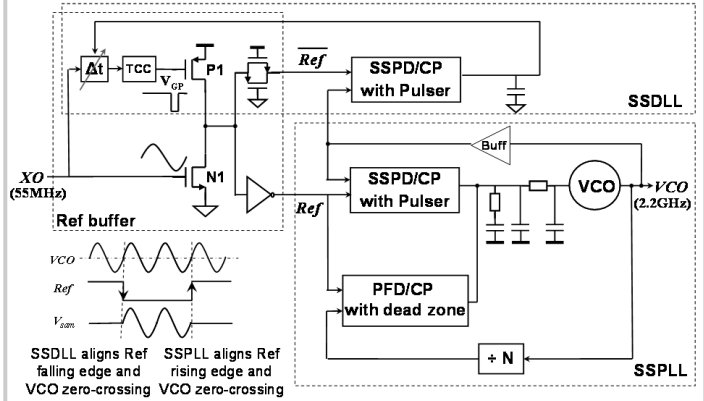


Figure 26.4.2: Block diagram of the PLL.

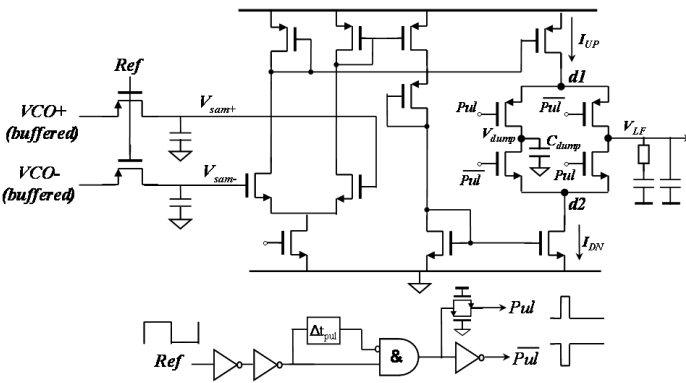


Figure 26.4.3: Schematic of SSPD/CP with Pulser.

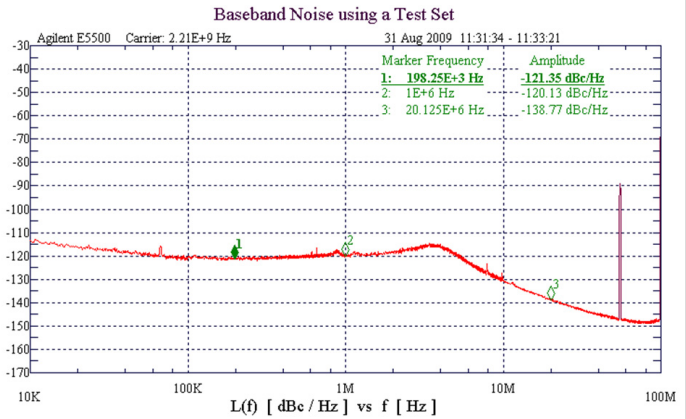


Figure 26.4.4: Measured PLL phase noise spectrum from an Agilent E5501B phase noise measurement setup.

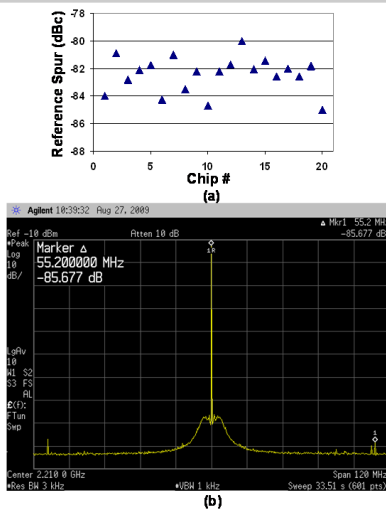


Figure 26.4.5: (a) Measured reference spur level from 20 samples and (b) the best case reference spur measured among the 20 samples using Agilent E4440A Spectrum Analyzer.

	This Work	[2]	[3]	[4]	[5]*
Out Frequency	2.21GHz	5.5GHz	5.4GHz	5.2GHz	2.4GHz
Ref Frequency	55.25MHz	43MHz	10MHz	10MHz	12MHz
f_{BW}/f_{ref}	1/20	1/540	1/400	1/50	1/12
Ref Spur (Sample #)	-80dBc (#=20)	-69dBc (#=1)	-70dBc (#=1)	-69dBc (#=1)	-70dBc (#=4)
In-band Phase Noise	-121dBc/Hz @200kHz	-88dBc/Hz @40kHz	-63dBc/Hz @10kHz	-76dBc/Hz @20kHz	-103dBc/Hz @100kHz
Power	3.8mW	23mW	13.5mW	19.8mW	39mW
Active Area	0.20mm ²	?	0.49mm ²	0.64mm ²	<4.8mm ²
Technology	0.18- μ m CMOS	0.25- μ m CMOS	0.25- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS

*This is a Fractional-N PLL with the numbers measured in Integer-N mode.

Figure 26.4.6: PLL performance summary and comparison with low spur PLL designs.

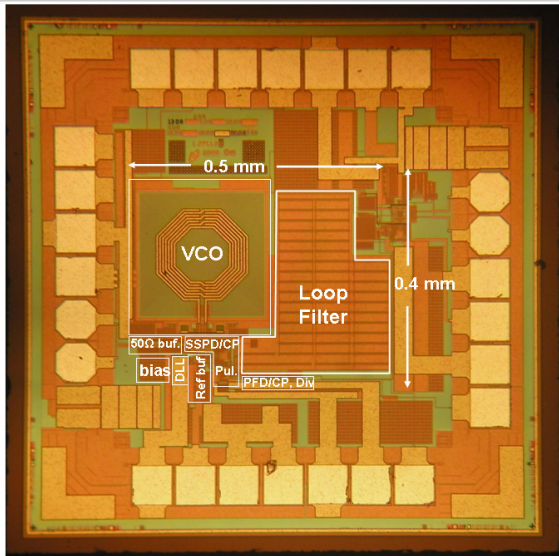


Figure 26.4.7: Chip micrograph.