A Differential 4-Path Highly Linear Widely Tunable On-Chip Band-Pass Filter

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***Abstract* — A passive switched capacitor RF bandpass filter with clock controlled center frequency is realized in 65nm CMOS. An off-chip transformer which acts as a balun, improves filter-Q and realizes impedance matching. The differential architecture reduces clock-leakage and suppresses selectivity around even harmonics of the clock. The filter has a constant -3dB bandwidth of 35MHz and can be tuned from 100MHz up to 1GHz. IIP3 is better than 19dBm, P_{1dB}=2dBm and NF<5.5dB at P_{diss}=2mW to 16mW.**

***Index Terms* — N-path filters, commutated capacitor, CMOS bandpass filter, inductorless, cognitive radio, software-defined radio.**

I. Introduction

Tunable RF filters have many applications in receivers, transmitters and synthesizers, e.g. to reject out-of-band interference, harmonics, and spurious tones. Although off-chip passive filters provide high rejection, low insertion loss and high linearity, integrated CMOS alternatives are highly desired for reasons of size, cost and programmability. Moreover, especially below 1GHz, filters based on on-chip inductors have limited Q resulting in significant insertion loss, while also consuming large die area. Q-enhanced techniques [1]-[3] can improve filter quality factor but degrade linearity and noise.

Tunable filters based on periodically time variant networks have been addressed in literature under different names such as N-path filters, sampled data filters, commutated capacitors, etc. [4]-[6]. These filters basically transfer the lowpass/notch characteristic of a network to a bandpass/bandstop one by means of frequency mixers. An N-path filter can realize an inductor-less tunable band-pass or band-stop filter [4] in which the center frequency is determined by the mixing frequency. These features make N-path filters interesting for software defined and cognitive radios in which tunable filters with a large frequency tuning range are highly wanted. While the concept of passive N-path filters and commutating networks is known for a long time and has been used for low frequencies [4], the concept seems to be somewhat forgotten. Recently, the concept was applied to high frequencies [7] where an 8-path filter with on-chip clocking was realized in CMOS.

In this paper we propose a 4-path differential bandpass filter. Compared to [7], the differential architecture suppresses selectivity around even harmonics of the mixing frequency. Moreover, input matching is provided by employing a wide-band RF transformer with termination resistor. The effects of switch resistance on the stop-band rejection and the tradeoffs between input matching, noise and achievable Q are addressed as well.

II. N-Path Filter

The basic block diagram of an N-path filter with bandpass characteristic is presented in Fig. 1 [4]. It is composed of N similar time invariant lowpass networks and 2N frequency mixers driven by time/phase shifted versions of clock p(t) and q(t). This architecture transfers a lowpass characteristic to a bandpass with the center frequency determined by the mixing frequency. In fact the input signal is downconverted to baseband, filtered and then upconverted again to the same band as V_{in}.

Now suppose that, as in Fig. 2a, we realize mixers with switches driven by multiphase clocks, while implementing the lowpass filters with simple RC networks. Since a resistor is a memory-less element, it can be shared by all paths and shifted in front of them. Moreover, the first set of switches can also implement the function of the second set of switches, if V_{out} is tapped between the resistor and switches (see Fig. 2b).

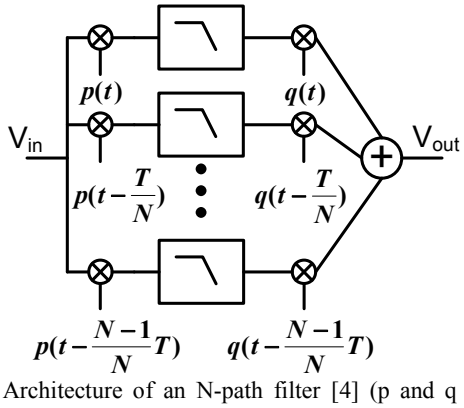

Fig. 1. Architecture of an N-path filter [4] (p and q are the mixing functions and T is the period of the mixing frequency).

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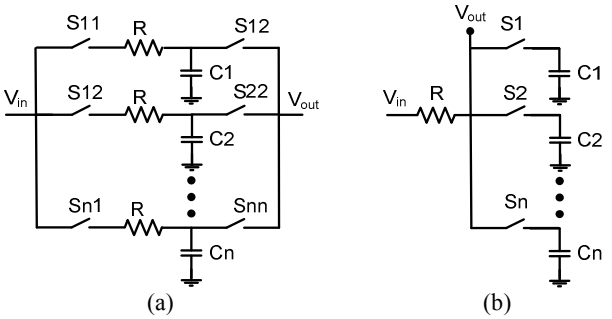

Fig. 2. (a) Switched-RC N-path filter. (b) Simplified version.

As a matter of fact Fig. 2b not only represents a simple form of an N-path filter, but it can also be utilized as multiphase passive mixer, if the voltages on the capacitors are considered as output [8]-[9]. The RC time-constant determines the -3dB bandwidth and thus the quality factor (Q) of the filter for a given center frequency. Larger RC results in less bandwidth, and hence renders a higher Q. In Fig. 2b, R can be considered as source impedance, but it can also serve as an "auxiliary resistance" to increase Q as in [7]. However, adding resistance results in noise degradation. In this paper we will increase source impedance by using a transformer which (ideally) doesn't add noise.

III. Proposed Architecture

The architecture of the proposed differential 4-path bandpass filter is illustrated in Fig. 3. Each path is differential-in and differential-out, but contains one grounded capacitor connected to two anti-phase driven NMOS switches. A 4-phase 25%-duty-cycle clock provides all required clocks (see Fig.3) and is derived from an external clock by dividers and logic. Considering the comb-like characteristic of N-path filters [4], i.e. its repetitive selectivity around harmonics of the switching frequency, the architecture of Fig. 3 cancels the even harmonics of the switching frequency due to anti-phase switching of the differential input. In fact for input signals around even harmonics of the clock frequency, no charge is stored on the capacitors in steady state and no upconverted signal appears at the output.

An off-chip wide-band (50-1000MHz) RF transformer serves as a balun for single to differential conversion. Moreover, it increases the impedance level seen by the switched-capacitor circuit, increasing Q of the filter without degrading its noise. Neglecting switch resistance, the input impedance R_{in} in Fig. 3, seen looking into the input of the IC before the switches at the switching frequency f_s, can be written as [8]:

$$R_{in} = \frac{8R_{out}}{\pi^2 - 8} \quad (1)$$

As shown in Fig. 3, R_{out} is the driving impedance seen by the switched-capacitor circuit. Using (1), the required value for R_M to provide matching can be found as:

$$R_M = \frac{4\pi^2 R_s}{16 - \pi^2} \quad (2)$$

For Rs=50Ω the value for R_M becomes 322Ω. In practice, the insertion loss of the transformer is usually non-negligible and in our case it was actually sufficient to implement R_M. In the general case an equivalent total resistance R_M according to (2) is needed for good S_{11}.

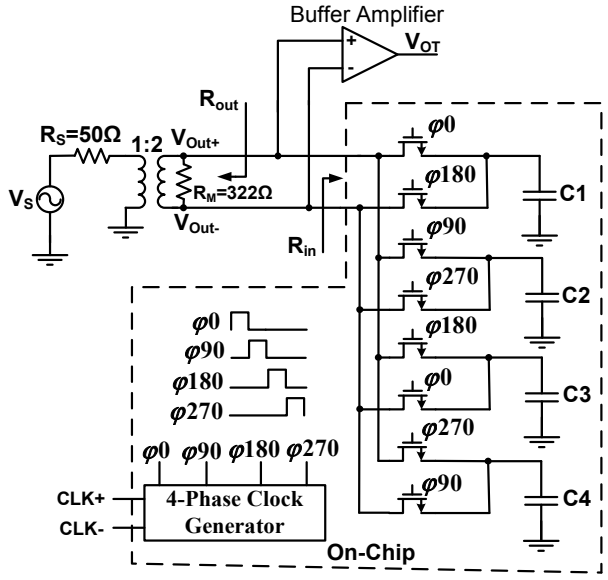

Fig. 3. Filter architecture including a balun and buffer amplifier for measurements.

IV. Measurement Results and Comparison

A prototype IC has been fabricated in 65nm standard CMOS technology (Fig. 4). A differential high input impedance buffer amplifier is added to the circuit in Fig. 3 to be able to measure with 50Ω equipment without loading the output of the filter. Measurement results show that the tunable filter in Fig. 3 works from 100MHz up to at least 1GHz. Fig. 5 shows measurement results and compares them to a simulation employing an ideal transformer and R_M=322Ω for f_s=400MHz, while also including a bond-wire inductance estimate. The buffer amplifier gain is de-embedded in all experiments, but the transformer effects are included. Close to f_s the input is matched to 50Ω and the -3dB bandwidth is 35MHz rendering a Q ranging from 3 to 29 (0.1 to 1GHz).

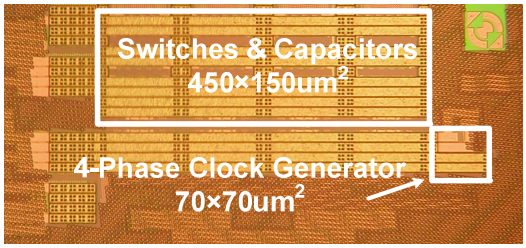

Fig. 4. Micrograph of the 65nm CMOS chip.

The maximum filter rejection is limited by non-zero switch resistance and impedance R_{out}. For frequencies far away from the switching frequency, input impedance R_{in} can be approximated as two times the switch resistance R_{SW} [8]. The maximum rejection, α, can coarsely be estimated as:

$$\alpha \approx 20\log\left(\frac{\pi^2}{8}\frac{2R_{SW}}{R_{out}+2R_{SW}}\right) \quad (3)$$

Thus increasing R_{out} not only results in less bandwidth and hence an increased Q, but also renders a larger maximum achievable filter rejection. More attenuation can also be achieved using wider switches at the cost of clock driver power. In the implemented architecture, $R_{SW}\approx 5\Omega$, $R_{out}=123\Omega$, resulting in α=-20.6dB. Measurement results render -16dB (Fig. 5). The error is mainly due to the effect of the non-zero rise and fall times of the clock which is not considered in deriving (3).

Fig. 5 also illustrates the frequency selectivity around odd harmonics of the switching frequency. A rejection of 10dB is found around the 3rd harmonic of the clock, while downconversion from the 3rd harmonic to the desired band also represents 10dB attenuation. Even order harmonics are rejected due to the differential nature of the circuit. The differential architecture also reduces the power leakage from the switching clock to the RF input. In Fig. 3, the rising and falling edges of the clock mainly produce a common mode signal, which is suppressed by the common mode rejection of the transformer. At the RF input -62dBm was measured. The flexible tuning capability of the filter is illustrated in Fig. 6 for f_s swept from 100MHz up to 1GHz. In-band S_{11} proves to be better than -10dB for the whole tuning range and the voltage transfer characteristic exhibits a maximum of 2dB passband attenuation. Due to parasitics of the transformer and printed circuit board some peaking occurs at 100 and 200MHz center frequencies. The main frequency limitations of the current design are related to the clocking circuit and transformer. Wider frequency ranges are possible by improving the clocking circuit and removing the transformer for on-chip applications. The implemented 4-phase clock generator consumes between 2mW and 16mW (f_s=0.1-1GHz, f_{CLK}=0.4 to 4GHz).

Noise figure measurements have been done using a low noise buffer amplifier. As de-embedding of the transformer and buffer amplifier noise contribution is non-trivial, raw measured data are shown in Fig. 7. The NF including transformer and buffer amplifier is below 5.5dB. Two simulated curves are also shown in Fig. 7 both for an ideal transformer and ideal buffer amplifier and: 1) $R_M=322\Omega$ (matched); 2) no R_M (unmatched). The latter case renders about 1dB noise figure. The measured IIP3 is 19dBm and is rather constant over frequency (Fig. 8). In table I the design is compared with two other on-chip filters, one using Q-enhancement [3] and the other an 8-path filter [7], clearly illustrating benefits in tuning-range, linearity and noise. In [7] the achieved Q is increased significantly by increasing source resistance without providing matching and also increasing the number of paths to 8. Inserting a resistor deteriorates the NF significantly. While reactive impedance transformation which is employed in this paper ensures a low NF.

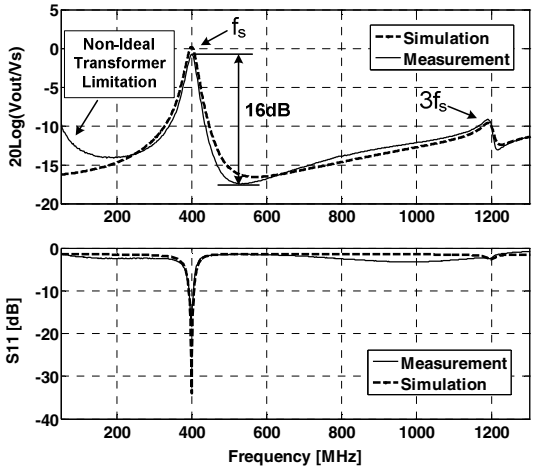

Fig. 5. Frequency transfer and S_{11} at f_s=400MHz.

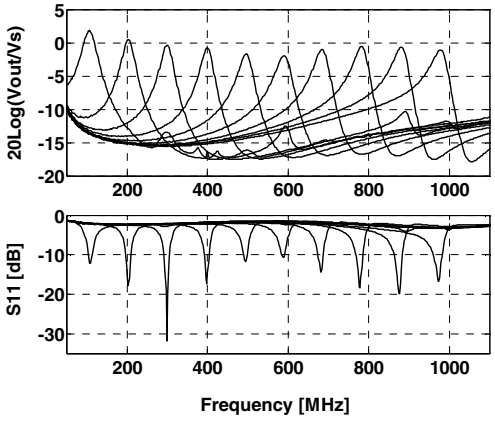

Fig. 6. Frequency transfer and S_{11} at f_s between 0.1 and 1GHz.

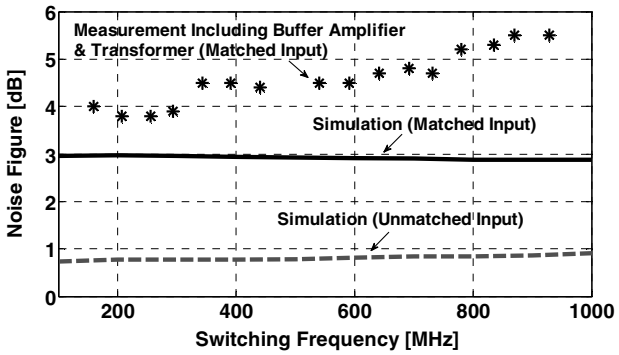

Fig. 7. Measured and simulated noise figure.

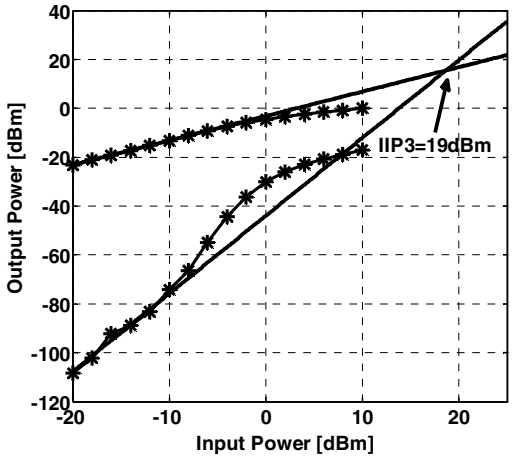

Fig. 8. Measured IIP3.

TABLE I
COMPARISON WITH OTHER DESIGNS

Performance	This Work	[3]	[7]
Process	65nm CMOS	0.18um CMOS	0.35um CMOS
Active Area	0.07 mm^2	0.81mm^2	1.9mm^2
Power Consumption	2 to 16mW	17mW	63mW
Frequency Tuning Range	0.1 to 1GHz	2 to 2.06GHz	240 to 530MHz
-3dB Band Width	35MHz	130MHz	1.75 to 4.6MHz
Voltage Gain	-2dB	0dB	-2dB
Quality Factor (Q)	3 to 29	15.4 to 15.8	301 to 114
P_{1dB}	2dBm	-6.6dBm	-8dBm
IIP3	19dBm	2.5dBm	NA
Noise Figure	<5.5dB	15dB	9dB

V. CONCLUSION

In this paper an integrated tunable filter based on N-path periodically time variant networks is implemented and measured. The proposed differential 4-path architecture provides an inductor-less filter with a decade tuning range. The availability of high quality switches in CMOS technology offers high linearity while the simulation and measurement results confirm a low noise operation as well. Although the filter rejection is currently limited to 16dB, the flexible tunability and high linearity are attractive assets for software-defined or cognitive radio applications.

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