“Switched Biasing” reduces both MOSFET 1/f Noise and Power Consumption

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Abstract -**“Switched Biasing” is proposed as a new circuit technique that exploits an intriguing physical effect: cycling a MOS transistor between strong inversion and accumulation reduces its intrinsic 1/f noise. The technique is implemented in a 0.8μm CMOS sawtooth oscillator by periodically off-switching of the bias currents during time intervals that they are not contributing to the circuit operation. Measurements show a reduction of the 1/f noise induced phase noise by more than 8 dB, while the power consumption is reduced by more than 30% as well.**

Keywords -**“1/f noise, noise reduction, CMOS, oscillators, phase noise**

I. INTRODUCTION

CMOS ICs nowadays may contain up to several millions of transistors, mainly used in digital circuits, but also in analog and mixed analog-digital interface circuits (e.g. ADC, DAC, pre- and postamplifiers, up- and downconverters between baseband and RF). As charge transport in electronic devices is fundamentally accompanied by noise, the behaviour of all MOS transistors is subject to these random variations. These random variations ultimately limit the signal processing capability of transistor circuits, as they put a lower limit to the signal that can be processed reliably. Thus noise for instance limits the Signal-to-Noise ratio of analog circuits, resulting in noisy music or noisy TV pictures. In digital transmission systems noise introduces bit errors.

As new generations of deep submicron CMOS processes have higher 1/f noise corner frequencies, 1/f noise is of increasing worry. Moreover, its detrimental effect in circuits is not limited to low frequencies, as 1/f noise can be up-converted to high frequencies, e.g. to phase noise in oscillators [1]. Phase noise close to the carrier is important, e.g. in communication systems with closely spaced channels.

In 1991, Bloom and Nemirovsky [2] published measurements demonstrating that cycling a MOS transistor between strong inversion and accumulation reduces its 1/f noise observed in strong inversion. Shortly after, their results were reconfirmed [3] and related to Random Telegraph Signals. However, for some time this 1/f noise reduction mechanism received no attention in the solid-state circuits community[1].

Recently, the authors showed that the 1/f noise reduction effect is relevant for the analysis of 1/f noise induced phase noise in ring oscillators with standard CMOS inverters [4,5]: about 8dB phase noise reduction was attributed to this effect. In these oscillators, the noise reduction comes for free due to the rail-to-rail switching signals that occur naturally. However, 1/f noise problems exist in a lot of other circuits, in which adequate switching does not occur automatically.

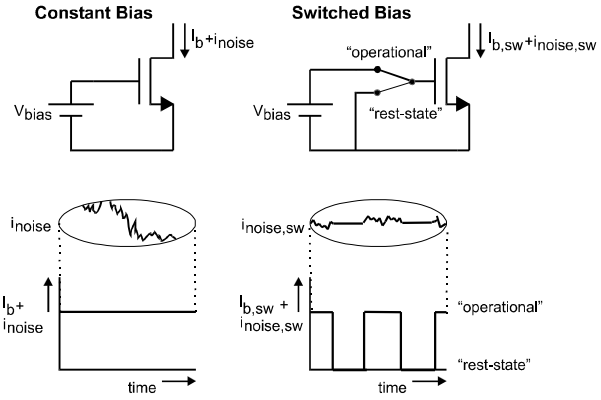

Fig.1: The concept of Switched Biasing

This paper (see also [10]) proposes "switched biasing” as a circuit technique that introduces *intentional off-switching* of MOS transistors, during the time that they are not contributing to circuit operation, with the purpose to *reduce their 1/f noise* in the active-state and *reduce* the *power consumption*[2]. The feasibility and effectiveness of the technique will be demonstrated by an application example in a recently proposed sawtooth oscillator [6] realised in 0.8μm CMOS.

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[1] No references to [2,3] in Science Citation Index ‘91-’97.

[2] Using larger transistors also reduces 1/f noise, but this generally leads to more power consumption to maintain the same speed.

It should be noted that conventional techniques, such as chopping or correlated double sampling, reduce the effect of 1/f noise in electronic circuits, whereas the switched biasing technique reduces the *intrinsic 1/f noise itself*. Loosely speaking, the transistor "forgets" its past and thus related low-frequency noise components. An overview of previous work can be found in the ProRisc proceedings of 1998 [9].

II. Switched Biasing and its Application

Fig.1 illustrates the principle of switched biasing and compares it to constant biasing. Instead of applying a constant gate-source bias, a MOS transistor is periodically switched between two states:

1) an "operational state" or "active state" in strong inversion, in which it contributes to the functional operation of a circuit (e.g. delivers a bias current).
2) a "rest-state" or "inactive state" in -or close to- accumulation, for practical purposes V_{gs}=0 Volt. In this state the MOS transistor is not operational. Apart from saving power, this rest-state is introduced to *reduce the 1/f noise* of the MOS transistor *during its operational* state [2,3,5].

Since 1/f noise is related to long self-correlation times [7], the switching to accumulation can be thought of as a means to reduce this self-correlation by interfering with the long-term memory processes that are responsible for the generation of 1/f noise in MOS transistors (e.g. carrier (de)trapping).
Of course, periodically switching transistors between an operational state and a rest-state is not always possible. However, some circuits offer this freedom, for example because a bias current is *needed* only during certain *time intervals* or because *signal processing is not* taking place *continuously*.

Oscillators are among these circuits: in many types of oscillators, the transistors contribute actively to the circuit's operation during only a fraction of the period of oscillation. This part-time usage of transistors allows for periodical off-switching during non-operational phases. In the next section an example of such an oscillator will be described.

III. The Coupled Sawtooth Oscillator

To enable quick verification of the feasibility of the switched biasing concept, an available 0.8μm CMOS oscillator IC was used, in which 1/f noise induced phase noise is a problem. For clarity, its operation is briefly explained. The oscillator is a controllable relaxation oscillator based on a new principle [6], that allows low phase noise to be achieved in combination with high control linearity. The phase noise of this type of oscillator is significantly lower (14dB) than that of a conventional relaxation oscillator, compared at equal control linearity and power dissipation. This is achieved by using an alternative for the Schmitt-trigger that is used normally in a relaxation oscillator to periodically reverse the capacitor current each time the capacitor voltage crosses one of the tigger's two threshold levels. The noise present on these decision levels is the dominant contributor to phase noise in a conventional relaxation oscillator [8]. This is due to the fast decisions taken by the trigger circuit, resulting in nearly ideal sampling of the threshold-level noise. As a consequence, the threshold-level noise is converted into phase noise over a large bandwidth.

The new coupled sawtooth oscillator [6] uses no schmitt-triggers but rather consists of a ring of identical stages each of which subsequently produces a rising voltage ramp across a capacitor. Its construction is such that only rising edges of the capacitor voltages determine the timing. The *key to the benefits* of the oscillator is that rising voltage ramps are produced by *gradually turning on a capacitor's charge current* instead of instantly, as happens in the regenerative oscillator.

Fig.2 shows the circuit schematic of stage number "n" of a coupled sawtooth oscillator consisting of a ring of six stages and Fig.3 shows the resulting capacitor voltage waveforms. The operation of the circuit is as follows. Transistor M_4 supplies the charge current I_b that is mirrored to become the tail current $I_{b,tail}$ of the differential pair $M_{1,2}$. This differential pair *gradually* starts charging the capacitor with $I_{b,tail}$ as soon as the capacitor voltage in stage (n-1) reaches the vicinity of the bias level V_{REF1}.

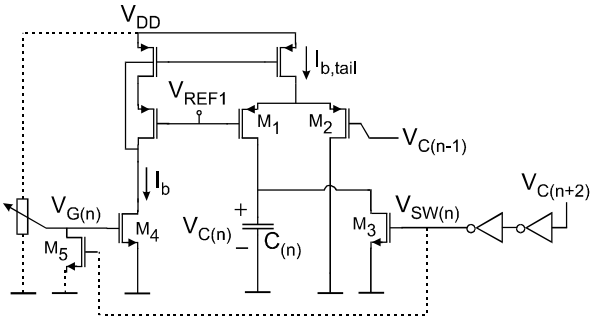

Fig.2: Circuit schematic of section (n) of the coupled sawtooth ring oscillator.

Of course the capacitors should also be discharged. The timing of the discharge is non-critical, as only rising edges are used to couple the individual stages. Transistor M_3, whose gate is driven by two inverters in series, discharges the capacitor during the time that the capacitor voltage in stage (n+2) is larger than the inverter's decision level V_{REF2} (see fig.3). Also shown in fig.3 are the switching signal $V_{SW(1)}$ produced by the inverters that supply the gate voltage of M_3 in stage 1 (see fig.2) and a signal $V_{G(1)}$ to be discussed later.

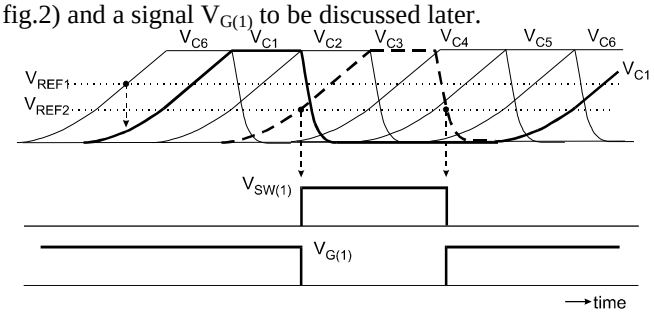

Fig.3: The capacitor voltages of the 6-stage coupled sawtooth oscillator and signals Vsw(1) and VG(1) that are used in stage 1 (see fig. 2 with n=1) to respectively discharge C1 and accomplish switched biasing.

Now, it can be shown [6] that the *gradual start-up* of the charge current *does not* introduce any *deterioration* of the oscillator's *control-linearity*, due to the point-symmetrical transfer function of the differential pair. Moreover, *gradual start-up* leads to low phase noise as the noise, present on the threshold-level V_{REF1} (see figs.4), is effectively *narrowband filtered* due to the *long start-up time* of the ramp (in contrast to wideband sampling of noise by instantaneous switching in a traditional Schmitt trigger based relaxation oscillator).

Fig.4 gives a qualitative time-domain impression of this filtering. Also shown in this figure is the time error Δt_{trig} that would result if a trigger-circuit is used to instantly start a new capacitor voltage ramp. For the same control linearity, its variance is much larger than the variance of the time error Δt_{saw} appearing in the sawtooth oscillator, due to the effective narrowband filtering [6]. The *key point* here is that the *long start-up* time *does not affect control-linearity*, while slowing down a schmitt-trigger to decrease noise bandwidth does affect control linearity.

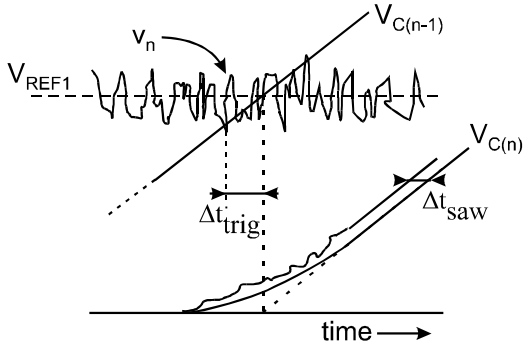

Fig.4: The effective filtering of noise v_n on the threshold level V_{REF1} in the coupled sawtooth oscillator results in a smaller time error Δt_{saw} compared to the time error Δt_{trig} that would appear in a regenerative oscillator.

IV. Switched Biasing Implementation

As a result of the filtering of the threshold-level noise, the (1/f) noise present on the capacitor's charge current now becomes the dominant contributor to (1/f induced) phase noise in the coupled sawtooth oscillator. Thus it is expected that switched biasing helps to reduce the phase noise. The switched-bias technique can be applied to all transistors that contribute 1/f noise to the charge current. The oscillator's operation allows the current $I_{b,tail}$, and thus the 1/f noise contributing transistors, to be switched off when the capacitor in a particular stage is not producing a rising ramp. The easiest way to implement this is to switch off these transistors at the same time when the capacitor is discharged. In this way *no change at all* will be noticeable in the capacitor *waveforms* and the oscillator's timing is not harmed in any way. The signal, necessary to switch the transistors, is supplied by the oscillator itself.

As the capacitor waveforms remain the same, no change in the amount of upconversion of 1/f noise is expected [1]. As a result, any change in the 1/f noise induced phase noise when applying switched biasing *is to be explained by a change in the transistors' intrinsic 1/f noise*.

To enable a quick verification of the switched biasing concept, an 0.8 µCMOS sawtooth oscillator IC which was already available [6] was used as an implementation vehicle. In the experiments to be described, the oscillator stage as shown in fig. 2 was on chip, accessible via extra bond-outs for the capacitor and bias current I_b. The technique is applied to an external current-bias transistor M_4 (see fig. 2, V_{SW1} and M5 implement the switch-of) which is available on the same die as the oscillator circuit. M_4 has a small W/L=4/0.8 such that its 1/f noise dominates in the current $I_{b(tail)}$. Of course this is not optimal for overall 1/f noise minimisation, but the main issue here is to show the feasibility of a technique. To further simplify the experimental setup, the switched bias technique was applied only to one stage. In the other stages, external low noise current sources were used. Note that these simplifications do not undermine the validity of the experimental results, as they could be applied to other current source devices as well.

The dashed lines in fig. 2 show the implementation of the switched biasing in the coupled sawtooth oscillator: transistor M_5 switches off the bias transistor M_4 at the same time when transistor M_3 discharges the capacitor. Fig. 3 shows the gate voltage $V_{SW(1)}$ of transistors M_3 and M_5 in stage 1 together with the resulting gate voltage $V_{G(1)}$ of bias transistor M_4.

V. Experimental Results

In order to characterise the 1/f noise reduction effect for the available 0.8 µCMOS technology, we used the switched-bias measurement setup proposed in [4, 5]. The measured noise spectra for NMOS devices with W/L=4/0.8 are shown in fig.5.

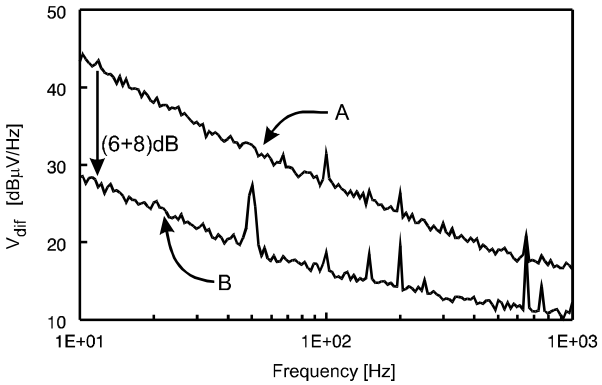

Fig.5: Measured baseband spectra for constant bias (curve A) and switched bias (curve B: f_{switch} = 100kHz, duty-cycle = 50%).

Curve A shows the 1/f noise spectrum measured with the devices constantly biased at a gate-source voltage of 1.5 Volt (V_T = 0.7V), and curve B shows the noise spectrum of the devices switched periodically between 1.5V and 0V with a 100KHz, 50% duty cycle square wave signal. Modelling the switching operation as a simple modulation action, 6dB noise reduction is expected for the 1/f noise in baseband (the overall noise power is halved and divided up in the spectrum around DC and multiples of the switching frequency). However, the

measurements show an *additional* reduction in 1/f noise spectral density of about 8dB at low frequencies, which is in the same order of the results reported in [2,3,4] (spectral peaks are due to 50Hz related interference).

The devices characterised above were used to implement switched biasing in the current source of the sawtooth oscillator, in the way described in the previous section. Due to limitations of the experimental setup, the oscillator is running at a rather low frequency f_{osc} = 120kHz. As expected, the application of switched biasing does not visibly affect the oscillator's capacitor-waveforms observed with an oscilloscope. However, a large difference is measured in the oscillator phase noise shown in fig.6: for switched biasing (curve B) the phase noise at 100Hz carrier-offset frequency is about *8dB lower than for constant biasing*. As motivated in the precious section, this reduction *is to be explained by a change in the transistors' 1/f noise*. Indeed, the amount of reduction is in compliance with the reduction observed in the baseband measurements of fig. 5.

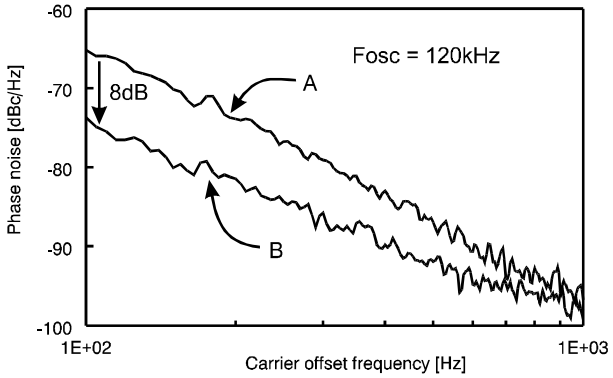

Fig.6: Phase noise [dBc/Hz] of the sawtooth oscillator as a function of carrier offset frequency for the constant bias (curve A) and switched bias condition (curve B): 8 dB reduction is achieved at 100 Hz.

The experiment shows that switching-off a transistor during phases in which it is not actively contributing to the circuit's operation, helps to reduce its 1/f noise during active phases. In addition, the power consumption in stage 1 is reduced by more than 30%.

Although switched-biasing is applied to just one current source in this experimental circuit, it can of course just as well be applied to the other current sources. As all oscillator sections are identical and contribute to the phase noise equally, the same reduction in phase noise is expected in that case.

VI. Conclusions

"Switched Biasing" has been proposed as a new circuit technique. It introduces off-switching of MOS transistors during the time they are not actively contributing to the circuit's operation. This not only saves power, but also reduces the 1/f noise of the switched MOSFETs during active phases. The feasibility of the technique was demonstrated in a 6-stage coupled sawtooth oscillator [6] running at f_{osc} = 120 kHz. Experiments demonstrate the effectiveness of the technique: 8dB reduction of the 1/f noise induced phase noise is achieved, while the power consumption is reduced by more than 30%. The authors believe that switched biasing can be useful to reduce 1/f noise in other circuits that allow for part-time operation of transistors (especially in HF circuits in which upconverted 1/f noise is a problem (mixers, oscillators) and traditional 1/f reduction techniques like enlarging devices or chopping cannot be used).

VII. Acknowledgements

This work was supported by Philips Research Laboratories, Eindhoven, The Netherlands.

VIII. References

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