ANALYSIS OF A CURRENT MODE MOST-ONLY D-A CONVERTER

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Abstract

The subject of this paper is a MOST-only current mode D-A converter. Its topology resembles that of an R-2R ladder. The MOSTs are used to implement both weight factors and switches. Its operation is based on a current division principle [1]. Error sources are identified and analyzed resulting in a fairly simple method to predict achievable performance. Analysis and measurements show 9-bit resolution.

Introduction

In [1], [2] a MOST-only current division technique is described which can be used for D-A conversion. It has the advantages that it results in a compact converter that is both simple in operation and circuit topology. Such a converter could be used for instance in a digital Sea-of-Gates (SoG) environment in which MOSTs are the only available non-parasitic components. This paper focuses on the error sources in this type of converters in order to estimate attainable performance.

Operation principle

The current division (M-2M) D-A converter which topology resembles that of an R-2R ladder utilizes MOSTs to obtain simultaneously binary weight factors and switches. Its operation is based on the current division principle that states the two-transistor network shown in figure 1 is a linear current divider

$$\frac{\Delta I_{D1}}{\Delta I_{D2}} = \frac{W_1/L_1}{W_2/L_2} \qquad (1)$$

as long as drain-dependent effects on the saturated drain current (e.g. velocity saturation) are negligible. Secondly in series and in parallel connected MOSTs may be replaced by composite MOSTs with the respective transconductance factors

$$1/K_{ser} = \sum 1/K_i \,,\; K_{par} = \sum K_i \qquad (2)$$

The MOST look-alike of an R-2R ladder, shown in figure 2, forms the analogue core of the D-A converter. All MOSTs have the same transconductance factor K_u. The MOST M_{term} can be seen either as an actual MOST or as a composite MOST representing the next stage. For proper operation the MOSTs are biased in the linear region, $I_{ref} < I_{D,sat}$ and $V_{sum} = V_{dump}$.

Every stage splits its input current into two equal parts: $I_{i,out} = 0.5I_{i,in} = b_i 2^{-i} I_{ref}$ (MSB: i=1). In an actual converter every stage exhibits an error ε_i, so $I_{i,out} = \beta_i I_{i,in} = (b_i 2^{-i} + \varepsilon_i) I_{ref}$. In order to obtain INL < 0.5 LSB and DNL < 1 LSB

$$\max(|\varepsilon_{sum}|) = \max(|\underline{b} \bullet \underline{\varepsilon}|) = \max\left(\left|\sum b_i \cdot \varepsilon_i\right|\right) < 1/2^{n+1} \qquad (3)$$

Error sources and their influences

There are several non-idealities present in the converter. The errors caused by MOSTs are: some second order effects, mismatch, and noise. The major external error, is an offset voltage between sum and dump. This section presents some general formulas. These can be used to generate curves as those in the diagram of figure 4, that predict the attainable performance. The diagram of figure 4 shows the attainable performance for a converter on the β-array [3] (NMOSTs 11λ/2λ) in the λ = 1.25μm UT-CMOS process and is intended as an illustration.

Second order effects

The dominating second order effect is velocity saturation (violates current division principle). It introduces ε_i's proportional to I_{ref} (see figure 3). The vertical axis scales with gate length of the MOSTs and process. The ε_i's are independent of the number of stages in the converter. Also $|\varepsilon_1| > |\sum \varepsilon_i|$ (i=2,..,n), thus the maximum error will occur at code 100..0. Because of the linear relation between ε_1 and I_{ref} the following relation holds

$$\max(|\varepsilon_{sum}|) = \max(|\varepsilon_1|) = (I_{ref}/I_{D,sat}) \cdot |\varepsilon_{1,max}| \qquad (4)$$

Substitution of this relation in formula (3) yields curve 1 in figure 4. A simple and effective method to reduce errors is to introduce the same non-idealities in both branches of a stage by replacing the output branches by a dummy ladders in the first stages. Curve 2 in figure 4 illustrates this improvement.

Mismatch

The mismatch of a device parameter satisfies a Gaussian distribution. It can be split in a device area and in a separation distance dependent part [4]. The latter is in most cases much smaller than the former, so it is not considered here. Due to biasing, mismatch in transconductance factors is dominant. It can be described by $\sigma^2(K)/K^2 = A_K^2/WL$. ($A_K$ is process dependent) and used to predict variances of β_i's. Assuming their variations are independent a worst-case estimate of ε_{sum} can be made using for instance 3σ-limits. The worst-case situation occurs if successive stages show alternating +/- 3σ errors in combination with an alternating 0-1 input code

$$\max(|\varepsilon_{sum}|) = \tfrac{5}{4} \cdot \delta + \delta^2 + ... \qquad (5)$$

where $\delta = 3\sigma(\beta_i)/2$. and the higher order terms may be neglected. A Monte-Carlo verification showed that in this way $\max(|\varepsilon_{sum}|)$ is slightly overestimated. For the SoG example the result is shown in curve 3 in figure 4.

Offset

An offset voltage, V_{off}, between dump and sum results in a current I_{off}. The ladder is a composite MOST with dump as drain and sum as source, thus $I_{off}(\underline{b}) = -K_n(\underline{b}) \cdot (V_{GS} - V_{th}) V_{off}$. With the superposition principle $K_n(\underline{b})$ can be calculated. It appears $K_n(\underline{b})$ and therefore $I_{off}(\underline{b})$

is maximal for an alternating 0-1 input code. This result was verified with PSPICE. By comparing converters with varying numbers of stages it appears $\max(K_n) \approx K_u\,(n+1)/9$ This leads to the following expression

$$\max(|\varepsilon_{sum}|) = \max\left(\left|\{K(b)(V_{GS}-V_{th})V_{off}\}/I_{D,sat}\right|\right) = \left|\{2(n+1)V_{off}\}/\{9(V_{GS}-V_{th})\}\right| \quad (6)$$

Which is shown in curve 4 of figure 4 for the SoG example in case of V_{off} = 0.5 mV.

Noise

It is expected that the influence of 1/f-noise is much smaller than the influence of thermal noise. Therefore only thermal noise was considered in the analysis. Regarding the ladder as a composite MOST and by allowing thermal noise to be equal to quantisation noise, leads to

$$\left(I_{ref}/I_{D,sat}\right)^2 > 12\cdot 2^{2n}\cdot\left[\tfrac{16}{9}kT(n+1)\Delta f\right]/\left[K_{unit}(V_{GS}-V_{th})^3\right] \quad (7)$$

This relation is shown in curve 5 in figure 4 for the SoG example with Δf = 1 MHz. Clearly in this case it is not a performance limiting factor.

Experimental Results

At the time of writing only a full-custom realisation in a 20nm gate-oxide process with 20µm/20µm MOSTs was available for verification purposes. The limitations imposed by velocity saturation, mismatch, noise and offset as predicted by our method are shown in figure 5. Figure 6 shows the INL obtained from a least square fit on the measured transfer curve at $I_{ref}/I_{D,sat}$ = 450µA/485µA. As can be seen the converter exhibits a 0.5 LSB INL at the 9-bit level. This performance is indicated in figure 5 by the black dot and is in good accordance with prediction.

Conclusions

A fairly simple method to predict the performance of a current mode MOST-only DAC is presented. For a SoG-implementation of the converter this method predicts nearly 8-bit resolution. For a full custom converter it predicts a 9-bit resolution, which is in accordance with measured results.

References

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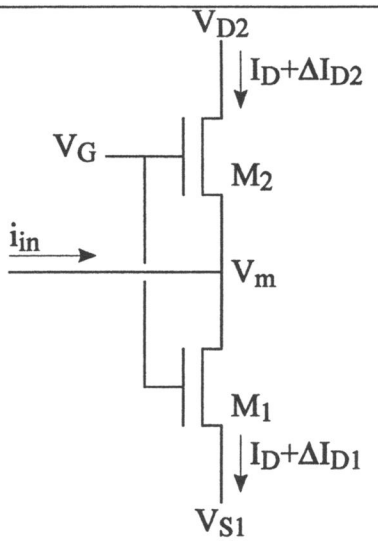

fig. 1 basic current division circuit

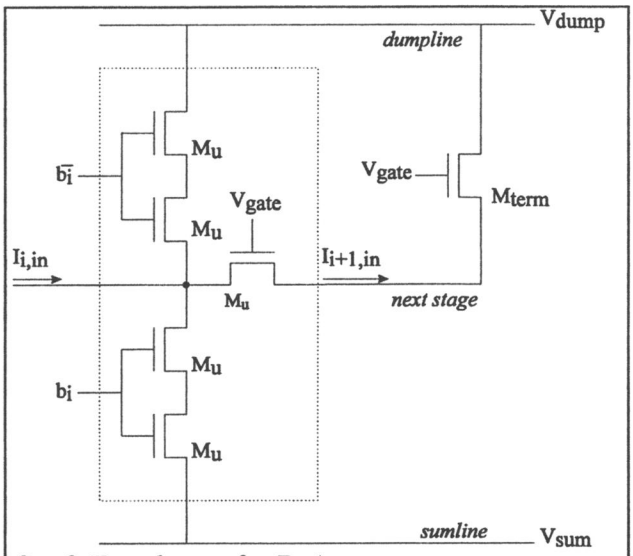

fig. 2 Topology of a D-A converter stage

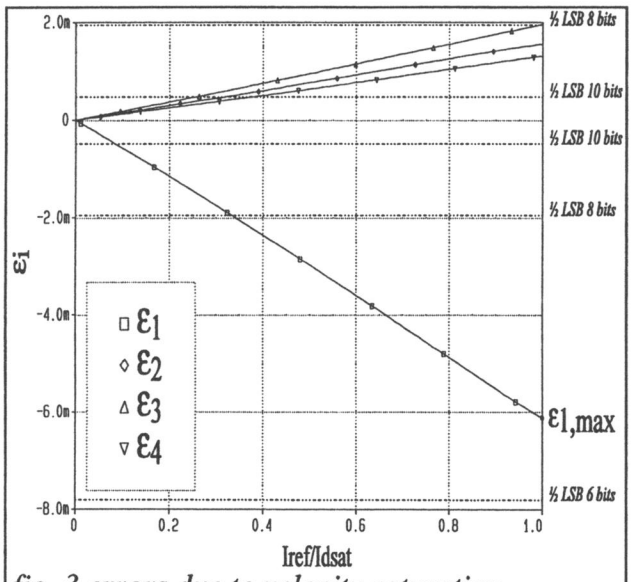

fig. 3 errors due to velocity saturation

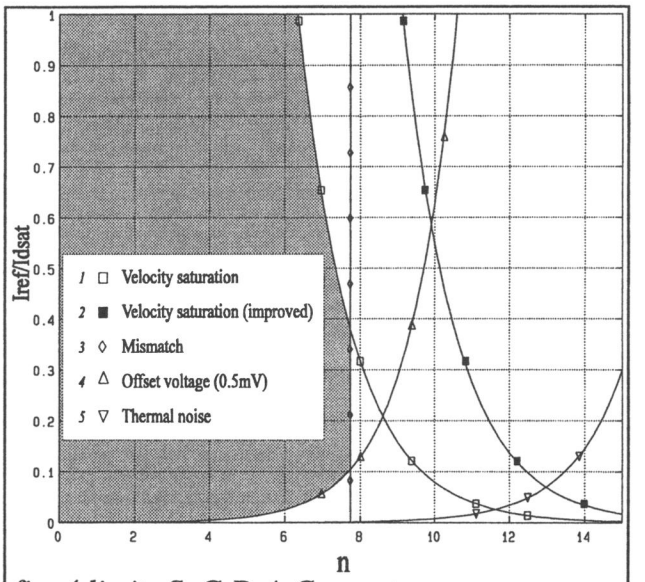

fig. 4 limits SoG D-A Converter

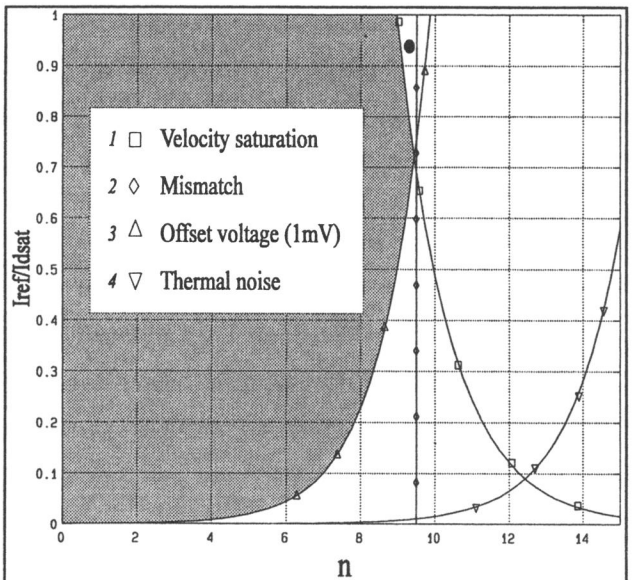

fig. 5 limits full custom D-A Converter

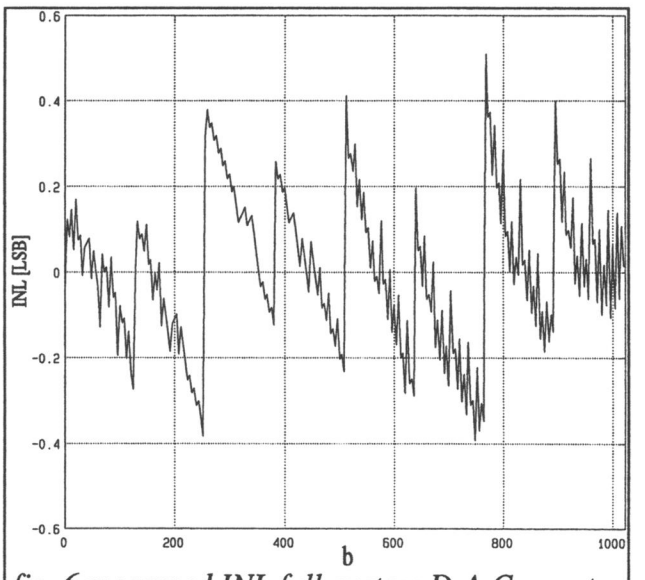

fig. 6 measured INL full custom D-A Converter