Slew Rate Induced Distortion in Switched-Resistor Integrators

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***Abstract*— OPAMP-RC integrators built with linear resistors and capacitors can achieve very high linearity. By means of a switched resistor, tuning of the RC time-constant is possible via the duty-cycle of the clock controlling the switched resistor. This paper analyzes the effect of OPAMP slew rate limitations on the distortion of a switched-resistor lossy OPAMP-RC integrator. We show via analysis and simulations that the use of two sets of switched resistors instead of one relaxes the OPAMP slew rate requirements, and reduces the resulting distortion significantly.**

I. Introduction

OPAMP-RC filters with highly linear passive resistors and capacitors have superior linearity properties for baseband filter applications, if OPAMPs with sufficient gain can be realized. Such filters can be made tunable using resistive or capacitive arrays [1], but this is only practical for coarse tuning. Fine tuning is possible using a MOSFET as variable resistor, and good linearity has been achieved in the past via this approach [2]. However, this requires a gate-source on-voltage which is substantially larger than the input voltage swing, which is impractical in low-voltage deep submicron CMOS processes. For low-voltage conditions a more practical approach is the use of a passive resistor, switched on and off by a clock with tunable duty cycle [3]. Figure 1 shows a simple lossy integrator using such a tuning technique with a single switched resistor. The resistor is in the feedback loop and hardly adds distortion. However, as will be evident, the resulting switching operation poses more stringent requirement on the slew rate of the OPAMP. This paper analyzes the slew rate limitations of the single switched resistor lossy integrator, and the resulting distortion. We also propose a network employing two switched resistors that is less sensitive to slewing problems.

II. Circuit Operation

A lossy integrator with one switched resistor ("Switched-1R") is shown in Fig. 1. The MOS switch before the OPAMP input is alternatingly turned on and off to select whether the current can pass to the capacitor or not. Like a track and hold circuit, it has 2 phases: tracking integration and holding. The variation in the on-time of the switch, determined by the duty cycle of the clock, effectively changes the resistance and hence

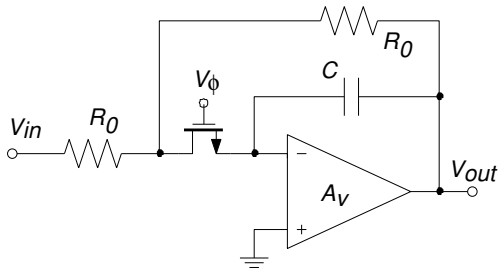


Fig. 1. Switched-1R Lossy Integrator

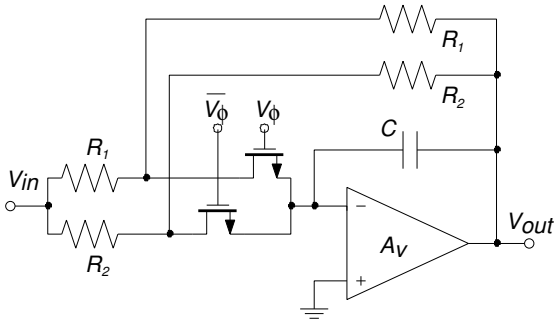


Fig. 2. Switched-2R Lossy Integrator

the lossy integrators cut-off frequency. If m is the duty cycle, then the effective resistance becomes:

$$R_{eff} = \frac{R_0}{m} \tag{1}$$

Thus we can theoretically tune the integrator time-constant between 0 and R_0C. However, in many cases we do not need this large tuning range, but only need about $\pm 20\%$ range to correct for technology and temperature variations, or $\pm 50\%$ to "bridge the gap" between coarse tuning steps. With this in mind, we propose an alternative circuit with two switched resistors (so called Switched-2R) in Fig. 2. If two sets of resistors are controlled by non-overlapping clocks, to realize a time constant ranging from R_1C up to R_2C, it will turn out that this circuit has less sensitivity to OPAMP slew rate problems.

Possible causes of distortion in a switched resistor lossy integrator are the non-linear on-resistance of the MOS switch

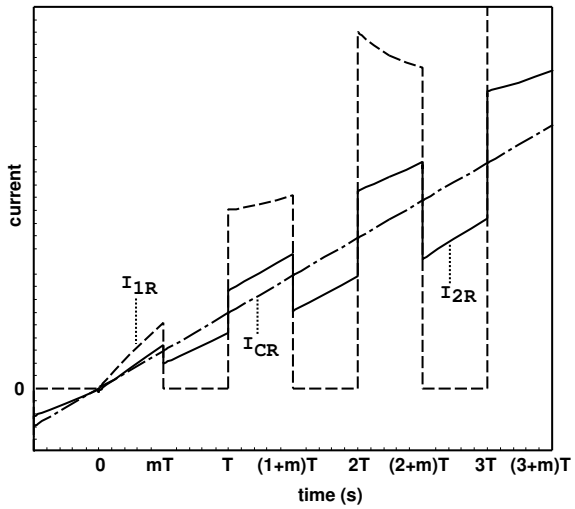


Fig. 3. Capacitor currents of lossy integrators

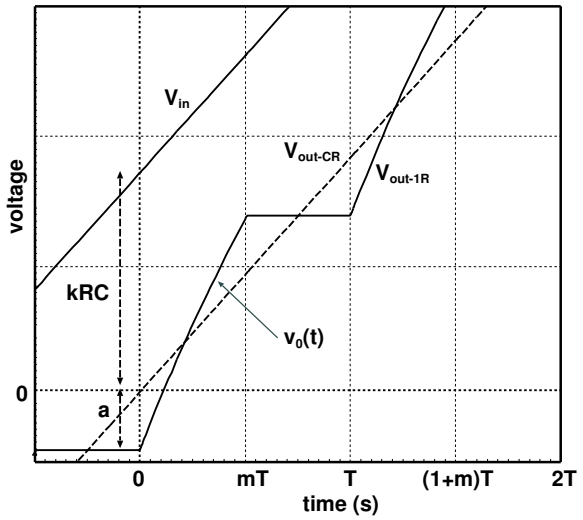


Fig. 4. Switched-1R output voltage response

and OPAMPs non-idealities. As the MOS switch is in series with a much higher linear resistor, while it is also embedded in the negative feedback loop, its non-linearity contribution can be very small. However, the OPAMP may introduce significant distortion, especially if a fast OPAMP response to large input signal changes is needed, and slew limitation occurs in the OPAMP. During slewing, the feedback loop is effectively broken for some time, and it is instructive to predict when slewing occurs, so that its effect can be minimized. We will analyze this in the next section.

III. Slew rate Analysis

A. Qualitative Analysis

It is known that the highest slope in a sinusoidal signal occurs at the zero crossing. So, for the sake of analysis, the input signal can be approximated as a ramp with a constant slope of $V_p\omega_{max}$. We will use a ramp signal to analyze slewing behavior of the lossy integrator. Figure 3 shows the capacitor current of the Switched-1R (I_{1R}) and Switched-2R (I_{2R}) lossy integrators for 50% duty cycle and identical effective time constants. For comparison, the current for a continuous-time integrator I_{CR} is also shown. It should be noted that the average current of the switched resistor circuits must be equal to the current in the continuous-time circuit in order to produce equivalent frequency response characteristics. Since the rate of change of the output voltage, $\frac{dV_o}{dt}$, is the same as the voltage change over the capacitor, this value is also directly proportional to the applied current and inversely proportional to its capacitor value. The capacitor value is fixed, and therefore only the current determines the voltage.

Consider the current plots in Fig. 3. In the Switched-1R case, the MOS switch will conduct current only during the integration phase while there is zero current flow during the hold phase. A larger current is therefore needed in the turn-on stage. On the other hand, Switched-2R has two non-zero current flows depending on whether system is operating in low-value resistor or high-value resistor mode. Hence, we should expect more voltage changes and higher slopes occuring in the Switched-1R case than for Switched-2R. Accordingly, we should also expect the higher OPAMP slew rate requirement for the Switched-1R case.

B. Detailed Analysis

The output voltages of the Switched-1R and Continuous-R integrators are plotted together with the input ramp signal in Fig. 4 (the outputs are inverted for ease of comparison with the input signal). The Switched-1R output voltage response tracks the continuous-time circuit well, except for a sawtooth-like waveform. This is because its average current has to be equal to the continuous-time current as mentioned in the previous section. It can be seen that there is a high slope response in the tracking period and zero slope in the holding period. Finding the maximum slope in the tracking period by considering t = 0 as the starting point, gives the observation that the Switched-1R lags the Continuous-R output by an amount "a" (see Fig. 4). Following this, the response curve within the clock period mT can be considered as the response of a lossy integrator with resistor R_0 value, under the excitation of a ramp input $V_{in} = kt$ and an initial condition at t = 0 of "$-a$". As illustrated in Fig. 4, this is equivalent to the lossy integrator that has been stimulated by a unit-step signal of $(kRC + a)$ magnitude superimposing a ramp signal with slope k within the period time mT. Hence, the complete output response will be the sum of the individual responses to the unit-step and ramp signal together since this circuit is linear and time-invariant system. It can be derived that the output response in the tracking phase (v_0) is

$$v_0 = \Big[(kRC+a)(1-e^{\frac{-t}{R_0C}})\Big]+\Big[kt-kR_0C(1-e^{\frac{-t}{R_0C}})\Big]-a \quad (2)$$

where R is the equivalent resistance equal to the the one used in the Continuous-R and the magnitude of a is a function of duty cycle m and clock period T.

$$a = k\frac{(1-m)T+(R_0-R)Ce^{\frac{-mT}{R_0C}}}{1-e^{\frac{-mT}{R_0C}}}$$

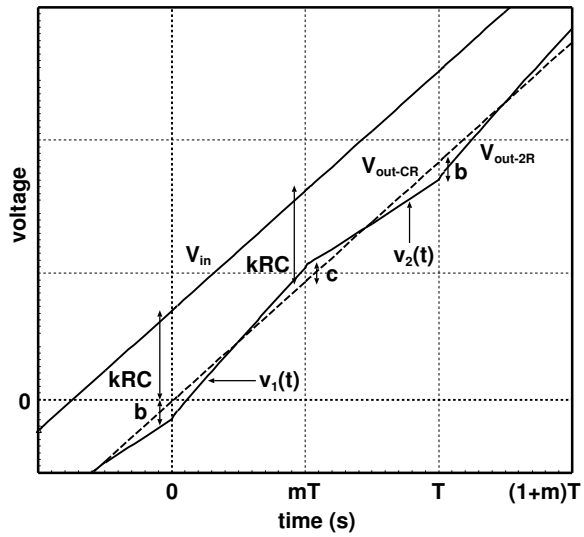


Fig. 5. Switched-2R steady output voltage response

The components in the first square brackets of Eqn. (2) constitute the unit-step response. The second is the response to the ramp and the last term is the initial condition. The maximum slope values of this response, which is determined by finding its derivative, is

$$S-1R \;=\; \frac{kRC+a}{R_0C} \tag{3}$$

The Switched-2R's output response exhibits two slopes as shown in Fig. 5. By assigning resistor value $R_1 < R_2$, the moment t = 0 will refer to the state that R_2 just switches to R_1. At that instant, the Switched-2R response is lower than the Continuous-R response by an amount "b". On the other hand, at the end of time period mT, the output response of the Switched-2R is higher than the Continuous-R by an amount "c". In the same analysis manner as for the Switched-1R, it can be derived that the output response for the low value resistor R_1 phase (v_1) and for the high value resistor R_2 phase (v_2) are:

$$v_1 = \left[(kRC+b)(1-e^{\frac{-t}{R_1C}})\right]+\left[kt-kR_1C(1-e^{\frac{-t}{R_1C}})\right]-b \tag{4}$$

$$v_2 = \left[(kRC-c)(1-e^{\frac{-t}{R_2C}})\right]+\left[kt-kR_2C(1-e^{\frac{-t}{R_2C}})\right]+c \tag{5}$$

where b and c are also functions of m and T.

$$b = kC\frac{(R_1-R_2)e^{\frac{-(1-m)T}{R_2C}}+(R-R_1)e^{\frac{-T}{RC}}+(R_2-R)}{1-e^{\frac{-T}{RC}}}$$

$$c = kC\frac{(R_1-R_2)e^{\frac{-mT}{R_1C}}+(R_2-R)e^{\frac{-T}{RC}}+(R-R_1)}{1-e^{\frac{-T}{RC}}}$$

As a result, the maximum slopes that the OPAMP has to follow will be:

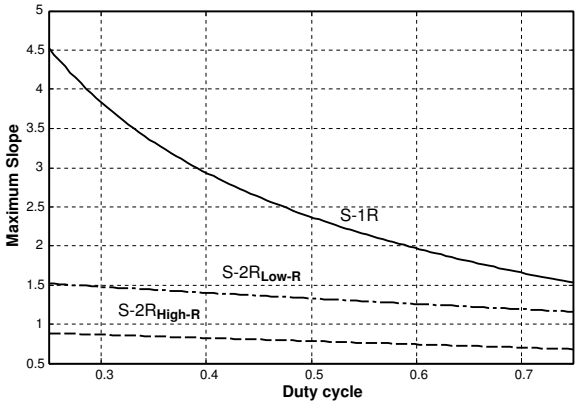
$$S-2R_{Low-R} = \frac{kRC+b}{R_1C} \tag{6}$$

$$S-2R_{High-R} = \frac{kRC-c}{R_2C}e^{\frac{-(1-m)T}{R_2C}}+k(1-e^{\frac{-(1-m)T}{R_2C}}) \tag{7}$$

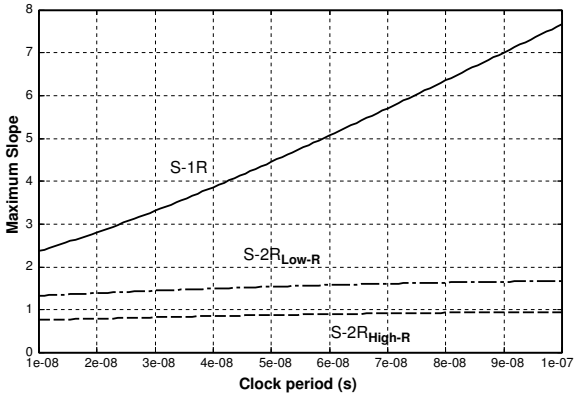
TABLE I

MAXIMUM SLOPE COMPARISON

	m = 0.43		m = 0.5		m = 0.56	
	Math	Sim	Math	Sim	Math	Sim
$S-1R$	4.527	4.518	2.370	2.368	1.527	1.526
	m = 0.25		m = 0.5		m = 0.75	
$S-2R_{Low-R}$	1.521	1.520	1.331	1.330	1.160	1.160
$S-2R_{High-R}$	0.869	0.867	0.760	0.755	0.663	0.656



(a) varied with m (at T=10 ns)



(b) varied with T (at m=0.5)

Fig. 6. Maximum slope variation with duty cycle and clock period

The above equations show the relationship between maximum slope and duty cycle "m" and clock period "T". This relation was verified by comparing the mathematical results with simulation results under the same condition. The maximum input slope, k, is set to 1 for simplicity. The cut-off frequency is chosen to be 10 MHz, consequently yielding capacitor C at 3 pF, R_0 for Switched-1R at 2.5 kΩ, R_1 and R_2 for Switched-2R at 4kΩ and 7kΩ, respectively. Table I shows the results of the two systems by varying m = 0.43, 0.5, 0.56 in Switched-1R and m = 0.25, 0.5, 0.75 in Switched-2R at 10 ns clock period for the same corresponding cut-off frequencies.

The plots of the maximum slope as a function of "m" and "T" are shown in Fig. 6. Fig. 6(a) shows the slope change at varying duty cycles when the clock period is fixed at 10 ns (f_{clk} = 100 MHz) and Fig. 6(b) shows the slope change

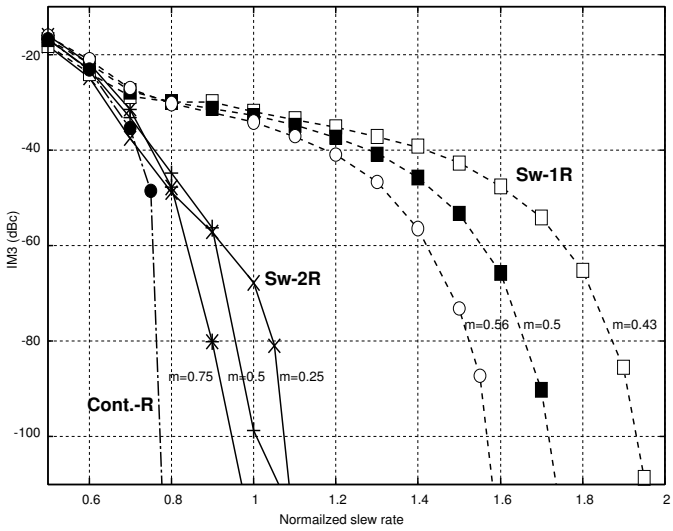


Fig. 7. 3^{rd}-order Intermodulation Distortion

with clock period adjusting when the duty cycle is fixed at m = 0.5. Since the occurred maximum slope for Switched-2R operating with a low valued resistor is always higher than for a high valued resistor, the low-R region determines the slew rate requirement.

Interestingly, when increasing m, the maximum slope becomes smaller and vice versa. This is because when m is increased, more time is spent in the high current period while the low current period is shortened. Therefore, the extra current magnitude in the high current phase, needed for compensating with the low current phase, is smaller and this results in a lower maximum slope. However, since the difference between the current magnitudes in these two phases is larger for Switched-1R, changing m will affect its output response more than Switched-2R.

IV. Simulation Results

Figure 7 shows the third-order intermodulation distortion, IM_3, of the three structures, Switched-1R, Switched-2R and Continuous-R, plotted versus normalized slew rate. The normailzed slew rate is defined as the slew rate value divided by the maximum input signal slope, which is assumed to be the basic slew rate requirement for OPAMP operated in continuous-time mode. It is introduced here in order to enable the systems' performance comparison independent to their applied input signals. An OPAMP analog behavioral model and ideal switch have been used initially to investigate the linearity properties, since their parameters can be effectively controlled [4]. The lossy integrators are configured to have 10 MHz cut-off frequency under 2-tones test of 5 MHz and 6 MHz, 0.4 Vp magnitude, 100 MHz clock frequency and 80 dB OPAMP DC gain. The maximum input slope can be calculated from $V_p\omega_{max}$ = 15.08 V/μs.

From Fig. 7, it can be noticed that the Switched-2R's distortion components drop as fast as for continuous-R while roughly two times more slew rate is needed in the Switched-1R case before the distortion will drop to the minimum level. Changing duty cycle will alter the curves as expected. These results reflect the previous developed equations very well. As can be seen from Fig. 6(a), the maximum slope occurred at m = 0.5 in Switched-2R (1.3) is much closer to the continuous-time (1) than Switched-1R (2.3). Moreover, the larger variation of maximum slope to the changes of m in Switched-1R, also appears in the distortion results. It can be shown that the distance ratios of slew rate requirements between each system in Fig. 7 are quite close to the ratios of their corresponding maximum slopes in Fig. 6(a).

Simulation results of the practical systems using MOS switches and typical two-stage OPAMP circuit also show the same trend. Using OPAMP with 60 dB gain and 18.6 V/μs slew rate produces IM_3 distortion of -57.97 dBc, -54.23 dBc and -48.09 dBc for Continuous-R, Switched-2R and Switched-1R, respectively. Although these values are twice as worse as the ideal model predictions due to the other non-ideal effects, they still possess the similar ratio between each other. All the normalized systems produce the same high distortion level at the slew rate less than about 0.7. In term of noise performance, there is not any considerable difference between all the systems. On the one hand, although Switched-1R utilizes the track and hold operation, it employs the clock frequency much higher than its cut-off frequency so that the noise folding problem will not take effect. On the other hand, Switched-2R does not has any noise folding effect, therefore, this is another advantage over conventional switched-capacitor structures.

V. Conclusion

OPAMP slew rate requirements for switched-resistor lossy integrators have been analyzed. The theory along with simulation results confirm the advantage of using two sets of resistors over one set of resistors in the sense of lowering the required OPAMP slew rate at the same output's distortion level. The tuning range of two sets of resistors can be extended by increasing the difference of the constituent resistors' values, however, it trades with the higher distortion. This gives a more freedom to deal with tunable range and linearity.

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