Theoretical Analysis of Highly Linear Tunable Filters Using Switched-Resistor Techniques

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***Abstract*—In this paper, an in-depth analysis of switched-resistor (S-R) techniques for implementing low-voltage low-distortion tunable active-*RC* filters is presented. The S-R techniques make use of switch(es) with duty-cycle-controlled clock(s) to achieve tunability of the effective resistance and, hence, the *RC* time constant. The characteristics of two S-R networks utilizing one set (S-1R) and two sets (S-2R) of switch and resistor combinations are analyzed. It will be shown that the S-2R network outperforms the S-1R counterpart in terms of finite-slew-rate-induced distortion, frequency translation, and noise performance. In order to extend the tuning range, an S-R bank scheme is also described. The theoretical analysis was verified by an experiment on a 100-kHz first-order S-R filter prototype, implemented using discrete elements, where several advantages of the S-2R over the S-1R networks are demonstrated. Simulations of 10-MHz low-pass filters based on the S-1R and S-2R techniques in a standard 0.18-μm CMOS process are also included for performance comparison in practical on-chip filter implementations.**

***Index Terms*—Cyclostationary noise, duty cycle control, finite-slew-rate-induced distortion, frequency translation, high linearity, linear time varying, low voltage, sampled-data filters, switched-resistor (S-R), tunable filters.**

I. Introduction

RECENT TRENDS in wireless telecommunications have focused on developing reconfigurable systems such as multistandard software-defined-radio transceivers, which are capable of operating a variety of different mobile-communication standards. Since individual standards differ significantly in characteristics like frequency band, signal bandwidth, and modulation type, combining more than one of them into a single receiver leads to demanding tasks. One crucial issue is the ability to define the bandwidth of the channel select filter, which helps in separating the desired channel from the others and from interference. The challenge has arisen because several strong signals may exist within the wide receiving frequency range. These pose a stringent linearity requirement on analog filters, which is difficult especially if a wide tuning range is also needed. The situation is exacerbated by a low-voltage low-power constraint in portable devices as the linearity is further limited.

The continuous-time (CT) active-*RC* filters comprising operational amplifiers (opamps) and highly linear passive resistors and capacitors have superior linearity properties for baseband applications, where opamps with sufficient gain are feasible. Nevertheless, there is a critical issue with these filters, which is the *RC* time-constant variation due to process uncertainty, temperature drift, and aging. In extreme conditions, a maximum variation of $\pm 50\%$ in the 3-dB cutoff frequency is typical in integrated filters. Although this variation can be overcome by making the *RC* time-constant tunable through a digital-trimming weighted resistor or capacitor array [1], [2], high precision tuning may lead to excessive die area.

Typical fine tuning techniques, which accommodate reasonable die size, often use linearized behavior of a MOS transistor operating in triode region as a variable resistor [3], [4], and its linearity can be improved by using a combination of passive resistors and current-steering MOS transistors [5]. However, this kind of tuning technique requires a gate–source on-voltage substantially larger than the input voltage swing in order to achieve an adequate linearity and tuning range. As a result, gate voltage bootstrapping is usually employed in low-voltage applications, but this may affect long-term reliability of circuits due to gate-oxide stress and breakdown. Despite the fact that there are techniques where the gate oxide will not be subject to voltage exceeding the supply-voltage difference [6], [7], they impose an instantaneous higher voltage glitch across the thin gate oxide, and the requirement of variable voltage for tuning could make them more complicated.

The conventional analog sampled-data filters like switched-capacitor (SC) filters, although providing precisely tunable transfer functions and high linearity, also find difficulties to operate at a low supply voltage due to the presence of floating switches in the signal path [6], [7]. Unless, for example, a modification scheme as that has been introduced in [8] is employed, the SC technique necessitates a voltage bootstrapping, thereby incurring reliability issues. As modern deep-submicrometer IC integrations tend to operate at a decreased supply voltage along with the downscaling of transistor dimensions, a suitable tuning approach is to use a combination of passive resistor and switch, which is turned on and off dynamically by a

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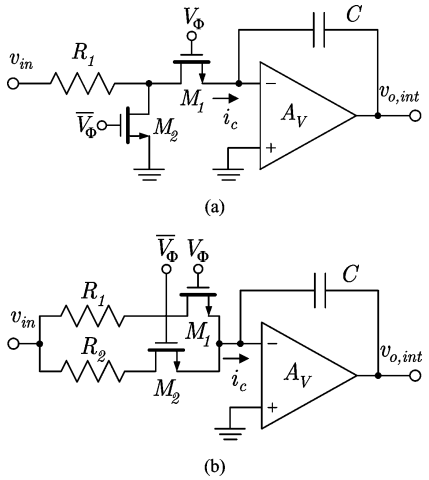


Fig. 1. S-R integrators. (a) S-1R integrator. (b) S-2R integrator.

duty-cycle-controlled clock, for the adjustment of the effective resistance. Such tuning occurs in the time domain, thereby decoupling the tuning ranges from supply voltages. Several circuits employing this variable-timing approach to tune the circuit time-constant or transfer-function coefficients have been proposed [9]–[17]. Among these is the switched-R-MOSFET-C (SRMC) filter in [15], which has recently been demonstrated through a successful chip implementation to offer a high-linearity performance at a supply voltage as low as 0.6 V [16], [17]. The technique essentially employs a linear resistor in series with MOS switches controlled by variable duty-cycle clocks as shown in Fig. 1(a) for its integrator arrangement. As the switches are placed at virtual ground node where the voltage change is kept minimal, they are suitable to be operated within a low-voltage environment. This may be considered as a sampled-data extension of the CT active-*RC* filter. The switching operation based upon one set of the switched-resistor (S-1R) network employed in the SRMC filter, however, poses a stringent requirement on the slew rate of the opamp. One promising modification is to employ two sets of the switched-resistor (S-2R) combination as shown in Fig. 1(b), where it has been shown in [18] via analysis and simulation that the performance of the S-2R networks are less sensitive to slew limitations. Therefore, they offer a relaxed slew-rate requirement of the opamp than their S-1R counterparts.

In addition, switching operation in sampled-data filters causes an aliasing problem, which entails a design complication particularly when signals undergo up and/or down sampling processes along a receiver chain. The S-1R filters also suffer from the aliasing problem similar to the SC filters due to the sampled-data utilization. However, they have no opamp/capacitor settling-time requirements, hence, very high clock frequency can be set to reduce the antialiasing filter specifications [17]. It can be further demonstrated that the S-2R filters have less aliasing components as compared to the S-1R filters, so that the requirements of the antialiasing filter are even more decreased.

This paper presents an extensive performance analysis and comparison of the S-R techniques based on the one-set (S-1R) and two-sets (S-2R) arrangements. The analysis vehicles are the integrator and first-order filter structures, since they are basic elements for higher order filter implementations. Section II describes the principle of operations of the S-1R and S-2R networks along with their finite-slew-rate-induced distortion and tuning-range extension using a resistor-bank scheme. In addition, since the S-R networks are linear time-varying circuits, they possess frequency translation and cyclostationary noise (details of which are also discussed in Section II). Section III provides verifications of the theoretical analysis and comparison through experiments of 100-kHz first-order S-1R and S-2R filters implemented from discrete elements and through simulations of fifth-order elliptic S-1R and S-2R filters using a 0.18-μm CMOS process in Section IV. Finally, the conclusions are given in Section V.

II. Detailed Analysis of S-R Circuits

A. Operation Principle

Throughout the analysis, we will investigate the S-R techniques via the operation of integrator and first-order filter structures as they are representatives of a wider class of filter implementations. An active-*RC* integrator employing one set of switch and resistor, so called S-1R integrator, is shown in Fig. 1(a), where it has two phases: tracking integration and holding. The MOS switches, M_1 and M_2, at the inverting input of the opamp are turned on and off abruptly by the nonoverlapping clocks, V_Φ and $\overline{V_\Phi}$. There will be a current flowing into the capacitor C only when M_1 is conducted in tracking mode, while M_2 steers current to ground when M_1 is off in holding mode [16]. Alternatively, an integrator employing two sets of switches and resistors or S-2R integrator is shown in Fig. 1(b). Unlike the track and hold operation in the S-1R integrator, there is always a signal current charging the capacitor, but the magnitude is dependent on which of the S-R resistor, R_1 or R_2, is conducting. In both cases, the variation of the clock duty cycle effectively modulates the charging currents of the capacitors, which are in turn dependent on the input signal $v_{\rm in}$. As a result, the time constant and the unity-gain frequency of the S-R integrators can be adjusted.

To simplify the description, let us first consider the operation of the S-2R integrator. Assume that the nonlinear on-resistances of the MOS switches are much smaller than the linear passive resistors, and the opamp has a very large gain. The charging current i_c can be written as

$$i_c(t) = \frac{v_{\rm in}(t)}{R_1} \cdot p(t) + \frac{v_{\rm in}(t)}{R_2} \cdot \overline{p}(t) \tag{1}$$

where the resistor value $R_2 > R_1$ is assigned, and the periodic waveforms of the nonoverlapping clock functions toggling between zero and one are

$$p(t) = m + \Phi(m,t) \tag{2a}$$

$$\overline{p}(t) = (1-m) - \Phi(m,t) \tag{2b}$$

where m and $(1-m)$ are the duty cycle, defined as the ratio of on time to clock periods, of the clocks $V_\Phi(t)$ and $\overline{V_\Phi}(t)$, respectively. $\Phi(m,t)$ can be shown in a Fourier expansion form of a squarewave signal with the duty cycle of m

$$\Phi(m,t) = \sum_{n=1}^{\infty} \frac{2}{n\pi} \cdot \sin(mn\pi) \cdot \cos(n\omega_{\rm clk}t - mn\pi)$$

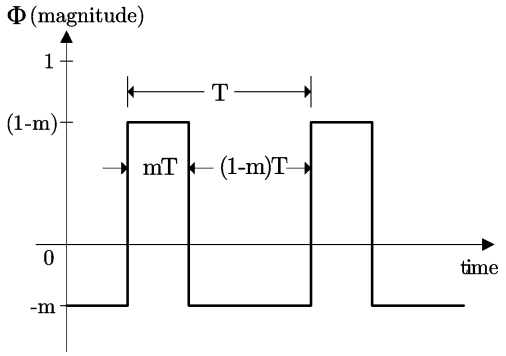


Fig. 2. Waveform of squarewave with varied duty-cycle factor $\Phi(m,t)$.

where $\omega_{\rm clk}$ is the clock radian frequency. A plot of $\Phi(m,t)$ is shown in Fig. 2, where T is the clock period and is equal to $2\pi/\omega_{\rm clk}$. Notice that both timing and magnitude of the waveform depend on the duty-cycle parameter m. That is, whereas the peak-to-peak magnitude of $\Phi(m,t)$ is always unity, the positive and negative peaks vary, yielding a change in the *average* value. This fact will provide a useful insight into the operation of the S-R networks as to be discussed later. Taking the integration of the charging current i_c results in the output voltage

$$v_{o,\rm int}(t) = -\left(\frac{m}{R_1}+\frac{1-m}{R_2}\right)\cdot\frac{1}{C}\cdot\int_0^t v_{\rm in}(t)\,{\rm d}t - \left(\frac{1}{R_1}-\frac{1}{R_2}\right)\cdot\frac{1}{C}\cdot\int_0^t \Phi(m,t)\cdot v_{\rm in}(t)\,{\rm d}t. \quad (3)$$

Note that(1), (2), and (3) are also applicable to the S-1R integrator by simply setting the value of R_2 to infinity.

From (3), if we consider only the baseband characteristic, the second term incorporating the clock function $\Phi(m,t)$ can be neglected. Note that this term will be examined later when we discuss finite-slew-rate-induced distortions, frequency-translation characteristics, and noise performance of the S-R networks. By considering the first component in (3) that represents the integrating function of the input signal, it is clearly seen that the time-constant and the unity-gain frequencies of the S-R integrators in Fig. 1 are dependent on the duty-cycle parameter m and can be written as

$$\omega_{u-1\rm R}(m) = \frac{1}{R_{\rm eq1R}C} = \frac{m}{R_{1-1\rm R}C} \quad (4a)$$

$$\omega_{u-2\rm R}(m) = \frac{1}{R_{\rm eq2R}C} = \left(\frac{m}{R_{1-2\rm R}}+\frac{1-m}{R_{2-2\rm R}}\right)\cdot\frac{1}{C} \quad (4b)$$

where$R_{\rm eq1R}$ and $R_{\rm eq2R}$ are the effective resistances of the S-1R and S-2R integrators, respectively. The unity-gain frequency of the S-1R integrator can be theoretically tuned between 0 and $1/R_1C$, while that of the S-2R integrator is between $1/R_2C$ and $1/R_1C$. This implies that the S-2R arrangement exhibits a narrower frequency tuning range, but it offers higher tuning resolution for the same duty-cycle steps.

The first-order S-R filter incorporating a feedback resistor from the output of the opamp to the input of the MOS switches is shown in Fig. 3. This configuration embeds the nonlinear on-resistance of the MOS switches into a feedback loop, and thus, their nonlinear contributions are further suppressed to be negligibly small [5], [15], [16], [18]. In this case, the output voltage of the first-order S-2R filter can be given as

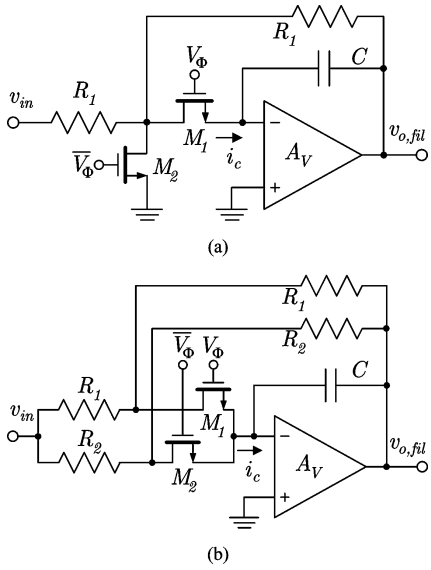


Fig. 3. First-order S-R filters. (a) S-1R filter. (b) S-2R filter.

$$v_{o,\rm fil}(t) = -\left(\frac{m}{R_1}+\frac{1-m}{R_2}\right)\cdot\frac{1}{C}\cdot\int_0^t (v_{o,\rm fil}(t)+v_{\rm in}(t))\,{\rm d}t - \left(\frac{1}{R_1}-\frac{1}{R_2}\right)\cdot\int_0^t \frac{\Phi(m,t)}{C}\cdot(v_{o,\rm fil}(t)+v_{\rm in}(t))\,{\rm d}t. \quad (5)$$

Again, when considering only the baseband operations, the second term containing the clock function $\Phi(m,t)$ is omitted. By using (5), it can be shown that the 3-dB cutoff frequencies of the first-order S-R filters are identical to the unity-gain frequencies of their corresponding integrators as given in (4).

B. Resistor-Value Selection

The choices of the resistor value for R_1 and R_2 in an S-2R filter is important, since there is a tradeoff between the tuning range and the maximum slope of the output, which in turn determines the distortion performance [18]. From (4b), if we select R_2 at x times larger than R_1, the unity-gain frequency of the S-2R integrator can be determined in the form of R_1

$$\omega_{u-2\rm R}(m) = \frac{1+(x-1)m}{xR_{1-2\rm R}}\cdot\frac{1}{C}. \quad (6)$$

Assuming that the nominal frequency has been assigned at the duty cycle of 50%, or $m=0.5$, the tuning range $\triangle f$ of the S-2R integrator derived from (6) is

$$\triangle f_{-2\rm R}(\pm\%) = \frac{(x-1)(m_{\rm max\,/\,min}-0.5)}{1+(x-1)0.5}\times 100\% \quad (7)$$

where $m_{\max/\min}$ is either the maximum or the minimum duty cycle of $\Phi(m,t)$. On the other hand, the unity-gain frequency of the S-1R integrator is directly proportional to the duty cycle as indicated in (4a), so the tuning range will be directly dependent on m as

$$\triangle f_{-1\mathrm{R}}(\pm\%) = \frac{m_{\max/\min} - 0.5}{0.5} \times 100\%. \tag{8}$$

Ideally, the duty cycle can be tuned from 0%–100% for $m = 0.0$ to 1.0, but in practice, the range should be limited because of problems relating to very small or very high duty-cycle clock implementation [15], [16].

The tuning range between these two circuits will have the following relation:

$$\frac{\triangle f_{-1\mathrm{R}}}{\triangle f_{-2\mathrm{R}}} = \frac{x+1}{x-1}. \tag{9}$$

For the same unity-gain frequency $\omega_{u-1\mathrm{R}} = \omega_{u-2\mathrm{R}}$ at $m = 0.5$ and the same capacitor value C, the relation between the resistor values of the S-1R and S-2R integrators is obtained by using (4a) and (6) and this is given as

$$R_{1-1\mathrm{R}} = \frac{x}{x+1} \cdot R_{1-2\mathrm{R}} = \frac{1}{x+1} \cdot R_{2-2\mathrm{R}}. \tag{10}$$

From (7), (8), (9), and (10), since $x > 1 \sim (R_2 > R_1)$, we can conclude that the tuning range of the S-2R integrator is always smaller than that of the S-1R integrator while the resistor values $R_{1-2\mathrm{R}}$ and $R_{2-2\mathrm{R}}$ are always larger than $R_{1-1\mathrm{R}}$, when both circuits are designed for the same ω_u at $m = 0.5$. Note that these tuning-range and resistor-value relations are also true for the first-order S-R filters because they share the same relationship for the 3-dB cutoff frequencies.

C. Distortion Analysis

Since passive resistors and capacitors can be very linear, the main causes of distortion in the S-R circuits are the nonlinear on-resistance of MOS switches and the nonidealities in opamps. The MOS switches are in series with linear resistors, which take most of the input voltage, provided that the on-resistance of MOS switches is chosen much smaller than the (linear) resistor values. Typically, finite DC gain, small-signal bandwidth, and output conductance of the opamp cause only deviations in the transfer function of the S-R filters, as there is no opamp/capacitor settling-time restriction [17]. However, slew rate, which determines the large-signal bandwidth of the opamp, may introduce significant distortion. This is particularly when a fast opamp response to a large input signal change is needed, typical in the operation of sampled-data circuits. During slewing, the feedback loop is effectively broken for some time, and it is instructive to predict when slewing occurs, so that its effects can be minimized [18]. Another potential source of distortion is time-dependent input resistances of the S-R filters, which may arise when the S-R circuits are driven by nonzero-impedance sources, e.g., of a driving mixer at the filters, and of each individual integrator within the S-R filters. These finite resistances, however, are in series with typically much larger linear resistors, hence, their contribution is relatively small. This issue will be investigated further with the help of simulations in Section IV.

To derive the slew-rate requirements for the opamps, we must determine the largest slope of the output that can occur. The rate of change of an output voltage is shown in the form of a slope function $S(t)$, which can be derived by taking the derivative of v_o, $dv_o(t)/\mathrm{d}t$. In the case of integrators, the slope functions can be shown in terms of the unity-gain frequency and the *RC* time constant based on (3), (4), and (10) as

$$S_{1\mathrm{R}}(t) = -\left[\omega_{u-1\mathrm{R}}(m) + \frac{\Phi(m,t)}{R_{1-1\mathrm{R}}C}\right] \cdot v_{\mathrm{in}}(t) \tag{11a}$$

$$\begin{aligned} S_{2\mathrm{R}}(t) &= -\left[\omega_{u-2\mathrm{R}}(m) + \left(\frac{1}{R_{1-2\mathrm{R}}} - \frac{1}{R_{2-2\mathrm{R}}}\right) \cdot \frac{\Phi(m,t)}{C}\right] \\ &\quad \cdot v_{\mathrm{in}}(t) \\ &= -\left[\omega_{u-2\mathrm{R}}(m) + \left(\frac{x-1}{x+1}\right) \cdot \frac{\Phi(m,t)}{R_{1-1\mathrm{R}}C}\right] \cdot v_{\mathrm{in}}(t). \end{aligned} \tag{11b}$$

The second terms in the square bracket containing $\Phi(m,t)$ determine the output slope limits of the S-1R and S-2R circuits. For the same unity-gain frequency ω_u, (11) suggests that, during the positive peak of $\Phi(m,t)$, S-1R integrator always produces higher output signal slope than the S-2R circuit, i.e., $S_{1\mathrm{R}} > S_{2\mathrm{R}}$, since $(x-1)/(x+1) < 1$ for $x > 1$.

The point with the maximum slope $S_{\max}$ can be determined by solving $\mathrm{d}S(t)/\mathrm{d}t = 0$ to find $t_{\max}$ and then substitute this value into (11) to estimate the maximum slope value. For a sinusoidal input signal of $v_{\mathrm{in}}(t) = V_p \sin(\omega_{\mathrm{in}} t)$, the maximum *input current* charging the capacitor occurs periodically at the peak of the input signal, that means at $t_{\max} = ((2k-1)/\omega_{\mathrm{in}})(\pi/2)$ for $k = 1, 2, 3, \ldots$. These points correspond to *zero crossing* points of the *output* voltage. The maximum slope equations can be further simplified by considering the graphical plot of $\Phi(m,t)$ in Fig. 2, which shows that it toggles between only two values: $(1-m)$ and $-m$. For a given unity-gain frequency, the output slope functions in (11) will reach the largest value when the input signal and $\Phi(m,t)$ are at their peaks at the same time. Under such a condition, the maximum slope can be approximated by replacing the input signal $v_{\mathrm{in}}(t)$ with the peak voltage V_p, the function $\Phi(m,t)$ with its highest magnitude at $(1-m)$, and the unity-gain frequency from (4), and this gives

$$S_{\max-1\mathrm{R}} \cong V_p \cdot \left[\frac{m}{R_1 C} + \frac{1-m}{R_1 C}\right] = \frac{V_p}{R_{1-1\mathrm{R}}C} \tag{12a}$$

$$\begin{aligned} S_{\max-2\mathrm{R}} &\cong V_p \cdot \left[\left(\frac{m}{R_1} + \frac{1-m}{R_2}\right) \cdot \frac{1}{C} \right. \\ &\qquad \left. + \left(\frac{1}{R_1} - \frac{1}{R_2}\right) \cdot \frac{1-m}{C}\right] \\ &= \frac{V_p}{R_{1-2\mathrm{R}}C}. \end{aligned} \tag{12b}$$

Interestingly, from (12), the output maximum slopes are independent on the duty cycle m, the input signal frequency ω_{in}, and the clock frequency ω_{clk}. They are determined only by the physical *RC* product and the input signal amplitude. The ratio between the output maximum slopes of the S-1R and S-2R integrators becomes the inverse ratio of their resistor R_1 values. According to the relation in (10), the maximum slope ratio can be simply given by

$$\frac{S_{\max-1\mathrm{R}}}{S_{\max-2\mathrm{R}}} = \frac{R_{1-2\mathrm{R}}}{R_{1-1\mathrm{R}}} = \frac{x+1}{x}. \tag{13}$$

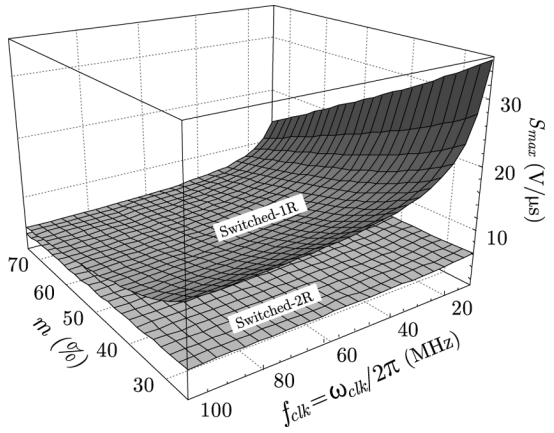


Fig. 4. Maximum slope variation versus clock duty cycle and clock frequency in the first-order S-R filters.

For a case example, for the integrators that have the same nominal unity-gain frequency ω_u of $2\pi \cdot 10$ Mrad/s at $m = 0.5$ and the integrating capacitor of 3.183 pF, we have the resistor $R_1 = 2.5$ kΩ for the S-1R integrator. By selecting the resistor ratio x at two in the S-2R integrator, resistors R_1 and R_2 can be calculated and take the values of 3.75 and 7.5 kΩ, respectively. Calculation of $S_{\max}$ for the input signal with $V_p = 0.1$ V magnitude by using the complete (11) gives a constant maximum slope at about 13.303 V/μs for the S-1R integrator and 8.858 V/μs for the S-2R integrator regardless of the parameters m, ω_{in}, and ω_{clk}, whereas the approximated results from (12) are about 12.567 and 8.378V/μs for the S-1R and S-2R integrators, respectively.

The maximum slope in the first-order S-R filters can be found either by numerical evaluation of (5) or by using an analytical approximation method in [18]. In contrary to the integrators, they are dependent on m, ω_{in}, and ω_{clk}. Fig. 4 shows the numerical plot of the maximum slope $S_{\max}$ in the first-order filters as a function of m and ω_{clk}, based on the same component parameters as the integrator example and a fixed ω_{in} at $2\pi \cdot 5$ Mrad/s. A large variation in the S-1R maximum slope over the tuning parameters is observed, while that of S-2R filter stays almost flat. This demonstrates an important advantage in term of a relaxed slew-rate requirement in the opamp from S-2R circuits.

D. Tuning-Range Extension

Fig. 5 shows plots of the frequency tuning range using (7) and the maximum slope using (12b) of the S-2R integrator versus the resistor ratio x for the duty-cycle variation between 25%–75%, which is typical in practical implementation of the duty-cycle control circuit [15], [16]. For the S-1R integrator, it has a constant tuning range of $\pm 50\%$ and a constant maximum slope of 13.303 V/μs for the same parameters as in Section II-C. Clearly, a larger ratio x results in a wider tuning range, but the maximum slope increases accordingly. Eventually, at a very large x, both the tuning range and $S_{\max}$ approach those of the S-1R counterpart at $\pm 50\%$ and 13.303 V/μs, respectively.

An appropriate means to extend the tuning range while barely touching the maximum slew-rate requirement is to use a resistor-bank scheme. Fig. 6 shows the schematic of the S-2R integrator using two resistor banks. The banks A and B will be operated upon whether the clock signal $V_{\Phi A}$–$\overline{V_{\Phi A}}$ or $V_{\Phi B}$–$\overline{V_{\Phi B}}$

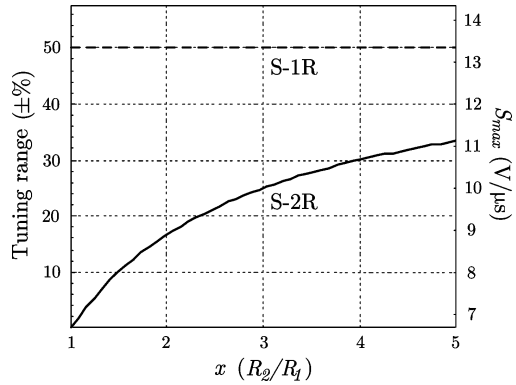


Fig. 5. Tuning range for m between 25%–75% and the maximum slope of the S-2R integrator versus resistor ratio.

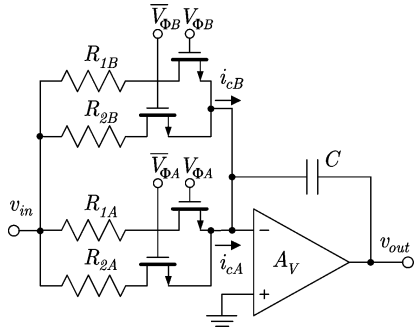


Fig. 6. S-2R integrator using resistor-bank scheme.

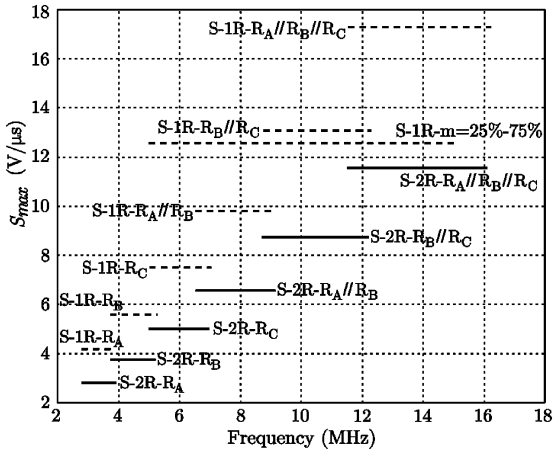


Fig. 7. Tuning range for m between 25%–75% and the maximum slope of the S-1R and S-2R integrators.

is applied. In addition, these two controlling clocks can also be applied simultaneously to execute both of the resistor banks, and in this case, the total effective resistances will become their parallel values. In this way, we can design the resistor banks A and B to have continuous frequency tuning range and then use their parallel operation to further extend the upper frequency limit.

In fact, changing the resistor value will also affect the output maximum slope according to (12). Fig. 7 shows the overall tuning range obtained from the use of three resistor banks in the S-2R integrator, where the resistor order is $R_A > R_B > R_C$, and each of the banks has the ratio $x = 2$. For the sake of comparison, the black dashed line in Fig. 7 shows the tuning range of the single resistor set of the S-1R integrator, where the duty-cycle change is

TABLE I
RESISTOR VALUES FOR THE 10-MHz S-RINTEGRATORS WITH INTEGRATING CAPACITOR OF 3.183 pF

Resistor	S-1R	S-2R		
		bank-A	bank-B	bank-C
R_1	2.5 kΩ	11.0 kΩ	8.25 kΩ	6.19 kΩ
R_2	-	22.0 kΩ	16.5 kΩ	12.38 kΩ

between 25%–75%. The resistors in each bank of the S-2R integrator are designed to have about 10% overlapping frequency to the next bank in order to cover some component variations, and their values are summarized in Table I. It can be seen that the worse output maximum slope occurs when the resistor value is reduced, but the resulting excessive maximum slope per tuning range is much lower than that is obtained by changing the resistor ratio directly in a single bank scheme. Moreover, it gives a total tuning range of nearly $\pm 70\%$ for the adjustment of m between 0.25 and 0.75, while maintaining smaller output maximum slope than that of the S-1R integrator. In other words, for an equivalent tuning range with the S-1R integrator, the resistor ratio x in the S-2R circuit can be reduced, so that a further reduction in the output maximum slope is obtained. Although the resistor-bank arrangement can be used to enhance the tuning range, it also implies that several large-value resistors are required. However, typical wireless systems demand high dynamic range analog filters, in which the area of the capacitors is much larger than that of the resistors. Therefore, the area drawback of the resistor-bank arrangement is not of practical concern in such applications.

Similarly, the resistor-bank scheme is also applicable to the S-1R circuits, where the tuning range and output maximum slope plots of the three-bank S-1R integrator are shown by gray dashed lines in Fig. 7. Note that the duty cycle of each bank is tuned between 42%–59% in order to obtain the same tuning range with the S-2R integrator. Although the output maximum slope curves are lower at low-frequency region, they will exceed the value of the single-bank S-1R integrator (black dashed line) at upper frequency edge, and their magnitude are always higher than that of the S-2R integrator at the same resistor bank.

E. Frequency Translation

Since S-R networks exhibit a periodic time-varying nature, there exists frequency translation of input signals which can give rise to interferences at the output. The most important issue is the down conversion of the inputs outside the baseband frequencies, particularly those with spectral components around the clock frequency and its harmonics. This is because the down-converted signals directly interfere with baseband inputs. To suppress these spurs, it is necessary to include an input prefilter in the S-R network. Although there is also an up conversion of baseband inputs to frequencies near the clock spectral lines, this is not severe because the limited-bandwidth nature of the S-R network itself as well as the prefilter also help suppress such high-frequency interferences. Therefore, the up-conversion analysis is disregarded in this section.

Another issue regarding the frequency translation emerges when the S-R filters operate as an antialiasing filter in front of an ADC. Since the S-1R filters possess a hold phase by nature, its output at this period can be directly fed to the ADC with the same operating frequency. Nevertheless, an S/H circuit is needed in between if the ADC is operated at a different frequency. The S-2R filters, on the other hand, have no hold period, so they always require an S/H operation before the ADC. The resampling mechanism can be investigated by considering a typical output voltage spectrum of an S-R filter (S-1R or S-2R) under a band-limited input shaped by a prefilter in Fig. 8(a). It is evident that the spectrum is shaped by the *sinc* function similar to SC filters. After resampling by an ADC with the same frequency $f_{\rm SH} = f_{\rm clk}$, where $f_{\rm SH}$ is the S/H sampling frequency and $f_{\rm clk}$ is the clock frequency of the S-R filter, the high-frequency components will be aliased down to baseband as shown in Fig. 8(b). It is noticed that the aliased components around the in-band frequency are negligible due to large attenuation of high-frequency output spectrum around the clock frequency and its harmonics, since the spectral notches of the *sinc* characteristic coincide with the clock spectral lines. As a result, in case that the sampling frequency of the ADC is equal to or an integer multiple of $f_{\rm clk}$, the folded to in-band down-conversion signal levels are practically unchanged. On the contrary, these spurs may increase in magnitude if the ADC is not operated at the integral multiples of the S-R clock frequency, so that a more selective prefilter is necessary for suppressing the unwanted signals to the same desired level.

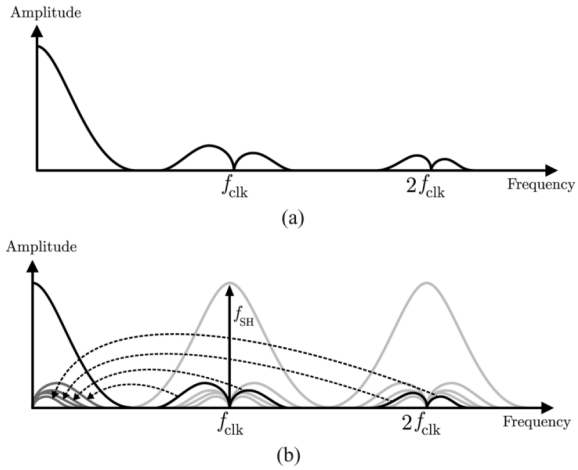


Fig. 8. Output voltage of a resampling S-R filter. (a) Output of the S-R filter. (b) Output after resampling by an S/H at $f_{\rm SH} = f_{\rm clk}$.

The effect of the frequency translation can be analyzed by focusing on the second term of the output-voltage expression for the S-R integrator in (3) involving the product of $\Phi(m,t)$ and $v_{\rm in}(t)$. Recall that this term was omitted in the analysis of the first-order characteristic in Section II-A. For a sinusoidal input $v_{\rm in}(t) = V_p \sin(\omega_{\rm in} t)$ with the peak magnitude at V_p, the second term in (3) yields the output voltage of

$$v_{o,\rm int}(t) = -\left(\frac{1}{R_1} - \frac{1}{R_2}\right) \cdot \frac{V_p}{\pi C} \cdot \sum_{n=1}^{\infty} \left[\frac{\sin(mn\pi) \cdot \cos((n\omega_{\rm clk} - \omega_{\rm in})t - mn\pi)}{n(n\omega_{\rm clk} - \omega_{\rm in})} - \frac{\sin(mn\pi) \cdot \cos((n\omega_{\rm clk} + \omega_{\rm in})t - mn\pi)}{n(n\omega_{\rm clk} + \omega_{\rm in})} \right] \quad (14)$$

where an integer n represents the fundamental clock frequency and its harmonics. By using (14), the voltage conversion gains of the down-converted spur components, i.e., from high frequency $\omega_{\rm in}$ to $n\omega_{\rm clk} - \omega_{\rm in}$, of the S-1R and S-2R integrators can be derived in terms of their corresponding unity-gain frequencies as

$$A_{\rm int-1R} = \frac{\omega_{u-1\rm R}(m)}{|n\omega_{\rm clk} - \omega_{\rm in}|} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right| \tag{15a}$$

$$A_{\rm int-2R} = \frac{\omega_{u-2\rm R}(m) - \omega_{2-2\rm R}}{|n\omega_{\rm clk} - \omega_{\rm in}|} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right| \tag{15b}$$

where $\omega_{2-2\rm R} = 1/R_{2-2\rm R}C$. Similarly, the conversion gains for the first-order S-R filters can be analyzed from the second term in (5), and these are given by

$$A_{\rm fil-1R} = \frac{1}{\sqrt{1 + \left(\frac{n\omega_{\rm clk} - \omega_{\rm in}}{\omega_{u-1\rm R}(m)}\right)^2}} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right| \tag{16a}$$

$$A_{\rm fil-2R} = \frac{1 - \frac{\omega_{2-2\rm R}}{\omega_{u-2\rm R}(m)}}{\sqrt{1 + \left(\frac{n\omega_{\rm clk} - \omega_{\rm in}}{\omega_{u-2\rm R}(m)}\right)^2}} \cdot \left|\frac{\sin(mn\pi)}{mn\pi}\right|. \tag{16b}$$

Note that the 3-dB cutoff frequencies ω_c of the first-order filters are represented by the unity-gain frequencies ω_u of their corresponding integrators for simplicity, since they are identical as mentioned in Section II-A.

By using (15) and the *RC* bank values listed in Table I, plots of the down-conversion gain from high frequency $\omega_{\rm in}$ to the unity-gain frequency $\omega_u(m)$, i.e., under condition $|n\omega_{\rm clk} - \omega_{\rm in}| = \omega_u(m)$ in (15a) and (15b), at $n = 1, 2, 3$, are given in Fig. 9 for both the S-1R and S-2R integrators. This frequency-translation choice usually brings about the strongest interference within the baseband frequency. A duty-cycle change between 25%–75% for each band of the resistor bank is assumed. In the plots, similarity between the variations of the conversion gain for the same m at each resistor bank of the S-2R integrator is noticed. This is because, under the applied condition, the frequency-related coefficients in (15) and (16) are made constant regardless of the choice of the resistor bank, and thus the conversion gain only depends on m and n through the *sinc* function. Also observed from the figure is that the S-2R circuit generally exhibits smaller overall conversion gain, and this is due to the existence of the minus term, $\omega_{2-2\rm R}$, in the S-2R equations [see (15b) and (16b)].

The same plots in Fig. 9 are also representatives of the first-order S-R filters under the condition that the down-converted components are well below their 3-dB cutoff frequencies, $|n\omega_{\rm clk} - \omega_{\rm in}| \ll \omega_c(m)$. In this case, however, the gains will continuously reduce when the down-converted frequency increases and have a 3 dB lower gain at the cutoff frequency, $|n\omega_{\rm clk} - \omega_{\rm in}| = \omega_c(m)$, following the filter characteristic.

Although the clock frequency can be made very high in order to reduce the down-conversion gains as seen from (15) and (16) thereby lowering the order of prefilters [17], it results in higher power consumption and difficulties to implement the duty-cycle-controlled tuning circuit. Fig. 9, therefore, is useful for order selection of the prefilter. For instance, assume that the first-order S-R filters require an in-band signal-to-interference ratio (SIR) better than -40 dB. From Fig. 9, the largest down-conversion gain of the S-1R integrator occurs at

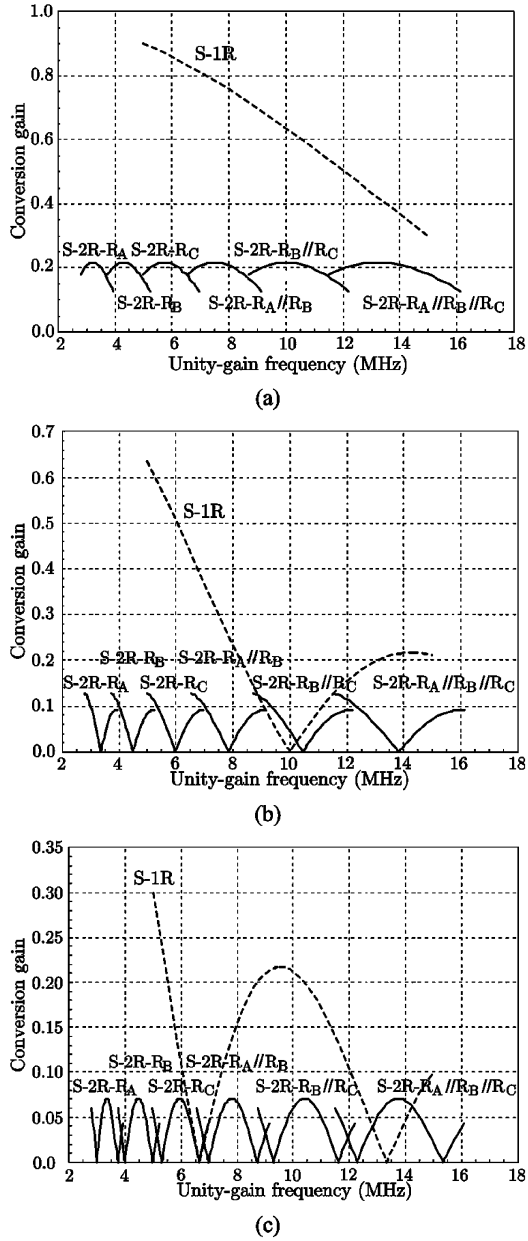


Fig. 9. Voltage down-conversion gains from high-frequency input components around the first few clock harmonics: (a) $n = 1$, (b) $n = 2$, and (c) $n = 3$, to the unity-gain frequency for a tuning range of m between 25%–75%.

$n = 1$ and $m = 0.25$ with a value of 0.902 or -0.89 dB. By including possible cutoff frequency variation at $\pm 50\%$, it can be found that a third-order 20-MHz CT prefilter is required to satisfy the SIR requirement. In the case of the S-2R integrator, the largest gain of 0.217 or -13.27 dB at $m = 0.5$ is found. Since the down-conversion gain is smaller, the prefilter order requirement is reduced to second order for the same 20-MHz cutoff frequency with $\pm 50\%$ variation. It can thus be deduced that the S-2R circuits may require a lower order prefilter with consequent benefits to less complexity and less power consumption.

F. Noise Analysis

An S-2R lossless integrator with two major noise sources, the resistors and the opamp, is shown in Fig. 10. Thermal noise from

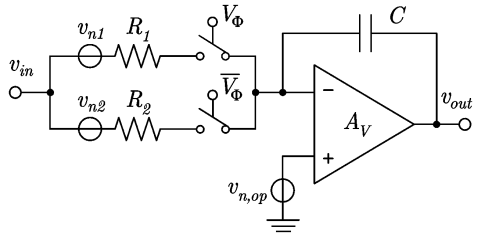


Fig. 10. Noise sources in the S-2R integrator.

the channel conductance g_{ds} of the MOS switches is omitted, since it is negligible as compared to the passive resistors. Flicker noise caused by a nonzero time-varying drain–current in the switches and noise from clock ports are also negligible when the control signals approach squarewave [19], [20]. In addition, jitter from clock signals also produces noise. However, it is negligibly small as compared to noise from resistors and opamp if the clock frequency is well below the gigahertz range. It is worth noting that, since the S-2R circuits have currents flowing through the capacitor C in both switching phases, they possess no hold mode in their operation. As a consequence, they are deprived of noise folding. By contrast, the S-1R circuits incorporate a hold phase, but since their output noise spectrum exhibit bandwidths much lower than the clock frequency, only a small noise portion is folded down from high frequencies to the baseband. This results in negligible noise contribution due to sample-and-hold operation in the S-1R circuits, and it is omitted in the following analysis.

Consider the noise component $v_{n1}(t)$ of the resistor R_1 in the S-2R integrator, which can be considered as wide sense stationary with power spectral density (PSD) $S_{n1} = 4kT_jR_1$, where k is Boltzmann's constant and T_j is the absolute temperature. The noise current due to R_1 that flows into the capacitor C after switching is a cyclostationary noise process

$$i_{c,n1}(t) = \frac{v_{n1}(t)}{R_1} \cdot V_\phi(t) \tag{17}$$

and its time-average PSD is [20]

$$S_{c,n1}(f) = \sum_{n=-\infty}^{\infty} |V_{\Phi,n}|^2 \cdot \frac{S_{n1}(f - nf_{\text{clk}})}{R_1^2}. \tag{18}$$

Since $S_{n1}(f)$ is constant, it can be moved out of summation. After being shaped by the capacitive impedance, the PSD of the output voltage noise power is given by

$$S^o_{n1}(f) = \left|\frac{1}{j2\pi fC}\right|^2 \cdot \frac{S_{n1}(f)}{R_1^2} \cdot \sum_{n=-\infty}^{\infty} |V_{\Phi,n}|^2 = \frac{4kT_jR_1}{(2\pi fR_1C)^2} \cdot m \tag{19}$$

where

$$\sum_{n=-\infty}^{\infty} |V_{\Phi,n}|^2 = \frac{1}{T_{\text{clk}}} \cdot \int_0^{T_{\text{clk}}} (V_\Phi(t))^2 \, \mathrm{d}t = m \tag{20}$$

is the power of the waveform $V_\Phi(t)$.

For the opamp noise which is modeled by an equivalent input referred noise source $v_{n,\text{op}}(t)$ as shown in Fig. 10, it is also cyclostationary due to the periodic switching. By following a similar analysis as earlier, the output noise density from the opamp when the R_1 branch is on can be expressed by

$$S^o_{n,\text{op1}}(f) = \overline{v^2_{n,\text{op}}} \cdot \left(1 + \frac{1}{(2\pi fR_1C)^2}\right) \cdot m. \tag{21}$$

For the output noise contribution from R_2 and the opamp when the R_2 branch is on, the noise expressions are similar to (19) and (21), respectively, with R_2 replacing R_1 and $(1-m)$ replacing m. If uncorrelated noise sources are assumed, the total output noise PSD of the S-2R integrator is given by

$$\begin{aligned} S^o_{n,\text{int}-2\text{R}}(f) &= \frac{4kT_jR_1}{(2\pi fR_1C)^2} \cdot m + \frac{4kT_jR_2}{(2\pi fR_2C)^2} \cdot (1-m) \\ &\quad + \overline{v^2_{n,\text{op}}} \cdot \left(\frac{m}{(2\pi fR_1C)^2} + \frac{1-m}{(2\pi fR_2C)^2} + 1\right) \\ &= 4kT_jR_{\text{eq2R}} \cdot \left(\frac{\omega_{u-2\text{R}}(m)}{2\pi f}\right)^2 + \overline{v^2_{n,\text{op}}} \\ &\quad \cdot \left(\frac{mx^2 + (1-m)}{(1+(x-1)m)^2} \cdot \left(\frac{\omega_{u-2\text{R}}(m)}{2\pi f}\right)^2 + 1\right). \end{aligned} \tag{22}$$

The rearrangement of the noise expression in terms of its equivalent resistor R_{eq2R} and unity-gain frequency $\omega_{u-2\text{R}}$ is also given in (22), where the output noise shaping by the integrator-frequency characteristic is evident. In the case of the S-1R integrator, the total output noise can be simply expressed using (22) by taking the limit for x to infinity, while replacing R_{eq2R} by R_{eq1R} and $\omega_{u-2\text{R}}$ by $\omega_{u-1\text{R}}$, resulting in

$$\begin{aligned} S^o_{n,\text{int}-1\text{R}}(f) &= 4kT_jR_{\text{eq1R}} \cdot \left(\frac{\omega_{u-1\text{R}}(m)}{2\pi f}\right)^2 \\ &\quad + \overline{v^2_{n,\text{op}}} \cdot \left(\frac{1}{m} \cdot \left(\frac{\omega_{u-1\text{R}}(m)}{2\pi f}\right)^2 + 1\right). \end{aligned} \tag{23}$$

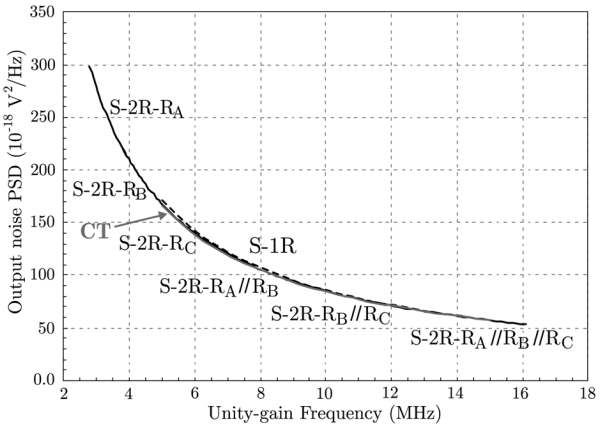
The same analysis procedure can be applied to the first-order S-R filters where the total output noise of the S-2R and S-1R filters are given, respectively, by

$$\begin{aligned} S^o_{n,\text{fil}-2\text{R}}(f) &= 2 \cdot \frac{4kT_jR_{\text{eq2R}}}{1 + \left(\frac{2\pi f}{\omega_{u-2\text{R}}(m)}\right)^2} + \overline{v^2_{n,\text{op}}} \\ &\quad \cdot \frac{\frac{mx^2+(1-m)}{(1+(x-1)m)^2} + 3 + \left(\frac{2\pi f}{\omega_{u-2\text{R}}(m)}\right)^2}{1 + \left(\frac{2\pi f}{\omega_{u-2\text{R}}(m)}\right)^2} \end{aligned} \tag{24}$$

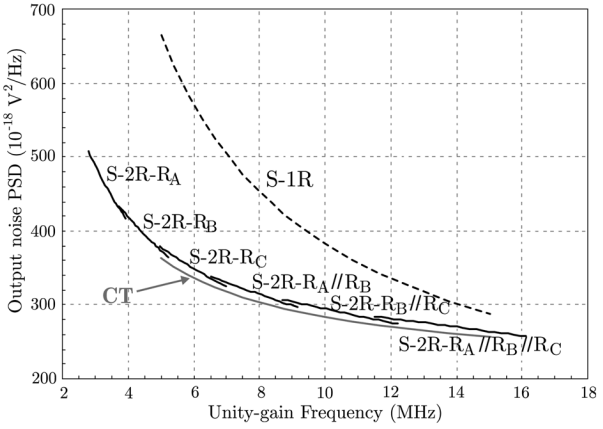
$$\begin{aligned} S^o_{n,\text{fil}-1\text{R}}(f) &= 2 \cdot \frac{4kT_jR_{\text{eq1R}}}{1 + \left(\frac{2\pi f}{\omega_{u-1\text{R}}(m)}\right)^2} + \overline{v^2_{n,\text{op}}} \\ &\quad \cdot \frac{\frac{1}{m} + 3 + \left(\frac{2\pi f}{\omega_{u-1\text{R}}(m)}\right)^2}{1 + \left(\frac{2\pi f}{\omega_{u-1\text{R}}(m)}\right)^2}. \end{aligned} \tag{25}$$

The integrity of derived equations has been verified by the simulations, and their results match well.

By using the parameters in Table I, the plots of the output noise PSD at the unity-gain frequency over the tuning range of both the S-1R and S-2R integrators are shown in Fig. 11. Fig. 11(a) is for the case that the opamp input referred noise is negligibly small as compared to noise from the resistors (at



(a)



(b)

Fig. 11. Output noise PSD of the S-R integrators. (a) Small opamp input referred noise (at one-tenth of resistor noise). (b) Large opamp input referred noise (comparable to resistor noise).

one-tenth of resistors' noise). It can be observed from (22) and (23) that when the opamp's noise is negligible, the total output noise is directly proportional to the equivalent resistance and the unity-gain frequency which are identical for the S-1R integrator and the S-2R integrator. On the other hand, Fig. 11(b) shows the plots when the opamp's noise and the resistors' noise are comparable, and noise performance differences between the S-1R and S-2R integrators can be noticed. This is mainly because of their unequal opamp noise terms in (22) and (23). Note that the output noise PSD of the CT integrators are also shown in Fig. 11, where almost the same result is found for the CT and S-2R integrators.

III. Experimental Results

Three first-order filters based on the S-1R, the S-2R, and the conventional CT circuits were constructed for measurement. The opamp OPA2348, with a dc gain of 98 dB, a gain-bandwidth product of 1.0 MHz, and a slew rate of 0.5 V/μs at a 5-V single supply, was selected. The clock frequency was set to 1.0 MHz unless stated otherwise. By defining the nominal 3-dB cutoff frequency ω_c to 100 kHz with the integrating capacitor C at 150 pF, we may choose the resistors based on available values as listed in Table II.

The resistor value in the S-1R filter was designed to exhibit 100-kHz cutoff frequency when it is operated at 50% clock duty

TABLE II
Resistor Values in the Experimental Board

Resistor	Cont.-time	S-1R	S-2R		
			bank-A	bank-B	bank-C
R_1	10kΩ	5.1kΩ	22.0kΩ	16.5kΩ	12.4kΩ
R_2	-	-	44.0kΩ	33.0kΩ	24.8kΩ

cycle, $m = 0.5$. For the S-2R circuit, the resistor-bank scheme was implemented with the resistor ratio $x = 2$ (Section II-D) to cover the same frequency range of the S-1R circuit for $m = 0.25$ to 0.75. The measured frequency response and tuning characteristics of the first-order S-R filters are shown in Fig. 12. Fig. 12(a) shows the S-1R responses at $m = 0.25$, 0.50, and 0.75 that yield the cutoff frequencies at about 52, 100, and 146 kHz, respectively, which are in good agreement with (4). Fig. 12(b) shows the response of the S-2R filter at the same corresponding cutoff frequencies obtained by selecting the resistor bank to R_A at $m = 0.30$, R_C at $m = 0.65$, and $R_B||R_C$ at $m = 0.30$. The clock spectral lines in the frequency responses for both circuits can be noticed. However, its magnitude is more pronounced in the S-1R case (beyond the upper range of the vertical axis in Fig. 12).

The measured in-band third-order intermodulation distortions (IMD3) for the cutoff frequencies at the nominal value of 100 kHz and the tuned corners at 52 and 146 kHz are shown in Fig. 13 under a two-tone signal, one at the cutoff frequency and the other at 10 kHz below. The distortion curves are plotted against the normalized maximum slope $S_{\max,N}$, which is defined as the maximum rate of change of the input voltage divided by the slew-rate parameter of the opamp. Therefore, $S_{\max,N} = 1$ means that the maximum input voltage change is equal to the slew rate of the opamp. Such a normalization is introduced to enable us to examine the general circuit performance regardless of the slew performance of the employed opamp. It also helps to indicate how large the input rate of change, as compared to the slew rate of the opamp, that the circuits can handle for a given distortion level. It should be noted that $S_{\max,N}$ shown in Fig. 13 is made variable by sweeping the input voltage magnitude for each cutoff frequency.

Considering the IMD3 curves in Fig. 13, we can observe similar distortion levels at a small $S_{\max,N}$, since none of the circuits at all tuning conditions has yet reached the slew limit. Note that the minimum measured distortion level is limited by the resolution of the test equipment. All the curves start to rise when the $S_{\max,N}$ increases, and a rapid growth in the IMD3 of the S-1R filter is evident. Moreover, the distortion of the S-1R filter is larger at $m = 0.25$ or at 52-kHz cutoff frequency (dashed line with square boxes). This is because the output maximum slope of the S-1R filter is inversely proportional to m, as indicated by the theoretical plot of Fig. 4. We found that the measured results of the S-2R filter also give a similar trend as in Fig. 4, where the output maximum slope is less sensitive to m. However, variations in distortion can still be noticed as shown in Fig. 13 when the S-2R filter is tuned to different cutoff frequencies by changing the resistance. This is due to the fact that the output maximum slope is also inversely proportional to the physical *RC* time constant. It should be noted that the distortion is worse when the smaller resistor bank is selected for a

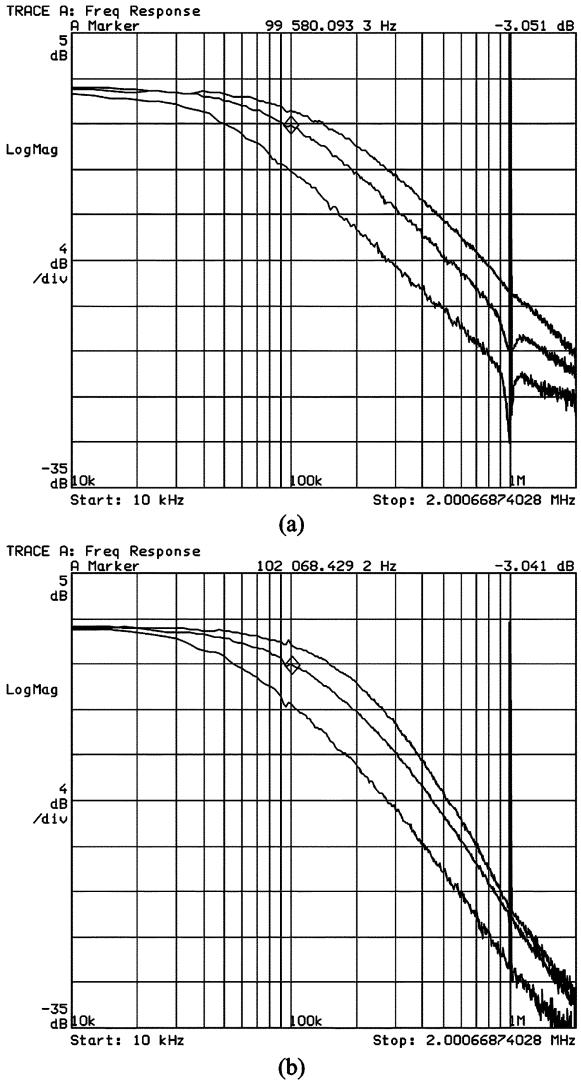


Fig. 12. Measured tuning capability of the first-order S-R filters. (a) S-1R filter. (b) S-2R filter with resistor-bank.

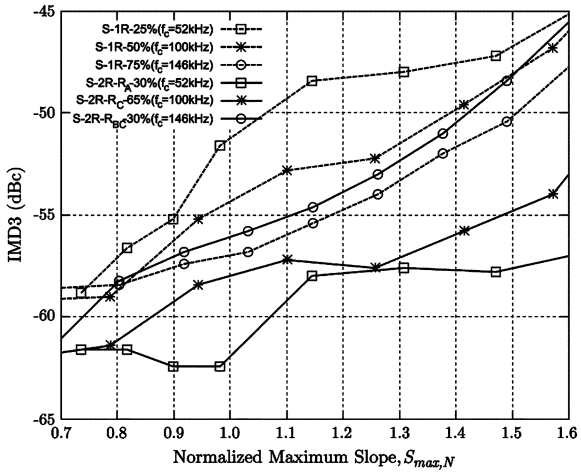


Fig. 13. Measured distortion comparison between the first-order S-1R and S-2R filters at different cutoff frequencies.

higher cutoff frequency (146 kHz or solid line with circles in this case). This is in contrast to the S-1R filter, which obtains

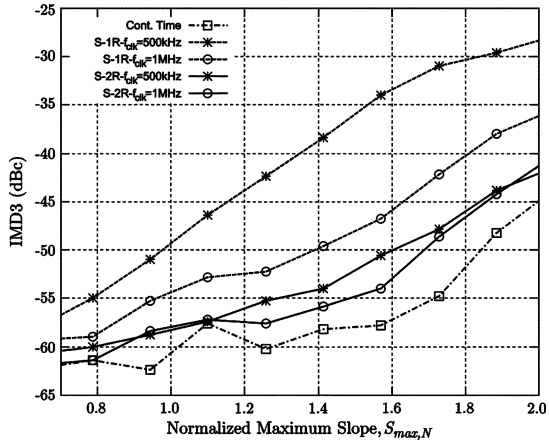


Fig. 14. Measured distortion comparison of the first-order S-R filters at 100-kHz cutoff frequency with clock of 1.0 MHz and 500 kHz.

smaller distortion level when move to a higher cutoff frequency by increasing the duty cycle m. This results in similar distortion performances between the S-2R and S-1R filters at high cutoff frequencies. Nevertheless, the S-2R filter still provides an overall better distortion performance than the S-1R filter. From the plots shown in Fig. 13, at $S_{\max,N} = 1$ or when the maximum input voltage change is equal to the slew rate of the opamp, the distortion level of the S-2R filter is about 3.8 dB lower at 100-kHz cutoff frequency f_c. It is even lower by more than 10.7 dB at $f_c = 52$ kHz, although it becomes 0.9 dB higher than that of the S-1R filter at $f_c = 146$ kHz. This implies that a lower slew-rate opamp may be employed in the S-2R filters, which gives it a possibility for a lower noise and power consumption [21] as compared with that of the S-1R counterparts.

The impact of clock frequency to the distortion performance of the S-R filters as described in Section II-C (see Fig. 4) was also verified by measurement. Fig. 14 shows the measured IMD3 of the S-R filters tuned for a constant 100-kHz cutoff frequency at 1.0-MHz and 500-kHz clock frequencies. The IMD3 result of the CT filter is also included for comparison. It is shown in Fig. 14 that, while the S-1R distortion is degraded by the reduction of the clock frequency $f_{\rm clk}$, the distortion of the S-2R filter remains close to that of the CT filter even $f_{\rm clk}$ is reduced by half. This agrees well with the indication in Fig. 4 that the output maximum slope increases at a lower $f_{\rm clk}$ in the S-1R filter but stays practically constant for the S-2R filter. This shows a potential to operate the S-2R circuits at a lower clock frequency.

The measured voltage down-conversion gains versus translated frequencies for $n = 1$ of the S-R circuits are shown in Fig. 15. The measured conversion gains at the translated frequency closed to dc agree well with the mathematical calculations shown in Fig. 9(a). Also evident in Fig. 15 is that the S-2R conversion gains are always lower than those of the S-1R filter as expected.

The measured output noise for the 100-kHz S-R filters are compared to the calculated plots using (24) and (25), including the noise floor of the equipment in Fig. 16. The calculated plot of the CT filter is also included, and it is almost identical to that of the S-2R filter. The opamp equivalent input referred noise of 35 $\rm nV/\sqrt{Hz}$ [22] was used in the calculations. It is

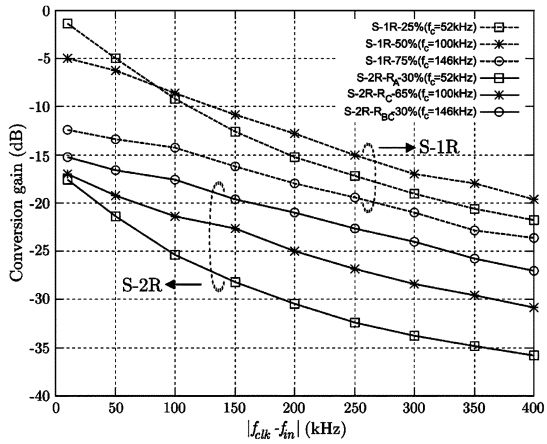


Fig. 15. Measured conversion gains of the first-order S-R filters for $n = 1$.

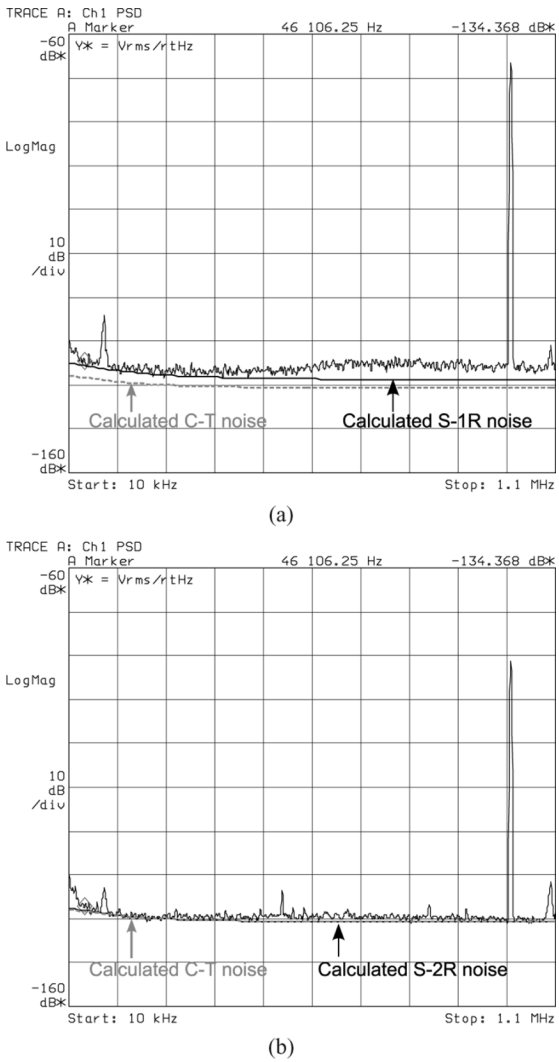


Fig. 16. Measured output noise of the first-order S-R filters at 100-kHz cutoff frequency. (a) S-1R filter. (b) S-2R filter.

shown in Fig. 16 that the S-1R filter produces about 2 dB larger output noise than the S-2R filter. This is because the opamp's noise (35 $\text{nV}/\sqrt{\text{Hz}}$) is comparable to the resistors' noise (25.75 $\text{nV}/\sqrt{\text{Hz}}$). Also noticed is the clock spectral lines

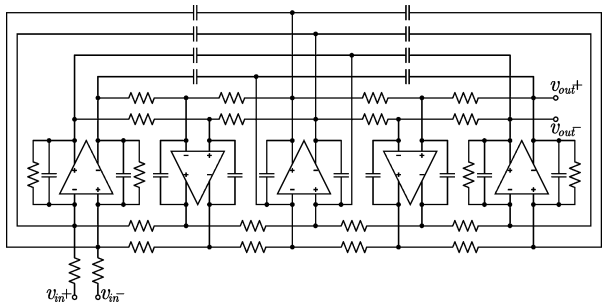


Fig. 17. Fifth-order CT fully differential elliptic low-pass filter.

component at the output of both circuits, and it is more than 10 dB larger in the S-1R filter.

IV. Practical Filter Demonstration

Fifth-order fully differential elliptic low-pass S-R filters were designed to demonstrate the capabilities and synergy of the proposed technique where their CT version is shown in Fig. 17 for reference. The designs are based on a prototype passive *RLC* filter with 10-MHz cutoff frequency, 0.1-dB pass-band ripple, and 50-dB stop-band attenuation. For minimum sensitivity, a leap-frog topology was used. A fully differential two-stage Miller-compensated unbuffered opamp was designed using UMC 0.18-μm CMOS process with 53.2-dB dc gain, 340-MHz unity-gain frequency, 55.7° phase margin, 103-$\text{V}/\mu\text{s}$ slew rate, and 4-$\text{nV}/\sqrt{\text{Hz}}$ input referred noise, under 1.5-V supply and 2.2-mA current consumption. All integrating capacitors are fixed at 3 pF, and the filter resistors are scaled such that the signal amplitude maxima at all opamp outputs are at the same level. Both the CT and S-1R and S-2R filters consume about 17 mW. The effective die size of the filters without tuning circuit are approximated and listed in Table III, where the passive elements were designed using linear metal–insulator–metal capacitors and nonsalicide polysilicon resistors. It is noticed that the capacitors dominate due to high dynamic range design (the third-order spurious free dynamic range of about 62 dB) typical for wireless applications, and the resistors and MOS switches take a negligible area as compared to the overall circuit. Therefore, the area disadvantage of the S-2R filter is not an issue in this case.

The simulated frequency responses of the fifth-order S-R filters under 100-MHz clock frequency are shown in Fig. 18. Besides the frequency response of the filters, we can also observe large clock components in the S-R filters. It should be noted that the S-1R and the S-2R filters with the resistor bank were configured to have a comparable tuning range similar to Fig. 7 within the duty-cycle change between 25%–75%. Fig. 19 shows the simulated output noise of the S-R filters together with that of the corresponding CT filter. The output noise is dominated by $1/f$ noise from the opamp at low frequencies and the white noise from the filter resistors near the pass-band edges. The observed $1/f$ noise corner frequency is about 700 kHz.

The simulated in-band third-order input intercept points (IIP3), out-of-band IIP3, and integrated input referred noise of the CT and the S-R filters are summarized in Table III. The simulation results were obtained from the nominal cutoff frequency $f_c = 10$ MHz and its $\pm 50\%$ tuning edge, i.e., 5

TABLE III
SIMULATED (IIP3) AND INPUT REFERRED NOISE

5^{th}-order filters	C-T	S-1R	S-2R
In-band IIP3 [dBm]			
• Fixed two-tone†			
- f_c = 5 MHz	38.56	31.74	38.97
- f_c = 10 MHz	38.99	35.72	38.16
- f_c = 15 MHz	38.49	38.05	37.50
• Varied two-tone‡			
- f_c = 5 MHz	38.56	31.74	38.97
- f_c = 10 MHz	35.77	30.50	34.39
- f_c = 15 MHz	32.54	30.33	31.04
Out-of-band IIP3 [dBm]			
• Varied two-tone§			
- f_c = 5 MHz	43.30	29.02	43.55
- f_c = 10 MHz	34.47	27.22	32.73
- f_c = 15 MHz	29.25	26.44	27.56
Noise* [μV rms]			
- f_c = 5 MHz	194.7	248.0	198.8
- f_c = 10 MHz	222.3	255.1	231.5
- f_c = 15 MHz	248.9	262.0	255.8
Effective area [μm^2]			
- Opamps	13,500	13,500	13,500
- Capacitors	33,200	33,200	33,200
- Resistors	36	78	193
- MOS switches	0	18	104

† : two-tone is fixed at 2.49 MHz–2.50 MHz
‡ : two-tone is varied, one at half of the cutoff frequency f_c and the other at 10 kHz apart
§ : two-tone is varied, one at 30 MHz and the other at 62.5 MHz, 65.0 MHz or 67.5 MHz
* : Input-referred, differential, integrated over 100 kHz to f_c

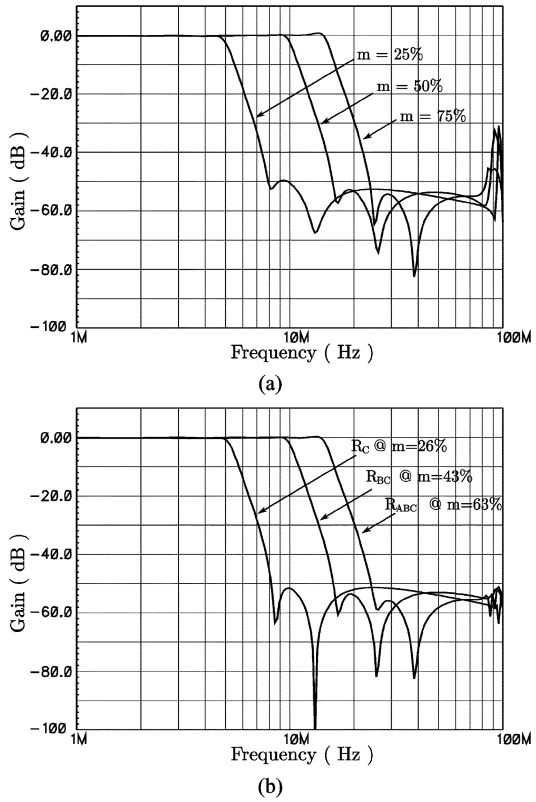


Fig. 18. Simulated frequency response of the fifth-order S-R filters. (a) S-1R filter. (b) S-2R filter with resistor bank.

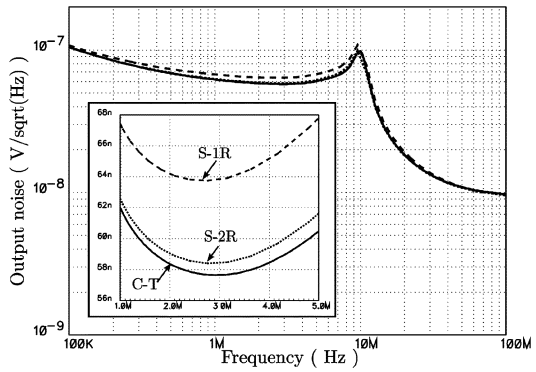


Fig. 19. Simulated output noise of the fifth-order elliptic filters.

and 15 MHz, under 100-MHz clock frequency. Note that the cutoff frequency in the CT filter was tuned by directly scaling all resistors in the filter.

The in-band IIP3 simulations were performed at two conditions. The first results were taken from a fixed in-band two-tone signal at 2.49 and 2.50 MHz for all cutoff frequencies f_c, and the other were taken when one tone was set to $f_c/2$ and the other tone was at 10 kHz apart. The simulation results of these two cases are also plotted together as shown in Fig. 20(a). In the first condition where the input maximum voltage change is fixed, the IIP3s of the S-2R filter are almost identical to that of the CT filter, and they are nearly unchanged for all f_c. This implies that the designed opamp's slew rate is adequate to handle the output voltage change at these fixed frequencies over the whole tuning range. On the other hand, the IIP3s of the S-1R filter are typically lower than the others due to the larger excessive output voltage change, which causes slew limitation, particularly at low f_c. Since the excessive output voltage change is inversely proportional to the duty cycle m as discussed in Section II-C, the IIP3 of the S-1R filter is comparable to those of the other filters at only the upper tuning frequency edge. For the second condition, the two-tone test signal was moved up to the half of each f_c, so that the input maximum voltage change would also increase. The IIP3s of the S-2R filter and the CT filter are again almost identical, and they are reduced for increasing f_c. This is because the increased input maximum voltage change at higher f_c are beyond the opamp's slew capability. In case of the S-1R filter, the IIP3s also tend to reduce due to the increase of the maximum input voltage change. However, they are partially compensated by the lowering of the excessive output maximum slope of the S-1R filter at larger duty cycle m, hence the overall IIP3s stay nearly unchanged with f_c.

For out-of-band IIP3 simulations, one input tone was fixed at 30 MHz and the other tone was selected at the frequency which yields the third-order intermodulation component at the half of its corresponding f_c, i.e., at 62.5, 65.0, and 67.5 MHz for $f_c = 5$ MHz, 10 MHz, and 15 MHz, respectively. Fig. 20(b) shows the comparison plots of the simulation results. They show similar trend to the in-band IIP3 at variable two-tone tests. However, distortion performance of the S-1R filters is degraded significantly in this case.

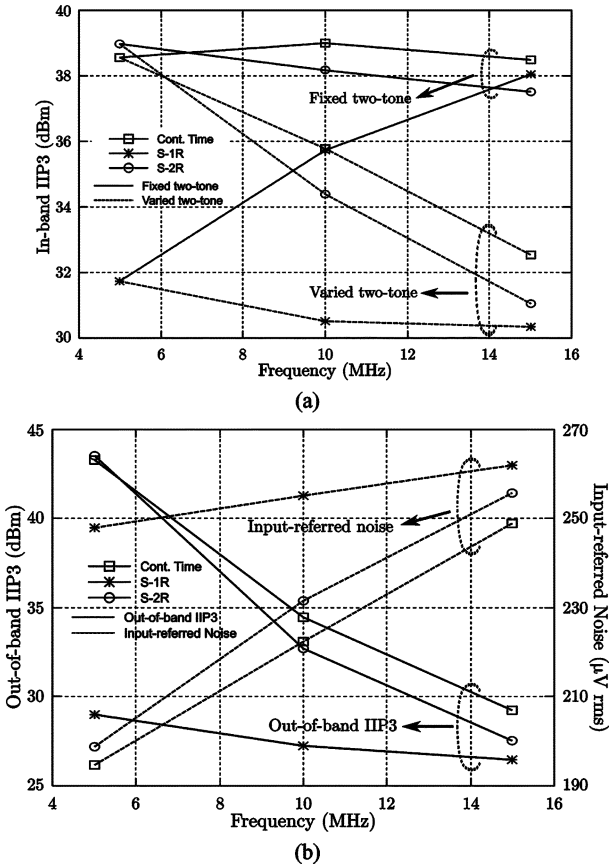


Fig. 20. Plots of the simulation results in Table III for 100-MHz clock frequency. (a) In-band IIP3. (b) Out-of-band IIP3 and input-referred noise.

To study the effect of the time-dependent input resistances, distortion simulations were also performed with the nonzero source impedance up to 1 kΩ, and this resulted in only a gain reduction while the frequency response and distortion performance are virtually unchanged. Moreover, it can also be deduced that the time-dependent input impedance at each individual stage has negligible effect on the distortion since the S-2R filters can achieve a linearity close to the CT filters as shown in Table III.

The simulated input referred noise of the filters is the integrated value over 100 kHz to the corresponding f_c, and the comparison plots are also shown in Fig. 20(b). The resulting noise in the S-1R filter is slightly higher than the others particularly at low f_c as a result of the opamp's noise as discussed in Section II-F.

V. Conclusion

We have presented a detailed analysis of S-1R and S-2R S-R techniques, which allow for high-linearity low-voltage tunable filters. The operating principle and several imperfections such as finite-slew-rate-induced distortion, frequency-translation characteristic, and noise performance of the S-R circuits have been studied. Experimental results of the first-order S-R filters follow the theoretical predictions very well and confirm the advantages of the S-2R filters over the S-1R filters in terms of the following: 1) lower slew-rate requirement of the opamp thereby reducing power consumptions; 2) lower magnitude of frequency-translation components so does the prefilter order necessity; and 3) lower noise in some certain applications where the low-noise opamp is not available. Performance comparison in practical applications was shown through the simulations of the fifth-order elliptic low-pass filters. Both the experimental and simulation results demonstrate that the S-2R technique provides a cutoff-frequency tunability under low supply voltage while offering comparable performances to the CT active-*RC* circuits.

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