Regular Brief Papers

A CMOS OTA for HF Filters with Programmable Transfer Function

Eric J. van der Zwan, Eric A. M. Klumperink, and Evert Seevinck

Abstract—**A CMOS OTA for programmable HF filters is presented. When used in an OTA-C integrator, the unity-gain frequency phase error remains less than 0.3° for frequencies up to more than one tenth of the OTA bandwidth. Since this phase error is preserved over the G_m range of the OTA, the OTA is suitable for filters with a programmable transfer function.**

I. Introduction

SEVERAL CMOS OTA's suited for the design of filters have been reported [1]–[5]. The poles and zeros of these filters are defined by the unity-gain frequencies $f_{ug} = G_m/(2\pi C_L)$ of OTA-C integrators (G_m is the transconductance of the OTA and C_L is its load capacitance). Usually G_m is tunable over a sufficient range to compensate for process- and temperature-dependent errors. However, the tunability of G_m can also be used to implement programmable filters [6], [7], which will be the scope of this paper.

It is well known that filter properties are extremely sensitive to integrator phase errors at f_{ug} [1], [8]. Since these phase errors generally depend on processing and temperature variations, a phase correction scheme ("Q control") is needed [2]. If the integrators in a filter are identical to or are scaled versions of a "master integrator," one control loop can control the phase of all integrators via a "master–slave" concept. However, since the phase error generally also varies when G_m is tuned, only simultaneous tuning of f_{ug} of all integrators is then possible (e.g., [3]: a low-pass filter with programmable cutoff frequency).

The OTA presented in this paper has a built-in phase compensation, which allows tuning of G_m while maintaining a small phase error. In a filter built with such OTA's, independent programming of f_{ug} of the individual integrators becomes possible. This enables programming of not only the filter cutoff frequency, but also of the transfer function itself.

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II. Operation of the OTA

The OTA to be presented is derived from the transconductor shown in Fig. 1(a), which was proposed in [9]. All back gates are connected to ground (NMOS) or to the positive (PMOS) supply voltages. The transistors operate in saturation and are characterized by the simple first-order model:

$$I_d = k(V_{gs} - V_T)^2 \qquad \left(k = \frac{\mu C_{ox}}{2}\frac{W}{L}\right). \tag{1}$$

As explained in [9], the differential pairs M_1/M_2, M_3/M_4, and M_5/M_6 operate as attenuating voltage copiers, copying input voltage v_{in} to V_{gs7} and V_{gs8} with different signs, but with the same offset V_c. This scaled copy of v_{in} is converted to a linear differential current by square-law devices M_7 and M_8. By means of current mirror M_{15}/M_{16} this differential current is transferred to the output. Using (1) and assuming $M_1 = M_2$, $M_3 = M_4 = M_5 = M_6$, and $M_7 = M_8$, the transconductance of the OTA can be calculated:

$$G_m = \frac{i_{out}}{v_{in}} = 4k_7\sqrt{k_1/k_3}\,(V_c - V_{T7}). \tag{2}$$

Equation (2) shows that G_m is electronically variable by means of V_c. Since V_c must be high enough to keep the lower tail-current sources $2I_0$ operating, V_{gs7} and V_{gs8} are rather high. This is unfavorable for the dc gain and power consumption of the OTA. To decrease the effective gate–source voltage of M_7 and M_8, transistors M_9 and M_{10} were added in series with them (see Fig. 1(b); the tail currents $2I_0$ of the differential pairs are provided by source V_0 and M_{11}–M_{14}).

For linear operation of the OTA, the stacked transistors M_7/M_9 and M_8/M_{10} must operate as square-law

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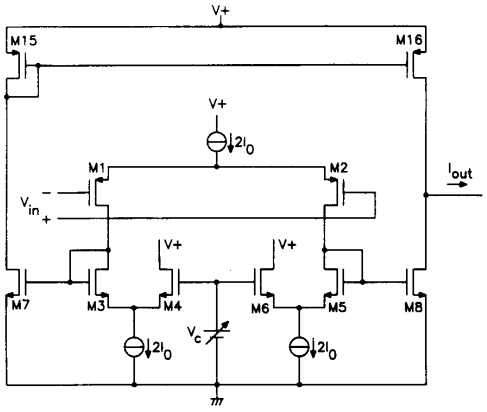
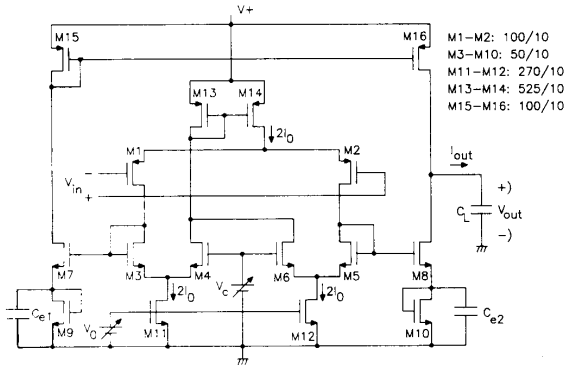


(a)



(b)

Fig. 1. (a) OTA proposed in [9]. (b) Modified OTA using stacked square-law transistors.

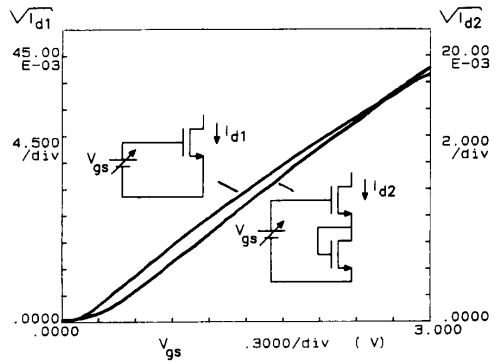


Fig. 2. $\sqrt{I_d}$ versus V_{gs} of a single 50/10 NMOS transistor compared to a stacked pair of 50/10 NMOS transistors: the stacked pair has a better square-law behavior for $V_{gs} = 0.6$–3 V.

voltage-to-current-transducers. In Fig. 2 the square root of the measured drain current of a stacked pair of equal transistors and a single transistor are compared. A straight line would indicate a perfect square-law behavior. Careful inspection of the curves shows that the stacked pair approximates this ideal situation better than a single transistor. This can be understood as follows. Using the square-law model (1), the drain current of the stacked pair is calculated as

$$I_{d7} = k_{eq}(V_{g7} - V_{s9} - V_{Teq})^2 \tag{3}$$

with

$$k_{eq} = \frac{k_7}{\left(1 + \sqrt{k_7/k_9}\right)^2}$$

and

$$V_{Teq} = V_{T7} + V_{T9}.$$

Equation (3) is a square-law relation similar to (1). An analysis of second-order effects reveals that mobility reduction is the most important cause of deviations from the square-law model. Because $V_{Teq} > V_T$ and because voltage $(V_{g7} - V_{s9} - V_{Teq})$ is distributed over two transistors, these deviations are smaller for the stacked pair than for a single transistor operating at the same voltage. Although V_{T7} is significantly enlarged by the body effect, the variation in V_{T7} due to v_{in} has a negligible effect on the drain current when compared to deviations caused by mobility reduction. Furthermore, since $k_{eq} < k_7$ and $V_{Teq} > V_{T7}$, the drain current of the stacked pair is significantly smaller than for a single transistor operating at the same voltage. This improves the dc gain and power consumption of the OTA.

III. Phase Compensation

An ideal integrator would have a phase shift of $-90°$ at f_{ug}. In a practical OTA-C integrator the finite bandwidth of the OTA will cause excess phase shift while the finite dc gain causes phase lead. For high unity-gain frequencies, the phase lag dominates the phase error. This excess phase shift can be compensated by a zero that is introduced by capacitors C_{e1} and C_{e2} parallel to M_9 and M_{10} (see Fig. 1(b)).

An analysis of the phase error at f_{ug} of the OTA of Fig. 1(b) loaded with a capacitor C_L was carried out. Transistors were modeled by g_m, g_{ds}, C_{gs}, C_{db}, and C_{sb} (assuming $M_1 = M_2$, $M_3 = M_4 = M_5 = M_6$, $M_7 = M_8 = M_9 = M_{10}$, $M_{11} = M_{12}$, $M_{13} = M_{14}$, $M_{15} = M_{16}$). Assuming $\arctan(\omega\tau) \simeq \omega\tau$ (error $\leq 1\%$ for $\omega\tau \leq 0.2$), the phase

error at f_{ug} can be approximated by

$$\Delta\phi(\omega_{ug}) = -4\frac{C_x}{C_L}\frac{k_{eq}}{k_3}\frac{V_c - V_{Teq}}{\sqrt{I_0/k_1}} - \frac{2C_{gs15}+C_{db15}}{C_L}\sqrt{\frac{k_{eq}}{k_{15}}\frac{k_1}{k_3}} + \frac{\lambda_7/2+\lambda_{15}}{4\sqrt{k_1/k_3}}(V_c - V_{Teq}) + \frac{C_e}{C_L}\sqrt{\frac{k_{eq}}{k_7}\frac{k_1}{k_3}} \quad (4)$$

with

$$C_x = \tfrac{1}{2}C_{gs3} + \tfrac{1}{2}C_{gs7} + C_{db1} + C_{db3} + \tfrac{1}{4}C_{db11} + \tfrac{1}{2}C_{sb3}$$

$$C_e = C_{e1} = C_{e2}.$$

λ is the channel length modulation parameter $(dI_d/dV_{ds})/I_d$. The first term of (4) is the excess phase shift due to the pole of the transconductor caused by parasitic capacitances at the gates of M_3 and M_5 [9]. The second term is caused by current mirror M_{15}/M_{16}. The third term is the phase lead due to the finite dc gain of the integrator, and the fourth term is the phase lead caused by the zero that is introduced by the compensation capacitors C_{e1} and C_{e2}.

When C_e is suitably chosen, the phase error for a nominal value of V_c can be eliminated by means of I_0 (4). f_{ug} of the integrator can be tuned by adjusting V_c. As the first and the third term of (4) are proportional to $V_c - V_{Teq}$, this results in variation of the phase error. The variation in the first term of (4) can be eliminated by making $\sqrt{I_0}$ proportional to $V_c - V_{Teq}$, which means that $V_0 - V_{T11}$ should be proportional to $V_c - V_{Teq}$. This can be done without affecting the G_m of the OTA [9, eq. (2c)]. The remaining phase error variation is caused by the variation in the third term of (4), which in fact equals $1/A_0$ [rd] (A_0 representing the dc gain). This variation can be acceptable for an OTA with sufficient dc gain. For example, the phase error variation for A_0 varying from 40 to 60 dB will be $\pm 0.25°$.

The ratio between $V_0 - V_{T11}$ and $V_c - V_{Teq}$ for optimum phase compensation depends on temperature and technology variations. However, it will be equal for matched integrators on the same chip. This means that the optimum ratio needs only to be established once for a group of identical integrators (one "Q-control" circuit). When applying this ratio to the individual integrators, independent programming of f_{ug} of individual integrators is possible, while maintaining a low phase error.

IV. Experimental Results

For quick evaluation of the above theory, the OTA of Fig. 1(b) was fabricated on our analog CMOS array (ACMA) in the UTCMOS process ($V_{TN} = 0.15$ V, $k_N = 40\ \mu A/V^2$, $V_{TP} = -0.4$ V, $k_P = 14\ \mu A/V^2$). The supply voltage was 5 V and the input voltage was at a 2.5-V common level. Depending on V_c and V_0, the OTA power dissipation was 1–5 mW. For G_m fixed at 210 μS, the nonlinearity error was below 1% for a 1-V_{pp} input voltage. A G_m range of 74–280 μS is obtained for a 0.5-V_{pp} input voltage with less than 1% nonlinearity error. The THD at 1 kHz was below 0.2% over this G_m range, increasing to 0.4% at 1 MHz. A larger G_m range is possible at the cost of a lower input voltage swing and vice versa. This is

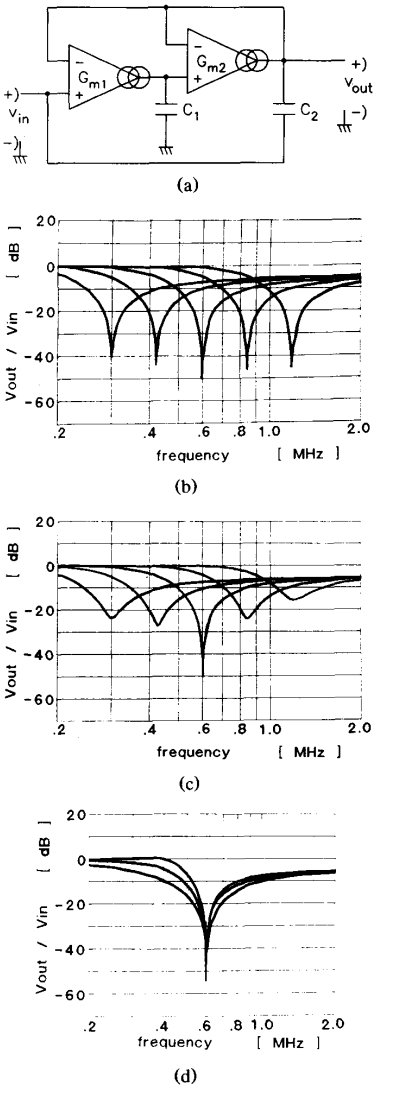


Fig. 3. (a) Second-order notch filter. (b) Frequency characteristics of the filter for V_0 tracking V_c according to $(V_c - V_{Teq})/(V_0 - V_T) = 3.2$. (c) Idem for a constant $V_0 = 0.64$ V. (d) Idem for constant $G_{m1}G_{m2}$ and $Q = 0.5$, $Q = 1$, and $Q = 2$.

because $V_c - V_{Teq}$ must be larger than $\sqrt{k_1/k_3}|v_{in}|$ to keep $M_7 - M_{10}$ in strong inversion (equations (2), (3)).

The measured short-circuit bandwidth of the OTA was 5–8 MHz (depending on V_0). The resulting phase shift was compensated by $C_{e1} = C_{e2} = 10$ pF. The residual phase error was examined by building and measuring a notch filter (Fig. 3(a)). It can be shown [8] that for small phase errors $\Delta\phi$, the transfer of this filter at the notch frequency ω_0 is

$$|H(j\omega_0)| = \frac{2}{|Q_{int}|} = 2|\tan(\Delta\phi)| \qquad (5)$$

The filter of Fig. 3(a) was breadboarded using OTA's fabricated on ACMA and with $C_1 = C_2 = 32$ pF. For correct phase compensation the $(V_c - V_{Teq})/(V_0 - V_T)$ ratio was kept constant at 3.2. Fig. 3(b) shows the amplitude characteristics of the notch filter for several equal values of G_{m1} and G_{m2} $(Q = \sqrt{G_{m1}C_2/G_{m2}C_1} = 1)$.[1] A notch frequency range of 300 kHz to 1.2 MHz is achieved. The notch is always below -40 dB, which means that the phase error is less than 0.3° (equation (5)). Without phase compensation this notch depth would only be achievable for frequencies up to approximately 1/200 of the OTA bandwidth (≈ 40 kHz instead of 1.2 MHz). Fig. 3(c) shows what happens if $V_0 - V_T$ is constant instead of proportional to $V_c - V_{Teq}$: the notch depth rapidly decreases when G_m deviates from its optimum value, which confirms the effectiveness of the phase compensation. In Fig. 3(d) independent programming of G_{m1} and G_{m2} is shown, thus varying the transfer function. The product $G_{m1}G_{m2}$ is kept constant, so that the notch frequency is fixed and Q varies from 0.5 to 2. Again the notch depth remains more than 40 dB.

V. Conclusions

An OTA suitable for HF filters with a programmable transfer function has been proposed. By using stacked square-law transistors the linearity, dc-gain and power-consumption properties of the OTA are improved. Compensation capacitors keep the phase error at f_{ug} of an OTA-C integrator smaller than $\leqslant 0.3°$ up to more than one tenth of the OTA bandwidth. Moreover, by making bias voltage V_0 of the OTA suitably dependent on G_m-control voltage V_c, this phase error remains low even when G_m is varied.

The maximum achieved f_{ug} was limited to 1.2 MHz mainly because no transistors with shorter channel length than 10 μm were available. Furthermore, the tuning of the transconductance and phase compensation was performed manually. Further research has to be done to explore the possibilities of automatic tuning and the extension to higher frequencies.

[1] Breadboard parasitics cause a capacitance C_3 from the output of the filter to ground. Therefore the high-frequency output level is not 0 dB, but $C_2/(C_2 + C_3)$.

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