Achieving Wideband sub-1dB Noise Figure and High Gain with MOSFETs if Input Power Matching is not Required

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***Abstract* — A 0.18 µm CMOS Low Noise Amplifier (LNA) achieves sub-1dB Noise Figure over more than an octave of bandwidth without external noise matching components. It is designed for a future radio telescope, requiring millions of cheap LNAs mounted directly on phased array antenna elements. The short distance between antenna and LNA and low frequency below 2GHz allows for using an LNA with reflective input impedance, increasing the gain with 6dB. Without any matching network, very low noise figure is achieved over a wide bandwidth. At 90mW power, sub-1dB Noise is achieved for 50Ω source impedance over a 0.8-1.8GHz band without external coils, and S21>20dB, OIP2>25dBm and OIP3>15dBm. Preliminary results with 150 Ω source impedance show noise temperatures as low as 25 K around 900 MHz.**

***Index Terms* — Low Noise Amplifier, CMOS, Wideband Amplifier, Phased Array, radio receiver, radio astronomy.**

I. Introduction

Deep submicron MOSFETs can achieve a minimum noise figure NF_{min} well below 0.5dB for low GHz frequencies [1], equivalent to a noise temperature below 35K. Thus MOSFETs are becoming a viable alternative for ultra low-noise applications and are even considered for future radio astronomy applications, traditionally the domain for cryogenic cooled LNAs. This paper reports simulated and measured results of a CMOS LNA designed to push the limits, aiming at the lowest possible noise over more than an octave bandwidth for a 100mW power budget. The LNA is designed for a "Square Kilometer Array" (SKA), a phased array antenna system with millions of antenna elements to achieve 100 times more sensitivity than the best telescope today. To achieve this sensitivity, high gain amplifiers with very low noise are attached directly to antenna elements, which means that millions of LNAs are needed. To realize such a system at reasonable costs, the use of low-cost mainstream technology is planned with antennas realized as printed circuits and CMOS LNAs mounted on them, preferably without any further external components. These boundary conditions make this paper also relevant for other low-cost wideband phased array applications.

In this paper we focus on a SKA-LNA for the 0.6-1.6GHz band. To achieve the desired sensitivity, the LNAs should have a NF<0.6dB in combination with a gain of at least 20dB to suppress the noise contributions of later stages sufficiently. Given the relatively low frequency, the LNA will be close enough to the antenna to neglect standing wave phenomena. Thus there seems to be no strict reason to require input impedance matching of the LNA to the antenna impedance, and a high ohmic highly reflective input impedance could be acceptable. However, output impedance matching is needed, as the LNA needs to drive a long 50Ω transmission line to a beam former, which will phase shift and combine multiple antenna signals of the phased array. In the wide 600-1600MHz band several strong interferers can occur, so both good 2nd and 3rd order linearity is desired.

This paper will discuss the design and experimental verification of a CMOS LNA aiming at wideband ultra low noise. Section II discusses LNA design considerations, motivating the choice for a reflective input impedance and high antenna impedance. Section III presents a 0.18µm CMOS circuit design. Experimental results are reported in section IV, while conclusions are drawn in section V.

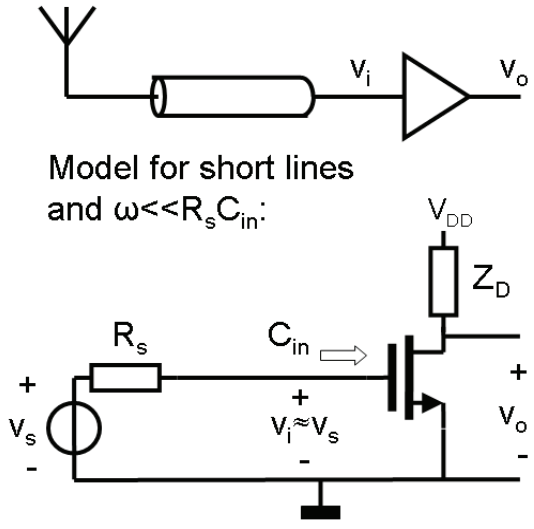

Fig. 1. Highly simplified Antenna with MOSFET LNA working in the low GHz range, mounted directly on an antenna element

II. LNA Design Considerations

Assuming the LNA is mounted close enough to the antenna elements and we don't require input impedance matching, we can exploit a common-source MOSFET with large transconductance and high drain impedance Z_D (see figure 1) to simultaneously obtain very large gain and very low noise.

Assuming $\omega<<1/(R_sC_{in})$, the full source voltage v_s will be available at the gate, instead of $v_s/2$ in case of impedance matching. This renders 6dB more gain, reducing the noise contribution of later stages. Moreover, the usual trade-off between impedance matching and noise matching is avoided, allowing to push the noise figure to very low values. Technology extrapolations predict a minimum NF_{min} decreasing with Moore's law [1]: at 2GHz and a current density of 100µA/µm gate-width, NF_{min} drops from roughly 0.4dB for a 0.25µm technology to 0.1dB for a 50nm technology. However, note that this minimum is only achieved at an optimum source impedance with a large resistive and inductive component.

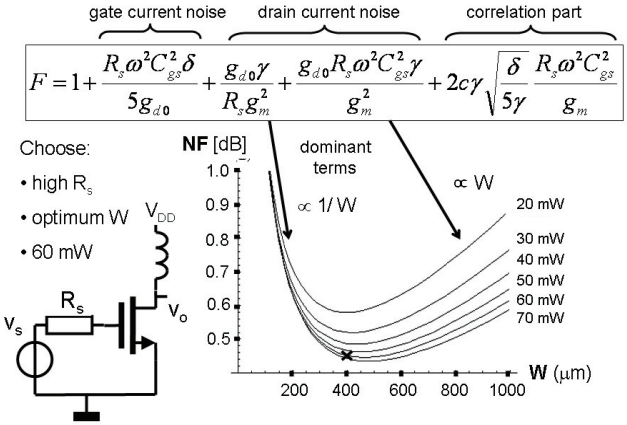

Fig. 2. Choices to optimize the noise factor F of a single Common Source MOSFET and Noise Optimization for R_s=150 Ω (symbols as commonly used [2]).

For a real source impedance of 50 Ω, typical NF50 values are not much lower than 1dB for a 0.18µm CMOS and 0.5dB for a 50nm technology [1]. Thus even 50nm technology seems not good enough to achieve <0.6dB noise figure, as 0.1-0.2dB noise budget is needed for other sources of noise, like the noise contribution of the load impedance, the 50-Ω driver stage and unavoidable losses in the connections. Unfortunately, the use of a simple gate series-inductor is not of great help. Citing [2] $B_{opt}\approx-\omega C_{gs}$: "We see that the optimum source susceptance is essentially inductive in character, except that it has the wrong frequency behavior. Hence, achieving a broadband noise match is fundamentally difficult." Indeed, all fully integrated CMOS LNAs with sub-1dB NF that we found in literature achieve low noise in a bandwidth which is only a small fraction of the center frequency.

Another problem associated with inductive noise matching networks is the need for large inductors, to realize the optimum source impedance for a very wide high transconductance MOSFET. To be effective at 600MHz, inductors in the order of 10nH or more are needed. As 1Ω series resistance already renders 0.09dB NF contribution for 50Ω, inductor Q-values of about 100 are needed, far from feasible on a CMOS chip. However, one option is still left: according to the noise factor equation in figure 2, raising the source resistance can be quite effective. Experiments with several antenna designs show that a real impedance level in the order of 150 Ω is feasible, and we optimized our LNA for that antenna impedance. The transistor width and bias was optimized at various frequencies using a power constraint noise optimization similar to [2]. Figure 2 shows a typical result for a 0.18µm MOSFET and indicates the dominant terms. A rather flat optimum width of about 400µm was found. To push the noise limit, a bias of 60mW at 1.8V was chosen (~75µA/µm, close to the optimum predicted by [1]).

III. CMOS LNA Design

In order to minimize noise and obtain more then 20dB gain, cascoding and a combination of a drain resistor and inductance is used. The drain inductor results in a strong increase of the gain with frequency, which degrades linearity and is problematic in the further signal processing. To equalize the gain somewhat, inductive degeneration was used in the second stage (see figure 3).

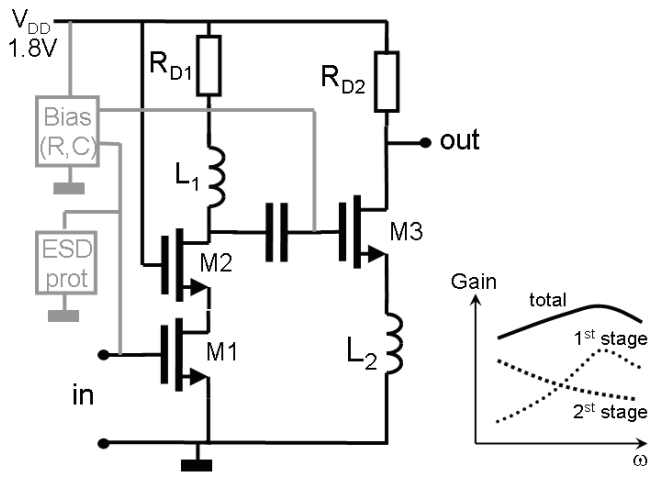

Fig. 3: Schematic of the LNA-IC with gain-variation reduction via the inductor L_2

Figure 4 shows simulation results for the LNA with 50 Ω and 150Ω source impedance using UMC18 RF models. For 150Ω source impedance, the noise figure remains below 0.6dB from 300MHz to 1.5GHz. For 50Ω the minimum noise is about 0.8dB@1.5GHz with sub-1dB noise figure from

600MHz to above 2GHz. Note that this includes noise of the RC-bias circuit. Almost all LNA noise originates from M1 (e.g. >93% for 0.8dB@1.5GHz). The gain equalization reduces the gain variation over the 0.6-1.6GHz band to <3dB (150 Ω) and <7dB (50Ω).

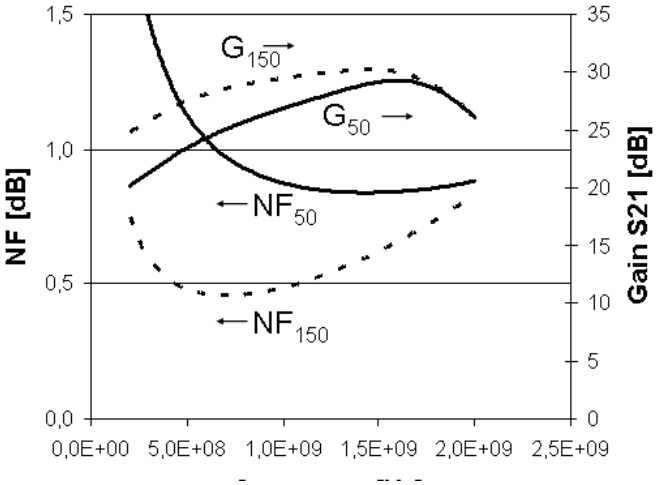

Fig. 4: Simulated Gain S21 and NF for 50Ω and 150Ω source impedance.

IV. Experimental Results

The chip was fabricated at UMC and its photograph is shown in figure 5. At this point in time, only well understood measurement results for a 50Ω source impedance are available, and we are still working on the 150Ω measurements. Figure 6 shows the s-parameters measured via wafer-probing.

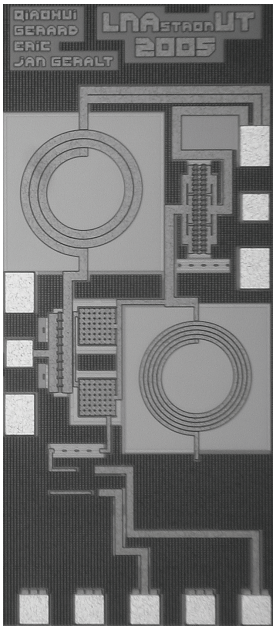

Fig. 5: Chip photo of the wideband LNA (0.60x1.2mm2)

There are some deviations w.r.t. simulation, rendering somewhat more peaking in the gain and worse S22 due to a (too) high RD2 value. The noise figure was measured in many ways with several double-checks, both on-wafer and on a board with the option to add external inductors. The best reproducible results were obtained in a Faraday Room for board measurements using a Agilent N8973A with a Agilent 346A noise source. Figure 7 shows that measurement results without external inductor resemble simulations (figure 4), except for a deviation at high frequencies which is most probably caused by the bond-wire inductance. To verify the measurement setup and the theoretical expectations, measurements with high-Q external series inductors were also done (4nH and 10nH). As expected, increasing the gate inductance helps to decrease the minimum noise figure (from 0.8dB to 0.6 dB), but also limits the low-noise bandwidth. The best bandwidth is achieved without external inductors, with more then 1GHz sub-1dB noise figure bandwidth. Table I compares both simulations and measurements to other designs, showing the competitiveness of this design in low-noise bandwidth.

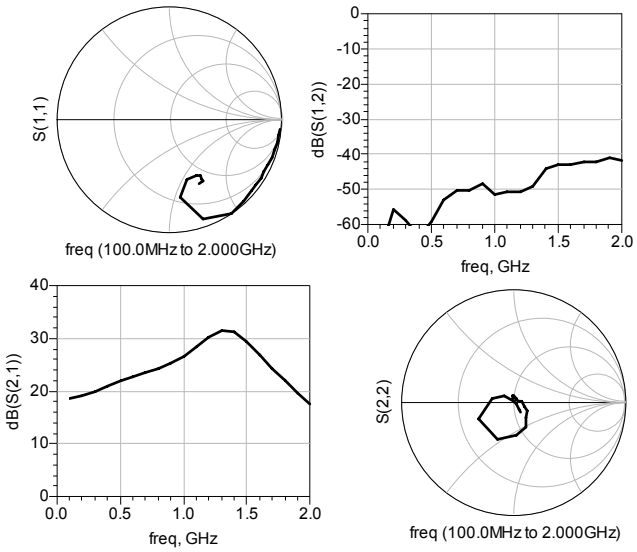

Fig. 6: Measured S-parameters of the LNA with respect to 50 Ω

Noise measurements for variable source impedance are currently ongoing, where we use a 50Ω, 100Ω and 150Ω resistor which is cooled down with liquid Nitrogen to 77K to realize a "cold" measurement, while doing a "hot" measurement at room temperature. Measurements for this method agree well with the 50Ω results in figure 7. For 100Ω and 150Ω source impedance, we measure lower noise figure, as expected. At 900MHz and 150Ω source impedance we reproducibly measure a noise temperature as low as 25K (0.35dB). However, above 1GHz the noise figure rises sharply. We currently try to resolve whether this is caused by non modeled parasitic components in the IC, or by the measurement setup (the current setup still requires an

electrically long transmission line to connect to the 150Ω resistance in the dewar with liquid nitrogen, and we also use a 92Ω semi-rigid coaxial line for reasons of practical availability).

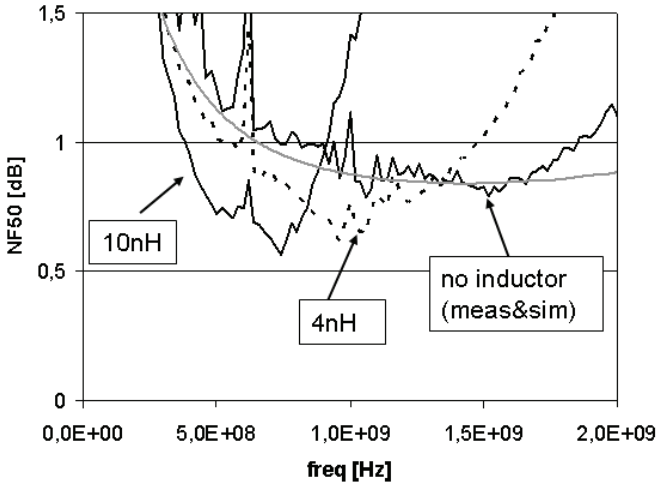

Fig. 7: NF50 measured using a bonded LNA on a board with and without high-Q external inductors

V. Conclusions

In this paper we report work that tries to push the noise figure and gain of a wideband 500MHz-1.6GHz CMOS LNA, assuming we don't need input impedance matching because the LNA is mounted an antenna with very short connection lines. We motivated why a Common Source MOSFET without any noise matching network is suitable to achieve wideband low noise without any external high-Q components, while a high antenna impedance is favorable to reduce the noise figure. Measurements show that even in a 0.18µm CMOS technology sub-1dB noise figure and more than 23dB gain can be achieved over more than an octave in bandwidth (0.8-1.8GHz) at 90mW power consumption. For 150Ω source impedance, a narrowband noise figure of 0.35dB has been measured at 900MHz, but further wideband noise characterization is needed.

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TABLE I
Performance comparison with other low noise amplifier designs.

Property	**This 150Ω**	**[3]**	**[4]**	**This 50Ω**	**[5]**	**[6]**	**[7]**	**[8]**
Gain [dB]	>26	>21	>18	> 23	14	25	14	20
lowest NF [dB]	0.35 meas	0.45	0.45	0.8	1.8	1.9	0.85	0.8
low noise band [GHz] for NF:	0.3 ...1.4 <.6dB	0.6...1.6 <.5dB	0.7... 1.5 <.6dB	0.8...1.8 <1dB	0.2...1.1 <2dB	1.0...4.5 <2dB	0.85...0.95 <1dB	1.1...1.3 <1dB
OIP2 [dBm]	28 1.8&.8G	?	?	25 1.8&.8G	26	-	-	-
OIP3 [dBm]	14 1.1&1.2G	15	?	15 1.1&1.2G	14	21	16	+9
Power [mW]	90	850	50	90	35	42	18	9
Area [mm^2]	0.72	1.5	?	0.72	0.075	~.025	.66	.66
External coils?	0	1	3	0 bondwire	0	0	1	0 bondwire
CMOS Process	.18µ	.2µ GaAs	.18µ	.18µ	.25µ	.09µ	.35µ	.25µ
meas/sim	sim	sim	sim	meas	meas	meas	meas	meas