kept for signal sources. In this circuit only four MOS transistors cause output noise, and only their matching is critical to the accuracy. An adjustable bidirectional current mirror/amplifier can be implemented with two identical OTAs, controlled by either a voltage or a current. All current mirrors/amplifiers have a simple structure and can be easily integrated in MOS technology.

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CMOS VARIABLE TRANSCONDUCTANCE CIRCUIT WITH CONSTANT BANDWIDTH

Indexing terms: Circuit theory and design, Transistors, MOS devices

This letter proposes a new linear CMOS transconductor circuit. It has a transconductance linearly variable by a gate voltage and a rather high bandwidth. Moreover, this bandwidth remains constant when the transconductance is varied. The circuit exploits the square-law characteristic of MOS transistors biased in saturation.

Introduction: Linear transconductors or voltage-to-current convertors are essential analogue integrated circuit building blocks. Several circuits have recently been proposed[1–4] relying on the square-law behaviour of a MOS transistor biased in saturation:

$$I_d = k(V_{gs} - V_{th})^2 \tag{1}$$

A design problem encountered in many of these circuits results from the fact that C_{th} depends on the source-bulk voltage ('body-effect' or 'back-gate effect'). If this voltage is not constant, deviations occur in the square-law V_{gs} to I_d relation, resulting in linearity errors in the transconductor.

This problem is often solved by using transistors, of which the bulk terminal is connected to the source.[1,3] However, this is only possible for transistors located in separate wells, and moreover it results in severe bandwidth reductions because a relatively large well-to-substrate capacitance is introduced on the source-node.[3]

An alternative approach[2,4] uses PMOS and NMOS transistors in a common-source configuration as square-law circuits. By suitable back-gate biasing first-order cancellation of the threshold voltage variations can be achieved.[2]

This letter proposed a circuit in which square-law transistors with constant source-bulk voltages perform the transconductance operation. Additional circuitry copies the input voltage to these transistors. When finalising this letter we discovered that this possibility of constructing a transconductor was previously recognised by Torrance *et al.*[5] but was not examined further in their paper. We shall propose a new circuit according to this principle and show that this circuit has attractive properties, especially with respect to high-frequency behaviour: it has an approximately first-order behaviour with a rather high bandwidth, and moreover this bandwidth remains constant when the transconductance is varied.

Operation of linear transconductor: Fig. 1 shows the basic transconductor circuit. Transistors M1 and M2 are the square-law transistors that perform the actual transconductor function. Transistors M3-M8 constitute three differential matched pairs with equal tail currents $2I_0$. These pairs are connected in such a way that M5–M6 and M7–M8 carry the same currents as M3–M4. As a result of this, voltage V_{in} is copied to the transconductor transistors M1 and M2. This is shown as follows: presume that M3 and M4 are characterised by k_3 and V_{th3}, M5–M8 by k_5 and V_{th5} and all wells are connected to the supply voltages. Using eqn. 1 and referring to Fig. 1, the following relations may be written:

$$V_{in} = (\sqrt{I_0 + i} - \sqrt{I_0 - i})/\sqrt{k_3} \tag{2}$$

$$V_{gs5} - V_{gs6} = V_{gs7} - V_{gs8} = (\sqrt{I_0 + i} - \sqrt{I_0 - i})/\sqrt{k_5} = \sqrt{k_3/k_5}\, V_{in} \tag{3}$$

It appears from eqn. 3 that two proportional copies of V_{in} arise across the lower differential pairs. These voltages are added to and subtracted from transconductance control voltage V_c (see Fig. 1). Using eqn. 1 and presuming that M1 and M2 are characterised by k_1 and V_{th1}, the output currents I_{out1} and I_{out2} can be calculated:

$$I_{out1} = k_1(V_c + \sqrt{k_3/k_5}\, V_{in} - V_{th1})^2 \tag{4a}$$

$$I_{out2} = k_1(V_c - \sqrt{k_3/k_5}\, V_{in} - V_{th1})^2 \tag{4b}$$

The difference of these currents is

$$I_{out1} - I_{out2} = 4k_1(V_c - V_{th1})\sqrt{k_3/k_5}\, V_{in} \tag{4c}$$

Eqn. 4c describes the transfer function of a linear transconductor. Its transconductance value is linearly variable by voltage V_c. Fig. 2 shows the complete transconductor circuit loaded with resistances $R1$ and $R2$. Transistors M1–M8 and source V_c are the same as in Fig. 1. Voltage source V_0 and transistors M9–M10 supply the tail currents $2I_0$ for the lower differential pairs. The sum of the drain currents of M6 and M7 is equal to this tail current (see Fig. 1). By means of current mirror M11–M12 this current is supplied to the upper differential pair, thus achieving tracking of all differential pair tail currents.

Bandwidth properties: The small signal bandwidth of the transconductor was calculated modelling the transistors with g_m, C_{gs}, C_{db} and C_{sb}. It can be shown that the transconductor has an approximately first-order behaviour with a -3 dB

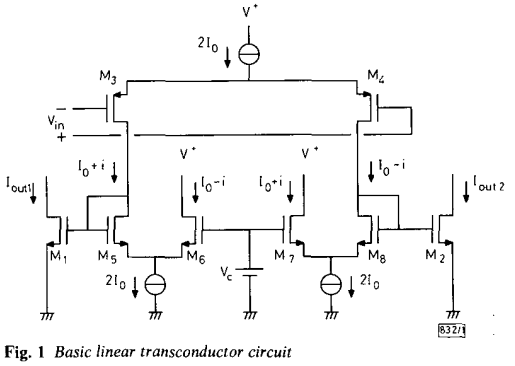

Fig. 1 *Basic linear transconductor circuit*

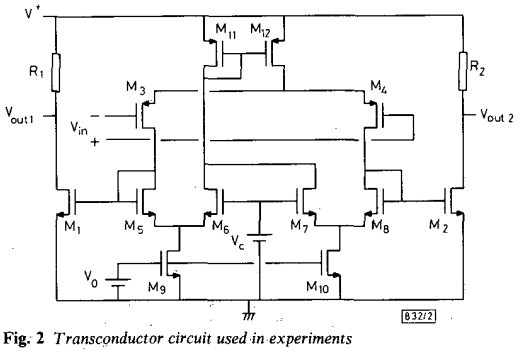

Fig. 2 *Transconductor circuit used in experiments*

bandwidth given by

$$\omega_{-3\,dB} = \frac{g_{m5}}{C_{gs5} + 0{\cdot}5(2C_{sb5} + C_{db9}) + 2(C_{gs1} + C_{db3} + C_{db5})} \quad (5)$$

A very rough estimate of this bandwidth can be made by modelling the transistors with only g_m and C_{gs}. For equal transistors a bandwidth of $g_m/(3C_{gs})$ results, which can be rather high (for reference: the bandwidth of a simple current mirror calculated in this way is $g_m/(2C_{gs})$).

Furthermore, note that, apart from capacitances, the bandwidth depends only on g_{m5}. Since g_{m5} depends only on I_0 (or V_0), and not on V_c, the bandwidth is to first-order independent of the transconductance value. In fact the circuit of Fig. 2 can be regarded (and used) as a first-order filter section with independently variable voltage gain and cutoff frequency, adjustable by V_c and V_0, respectively. This property can be very useful in applications where the phase shift of a gain element should not be affected when the gain is varied.

Experimental results: The circuit of Fig. 2 was realised on breadboard using MOS transistors with threshold voltage of $+0{\cdot}62$ V and $-0{\cdot}77$ V, fabricated in our 5 μm N-well CMOS process. The aspect ratios of the transistors were: 50/10 for M1–M2 and M5–M8, 100/10 for M3–M4, 150/10 for M9–M10 and 525/10 for M11–M12. $V+$ was 5 V, $R1$ and $R2$ were 2 Kohm and V_0 was 1·1 V, resulting in $I_0 = 50\,\mu$A. A balanced input signal was used with a common-mode voltage of 2·5 V.

Measurements showed mainly third-harmonic distortion. At 1 KHz the THD was lower than 0·2% for V_{in} values up to 1 V_{pp} and V_c ranging from 2 to 2·8 V (transconductance ranging from 620 μA/V to 930 μA/V). A larger V_c range is possible at the cost of a lower V_{in} range and vice versa. The main limitations of the V_{in} and V_c ranges for this supply voltage and k_3/k_5 ratio were the saturation conditions of M3–M4 and M9–M10 ($V_{ds} > V_{gs} - V_{th}$).

The high-frequency properties of the transconductor were studied by simulations, because breadboarding parasitics dominated the HF behaviour. The bandwidth was simulated to be 9 MHz for $I_0 = 50\,\mu$A, within 5% of the value predicted by eqn. 5. Breadboard measurements and simulations confirmed the statement that the bandwidth is independent of V_c.

Using the voltage copier circuits described in Reference 5, a larger V_{in} and V_c range might be achieved. However, this results in more complex circuits with additional time-constants.

Conclusion: A new linear transconductor circuit has been proposed. It has a transconductance linearly variable by a gate voltage. Moreover, it has a rather large bandwidth that is independent of the transconductance value.

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ABSOLUTE EVALUATION OF EFFICIENT HEURISTICS FOR DETERMINATION OF MINIMAL ESSENTIAL SETS

Indexing terms: Circuit theory and design, Graphs and graph theory, Mathematical techniques

We describe an absolute evaluation of efficient and fast heuristics for the determination of minimal essential sets, applied to sparse matrices. The estimated efficiency of finding an absolutely minimal essential set gives a probability of more than 0·7.

Introduction: An important methodology for analysing the structure of problems is related to the notion of the minimal essential set (MES).[1,2] Since the determination of an absolutely minimal essential set is an NP-complete problem, there is an obvious need for polynomial-time-bounded algorithms, based on purely local considerations, that are able to give a MES with a cardinality (order of the MES) close to the optimal value.

Among the various basic formulations of this problem, we may consider the determination of optimal k-bordered lower triangular matrices, usually transformed into a graph problem. In contrast to these current practices, we have proposed an approach which is based on a direct investigation of the matrix structure,[3] and which has been called the 'block approach'.

The purpose of this letter is to describe an absolute evaluation of the results obtained with this approach,[4] which exhibits a very good probability of obtaining an absolutely minimal cardinality of the MES. To do this, we present here two different heuristics and results obtained for each of them and from their combination.

The basic feature of this approach is that each iterative step is schematically built as follows:

(*a*) A number of variables (sources variables) are presumed to be known. In this sense, this 'source set' constitutes the basis for the choice of essential variables.

(*b*) A number of 'deduced variables' (the deduced set) can be obtained by direct substitution.

(*c*) The union of a source set and a deduced set constitutes a 'structured block'.

A necessary and sufficient condition for the deduction of new variables is that all variables but one are known in at least one equation. This holds for the starting step and thus a source set is built from variables in a 'source equation'.

Heuristic H1: This first approach restricts the search of blocks to the set of initial equations, taking into account that 'the solution of this problem should be found if we know all variables belonging to one equation in the original system'.

From this point of view, each equation constitutes a 'source set' and the solution exists if all the remaining variables can be 'deduced' from this starting situation. One considers first equations with the minimum of nonzero entries, to minimise the resulting MES cardinality. This approach fails if there are no equations giving a solution.

Heuristic H2: One is concerned here with the combinatory analysis of all the blocks generated starting from a subset of the equations with a minimum of nonzero entries. If the first