# Finding All Elementary Circuits Exploiting Transconductance

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***Abstract*—Commonly used elementary circuits like single-transistor amplifier stages, the differential pair, and current mirrors basically exploit the transconductance property of transistors. This paper aims at finding all elementary transconductance-based circuits. For this purpose, all graphs of two-port circuits with one or two voltage controlled current sources are generated systematically. This results in 150 graphs of "finite transactance two-port circuits" with at least one nonzero transmission parameter. Each of them can be implemented in various ways using transistors and resistors, covering many commonly required types of two-ports. To illustrate the usefulness of the technique several alternative circuit implementations for current amplifiers and voltage followers are generated. A new wide-band low-noise amplifier generated with the technique was realized in 0.35-$\mu$m CMOS.**

***Index Terms*—Analog circuit design, circuit synthesis, circuit topology, computer-aided design, systematic circuit generation, transconductor, voltage-controlled current source.**

## I. Introduction

ANALOG CIRCUIT designers commonly use elementary circuits as building blocks for larger circuits. Well-known CMOS circuit examples from textbooks are the common source, common gate, and common drain amplifier stages, the CMOS inverter, differential pair, and current mirror [1]. Such circuits are for instance cascaded to implement wide-band amplifiers and OPAMPs or synthesize transconductance-$C$ filters. In these circuits, the MOS transistor basically *acts as a transconductor* with small signal transconductance $g_m$. Therefore, we refer to this class of circuits as "transconductance-based CMOS circuits" [2]. There are several good reasons for exploiting transistors as transconductors.

- MOS transistors behave fundamentally like a transconductor in a wide frequency band. Therefore, transconductors are commonly used as active elements at high frequencies in amplifiers, mixers, oscillators, and filters.
- A wide range of transconductance values is possible by changing $W/L$ and biasing: $g_m$-values may range from nS (weak inversion) up to $S$ (strong inversion). This renders large design freedom, e.g., in the choice of $G_m$-$C$ filter time-constants.
- Transconductance values can be well matched by proper choice of transistor dimensions [3]. This is for instance exploited in the current mirror to obtain accurate current ratios and in the differential pair to obtain low voltage offset.
- Tuning the transconductance value electronically is possible by switching transconductance elements in parallel (coarse tuning), or by changing the bias point (fine tuning). Thus, it is possible to correct for production spread and ageing, or implement programmability (e.g., in variable gain amplifiers).

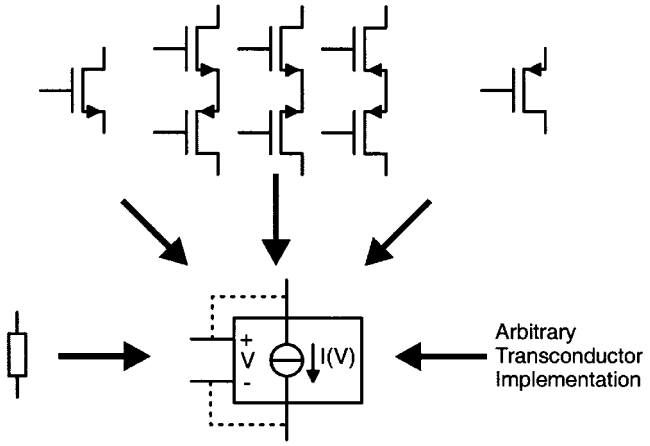


Fig. 1. In many circuits transistor and resistor configurations are exploited as a transconductor and can be modeled by a voltage controlled current source (VCCS).

As elementary transconductance-based circuits prove so useful, one might wonder whether there are more then the well-known textbooks circuits. This subject has been addressed in a systematic way in a Ph.D. dissertation, generating *all linear two-ports with 1 and 2 voltage controlled current sources* (VCCSs) [2]. This paper reports how potentially useful two-port circuits are generated systematically via linear graphs (Sections II–IV). This results in 150 graphs that are classified on nonzero transmission parameters to see which types of two-ports can be implemented (Section V). Each of the graphs can be implemented in various ways on transistor level as shown in Section VI. To demonstrate the usefulness of the generation method, several alternative circuit implementations of current amplifiers and voltage followers will be generated. Moreover, the practical usefulness of the technique is demonstrated via a new low-noise amplifier (LNA), found via the systematic circuit generation. A chip realization has attractive properties with respect to noise and linearity (Section VII).

## II. Generating Potentially Useful Transactors

As discussed in the introduction, we aim to find *all* elementary transconductance-based two-port circuits. As the transcon-

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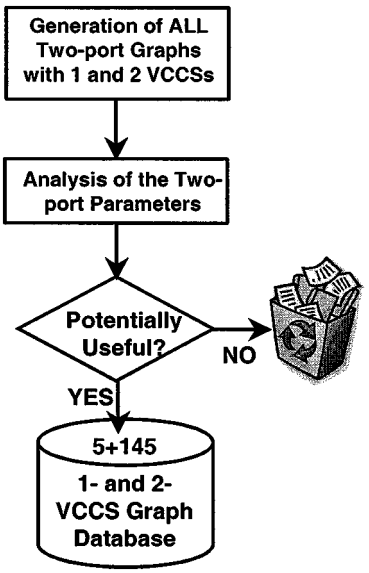



Fig. 2. All linear graphs of two-ports with one and two VCCSs have been generated and potentially useful ones with finite transactance are stored in a VCCS graph database.

ductance is exploited, a VCCS is used as elementary building block. Neglecting the body effect, a MOS transistor could in principle be modeled as a three-terminal VCCS. Nevertheless, a four-terminal VCCS with isolated voltage and current branches is a far more general and flexible device. As shown in Fig. 1, it can represent a single NMOS or PMOS transistor by adding 1 connection either at the top (PMOS) or at the bottom side (NMOS). It can also model a resistor by adding two connections. Furthermore, differential pairs of transistors (also shown in Fig. 1 without biasing), or more involved transconductor circuits are covered in this way (without additional connections). Thus, a four-terminal VCCS is chosen to act as a unifying element, which greatly reduces the number of different cases to deal with during the circuit generation that will follow.

From a viewpoint of circuit topology a VCCS can be represented by two branches: a $v$- and an $i$-branch. Our aim is now to find all elementary two-port circuits in a systematic way. As shown in the flowchart in Fig. 2, this is done by generating all graphs of two-ports with one and two VCCSs. The transfer function of the resulting two-ports is subsequently analyzed and potentially useful cases are stored in a database. The question to be answered now is what makes a linear two-port "potentially useful." To define this, we start from the general notion of what a linear two-port is supposed to do: it senses a signal at its input port and delivers an output port signal proportional to the input signal. The term "transactance" is useful in this respect. Nordholt has argued that the ultimate design goal should be optimum information transfer [4], that is aiming for the best-reproducing transfer function or "transactance" between a source signal quantity and load signal quantity. For now we put the minimum requirement of having some finite transactance (not zero or infinite) for a two-port to be "potentially useful."

### A. Transmission Parameters and Finite Transactance

To define the finite transactance concept more precisely in terms of two-port parameters, consider the transfer function of

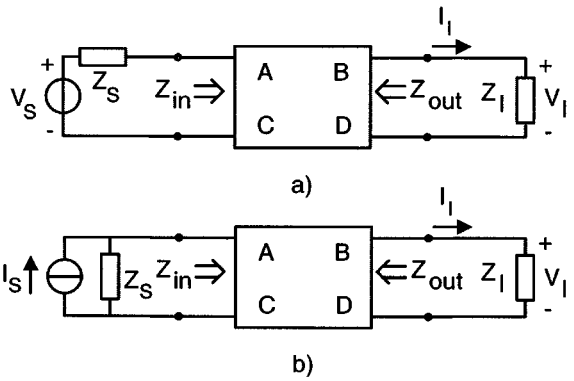



Fig. 3. Two-port described with transmission parameters connected between a signal source and load. As can be verified from (1)–(4), a finite transfer function requires at least one nonzero transmission parameter.

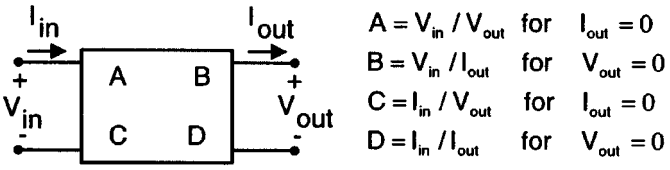



Fig. 4. Definitions of transmission parameters $[A, B, C, D]$.

a two-port connected between a signal source and a load, as shown in Fig. 3. The signal source is either modeled as a voltage source $V_s$ [Fig. 3(a)] with series impedance $Z_s$ or as a current source $I_s$ with parallel impedance $Z_s$ [Fig. 3(b)]. The load is modeled by load impedance $Z_l$ connected to the output port.

The two-port is modeled using transmission parameters $A, B, C$, and $D$, which are for convenience defined in Fig. 4. These parameters are directly related to the four basic "transactances" between voltages and currents: they are the inverse of the voltage gain, transconductance, transimpedance and current gain, respectively.

Using the transmission parameters, the transfer function or transactance from source to load can be calculated. For a voltage source as shown in Fig. 3(a), this leads to a voltage gain and a transadmittance given by

$$A_v = \frac{V_l}{V_s} = \frac{Z_l}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s} \quad (1)$$

$$Y_t = \frac{I_l}{V_s} = \frac{1}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s}. \quad (2)$$

For a current source as shown in Fig. 3(b) the results are a transimpedance and current gain given by

$$Z_t = \frac{V_l}{I_s} = \frac{Z_s \cdot Z_l}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s} \quad (3)$$

$$A_i = \frac{I_l}{I_s} = \frac{Z_s}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s}. \quad (4)$$

Considering the four equations above, it can be concluded that two-ports with a *finite transactance* should *at least have one nonzero transmission parameter*. Obviously, if all transmission

TABLE I
OVERVIEW OF 9 USEFUL TWO-PORTS WITH VERY HIGH, VERY LOW, OR MATCHED PORT IMPEDANCE. THEY CAN BE IMPLEMENTED WITH 1, 2, OR 4 NONZERO PARAMETERS. (ALSO SHOWN ARE THE INVOLVED NONZERO TRANSACTANCES)

| $Z_{in}$ | $Z_{out}$ | Non-zero parameters | Non-zero Transactances |
|---|---|---|---|
| $\infty$ | 0 | **A** | $A_v$ |
| $\infty$ | $\infty$ | **B** | $Y_t$ |
| 0 | 0 | **C** | $Z_t$ |
| 0 | $\infty$ | **D** | $A_i$ |
| $\infty$ | $= Z_l$ | **AB** | $A_v, Y_t$ |
| 0 | $= Z_l$ | **CD** | $Z_t, A_i$ |
| $= Z_s$ | 0 | **AC** | $A_v, Z_t$ |
| $= Z_s$ | $\infty$ | **BD** | $Y_t, A_i$ |
| $= Z_s$ | $= Z_l$ | **ABCD** | $A_v, Y_t, Z_t, A_i$ |

parameters would be zero, then all the transactances are undefined and useless due to the zero in the denominator.[1]

### *B. Port Impedance Considerations*

Apart from requiring a finite transactance, often also requirements on port impedances are important. It is instructive to discuss this matter in terms of nonzero transmission parameters in a bit more detail. The input impedance $Z_{\rm in}$ and output impedance $Z_{\rm out}$ of a two-port connected to a source and load can be expressed as

$$Z_{\rm in} = \frac{A \cdot Z_l + B}{C \cdot Z_l + D} \tag{5}$$

$$Z_{\rm out} = \frac{B + D \cdot Z_s}{A + C \cdot Z_s}. \tag{6}$$

Three types of port impedances are now of particular interest with regard to the adaptation to a given source and load: either very high, very low, or finite accurate port impedance appear to be particularly useful [4]. Finite accurate values of the input or output port impedance are mainly useful if *impedance matching* is required, e.g., for cable receivers or cable drivers to terminate a cable with its characteristic impedance. As can be verified from (5) and (6), the input impedance in general depends on $Z_l$ and the output impedance depends on $Z_s$. Only for specific combinations of transmission parameters this can be avoided, e.g., $Z_{\rm out}$ is independent of $Z_s$ for case $AB$ or case $CD$ (where $AB$ means nonzero $A$ and $B$, i.e., $Z_{\rm out} = B/A$). On the other hand, very high or very low input port impedance are useful to achieve voltage or current sensing, *independent* of the source impedance. For instance: if both $C$ and $D$ are zero, then $Z_{\rm in}$ becomes infinite (sense voltage) and the transactances $A_v$ and $Y_t$ become independent of $Z_s$. Very high or very low output impedances are useful to achieve either voltage or current driving respectively, *independent* of the load impedance. If both $B$ and $D$ are for instance zero, the transfer functions $A_v$ and $Z_t$ become independent of $Z_l$ and ideal voltage drive occurs ($Z_{\rm out}$ becomes 0 in that case).

[1]This implies that we require all circuits to operate as a two-port [5]. Also, all nullor two-ports are rejected (for a nullor all four transmission parameters equal zero). This is justified by the fact that a nullor *as such* is indeed *not* useful: it requires additional feedback components to implement a finite transactance. In theory the source impedance or load impedance could play this role in some exceptional situations. However, a transfer function that entirely depends on source and load impedances is in general useless, as there is no degree of design freedom.

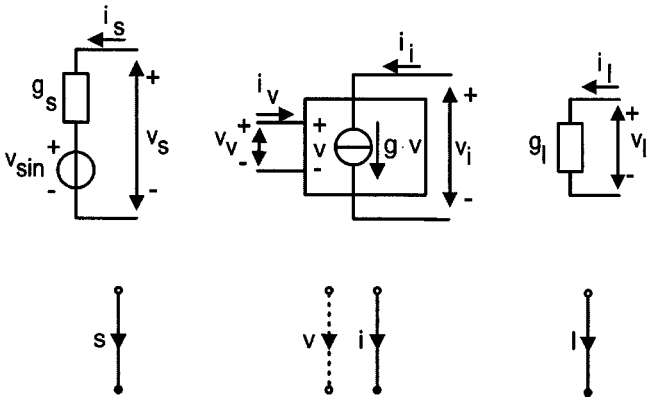



Fig. 5. Circuit elements and their graph representations: an independent source ($s$-branch), a VCCS ($v$- and $i$-branch) and a load impedance ($l$-branch).

Taking these three types of port impedance as a starting point, $3 \times 3$ types of "*transactors*" can be defined [4]. As shown in Table I, these can be implemented with either one nonzero transmission parameter, two nonzero transmission parameters, or four nonzero transmission parameters. Later in this paper, we will see whether we can implement these desired transactors with VCCS circuits.

It has been argued by Nordholt that accurate transfer functions and very high or very low port impedances should be implemented exploiting negative feedback [4]. However, at high frequencies sufficient loop gain is often not available, or renders stability problems. Simple "open-loop" circuits exploiting transconductance find ample application there. Fortunately, in many cases high accuracy is not required and approximations of the ideal transfer function are quite acceptable. Therefore, we do not take feedback as a necessary condition in this work. Instead, we systematically combine transconductors modeled by VCCSs in all possible ways and examine which two-port properties result. The only requirement we pose is to have *at least one nonzero finite transmission parameter*, i.e., at least one finite transactance. In this way we aim to find *all elementary two-port circuit* alternatives, both open-loop circuits and circuits exploiting negative feedback.

## III. GRAPHS WITH ONE VCCS

In the limited space available for this paper we cannot discuss in detail how all the different graphs were generated and analyzed. Only the main characteristics of the generation method will be discussed and the results that were obtained. We will start with circuits with one VCCS in this section, and discuss their generation and analysis. Such circuits consist of the elements shown in Fig. 5: a signal source, a VCCS, and a load impedance.

In order to find all two-port circuits with one VCCS we will use the linear graph representations also shown in the figure.

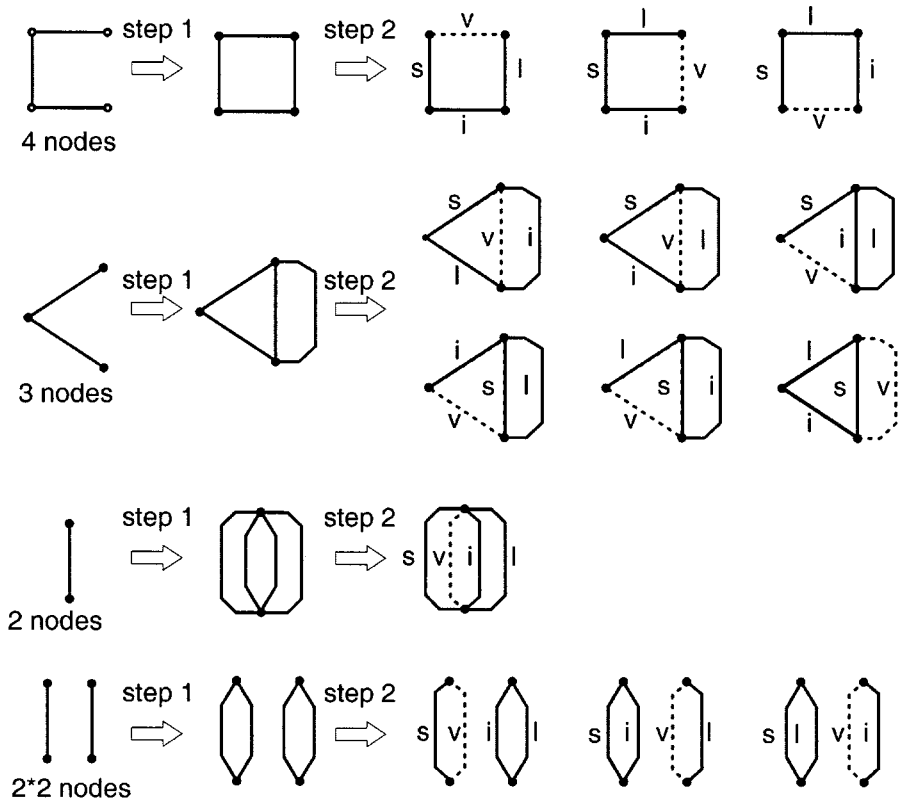



Fig. 6. Systematic generation of all 1 VCCS two-port graphs with the 4 branches shown in Fig. 5.

The graphs consist of four branches: the $v$- and $i$-branch of the VCCS and $a$ $s$- and $l$-branch for the source and load. We will now systematically generate all possible topologies by generating all possible graphs with four branches. This in done in two steps as shown in Fig. 6.

1) "Tree-graphs" [6] are used as a starting point, and "links" are added to find all "fully connected linear graphs" with four branches. Only these graphs have all branches connected in loops and are potentially useful. This is because unconnected graph branches do not serve any function in a circuit (open $v$-branch: undetermined voltage and related current; open $i$- or $l$-branch: zero current; open $s$-branch: input not sensed; so none of them contribute to Kirchhoff relations to force a finite transactance 9 (see also [8]).
2) Graphs are then labeled in all different possible ways (step 2 in Fig. 6).

In the following sections, the transmission parameters of all resulting two-ports are analyzed, to select cases with at least one nonzero transmission parameter.

### A. Systematic Analysis of the Transfer Function

The labeled graphs found in Fig. 6 represent a circuit topology. The transfer properties of an arbitrarily chosen graph will now be analyzed, to illustrate the procedure. Since there are many graphs, the analysis procedure is described in a systematic way, suitable for implementation in a symbolic analysis program. The analysis is performed in four steps and aims at finding the transmission parameters.

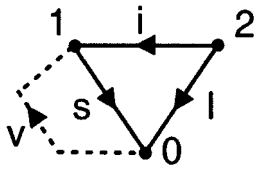



Fig. 7. Directed graph with node numbering used in the transmission parameter analysis example.

1) *Generate directed graphs with node numbers*—Reversal of the $v$- or $i$-branch introduces sign changes in the transfer function. Still these circuit variants can be described with a single graph, provided that we allow for positive and negative values of transconductance $g$, and define the branch orientations for which the transfer function is derived. For convenience, nodes are also numbered $0, 1, 2 \ldots, N$, and one of them is designated as the datum node (by convention node 0; note that this is not necessarily the ground node in a final circuit, but only serves a role during analysis). Fig. 7 shows an example.
2) *Derive a set of linear equations for the network that is represented by the graph*—For a circuit with $N$ nodes and $B$ branches, $N-1$ independent KCL equations and $(B-N+1)$ independent KVL equations exist [7]. Since the circuit contains a VCCS, which only has a admittance two-port representation and no impedance representation, KCL node equations are used as a starting point. Then

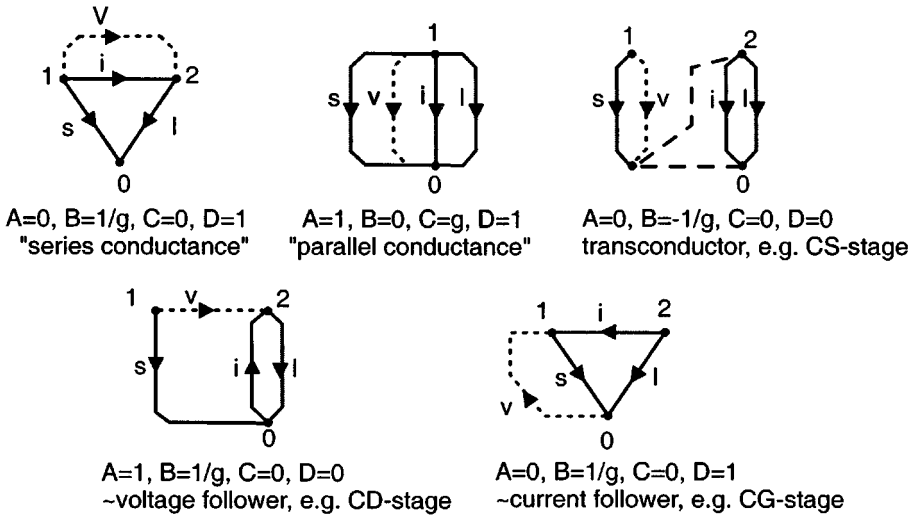



Fig. 8. All potentially useful graphs of circuits with a source $(s)$, load $(l)$ and one VCCS ($v$ and $i$) (see text).

branch equations are substituted, with voltages expressed in terms of node voltages. For the graph in Fig. 7, this leads to

$$g_s \cdot (v_1 - v_{\rm sin}) - g \cdot -v_1 - 0 = 0 \quad (7)$$

$$g \cdot -v_1 + g_l \cdot v_2 = 0 \quad (8)$$

where $v_{\rm sin}$ is the open terminal independent source voltage, $g_s$ is the source admittance, $g$ is the VCCS transconductance, and $g_l$ is the load admittance (see Fig. 5).

3) *Solve the set of equations for the node-voltages*—Obviously, this is only possible if the determinant of the set of equations is nonzero (else the circuit is rejected). For the example, the determinant is

$$\det\begin{vmatrix} g_s + g & 0 \\ -g & g_l \end{vmatrix} = g_s \cdot g_l + g \cdot g_l. \quad (9)$$

Thus, for a certain critical negative value of $g$, the set of equations has no solution. This leads to an interval requirement on $g$, also related to stability, as we will discuss later.

4) *Calculate the transmission parameters of the transactor*–The four transmission parameters are to be evaluated at either zero output voltage or zero output current. We can enforce these conditions by taking the limits of appropriate transfer functions, either for $g_l$ approaching zero or infinity.

For the example under discussion, the results are

$$A = 0 \quad B = 1/g \quad C = 0 \quad D = 1.$$

The analysis procedure described above has been automated using the mathematical software package MAPLE [9]. The results for circuits with one VCCS are described in the next paragraph.

### B. Resulting One VCCS Circuits

Fig. 8 shows the graphs with one VCCS and at least one nonzero transmission parameters. Obviously, it is possible to implement a transconductor with $B = -1/g$ (e.g., with a common source transistor). Also, a series conductance and parallel conductance are possible (e.g., via a "self-connected" VCCS implementation). Finally, for large transconductance values, a voltage follower can be approximated (only nonzero $A = 1$, e.g., with a source follower) and a current follower (only nonzero $D = 1$, e.g., a common gate stage). Happily, we appear to cover all the known single-transistor amplifier stages.

The upper rightmost graph in Fig. 8 is peculiar in the sense that it consists of two subgraphs: a parallel $s$- and $v$-branch and a parallel $i$- and $l$-branch. These graphs can be joint at an arbitrary node indicated with dashed lines without changing the transmission parameters. This is because the VCCS $v$-branch senses the differential voltage across the source branch: the common mode voltage with respect to the load ideally has no effect. In practical circuits this is useful to implement a so-called "floating input," and the graphs will be labeled *floating input graphs*.

## IV. Graphs With Two VCCSs

As we are not satisfied with only five circuits, a second VCCS will be added and all two-ports with two VCCSs will now be generated. As hundreds of graphs exist in this case, computer assistance is indispensable. From the experience gained in generating the graphs with one VCCS, rules for useless graphs have been inferred and proven. In this way we simplified the generation process. A very useful rather obvious rule found was that $v$-branches do not play any role in Kirchhoff Current Law (KCL) relations (their current is always zero). Hence, KCL relations can be derived from graphs *without $v$-branches*. As a consequence, it is possible to split the graph generation into two phases.

1) Generating all KCL-graphs consisting of two $i$-branches (from two VCCSs) and a source $(s)$ and load $(l)$ branch (no $v$-branches). This is a task with limited complexity similar to that of the one VCCS graph generation, which was still done by hand.
2) Systematically adding $v$-branches to the graphs in all possible ways and analyzing the transfer function in term, of

transmission parameters. This is a tedious job involving several hundreds of graphs performed by a MAPLE graph generation and symbolic analysis computer program.

Again, the final graphs with two VCCSs should be fully connected graphs. However, the KCL graphs do not necessarily have this property, because $v$-branches are added afterwards. Instead, KCL graphs should satisfy the following requirements.

- *At least one VCCS $i$-branch should be connected to the load*—This is because a VCCS can only affect load voltage and current via the $i$-branch. If none of the load quantities is affected by any VCCS, no finite transactance via a VCCS is possible.
- The *"other" $i$-branch may, but need not, be connected* to one or more branches in current loops: it can still be useful, even if it has zero current. This may seem odd at first sight. However, note that a VCCS can act as a nullor: the $i$-branch can act as a norator and the $v$-branch as a nullator (with reference to Fig. 5: if $i_i = 0$ then $v_v = i/g = 0$). This can result in finite transactance provided there is feedback from one of the norator nodes to a nullator node (i.e., from the $i$-branch to the $v$-branch). If this is the case, the "other" norator node can be connected to any node of the graph without effect (it does not contribute current to a node as its current is 0, while the voltage across an $i$-branch does not affect its current [ideal current source]).

These requirements allow for KCL graphs to consist of more pieces. They can have a separate $s$-branch, just as in the transconductor graph with one VCCS in Fig. 8. As one of the $i$-branches should be connected to the load (first requirement above), not more than three pieces can exist.

All graphs of Fig. 6 can now be re-used to find the KCL graphs we are looking for, where the $v$- and $i$-branch are replaced by the $i_a$- and $i_b$-branch ($i$-branches of two VCCSs indicated with index $a$ and $b$). In addition, graphs with a separate $s$-branch and maximally one separate $i$-branch need to be added. Fig. 9 shows KCL graphs that result from combining all possibilities and removing redundant equivalent ones (as the two VCCSs are equivalent, changing index from $a$ to $b$ results in an equivalent graph). For reasons of convenience, the KCL graphs have been given names, referring to the branch names and their interconnection structure: "$+$" refers to "in series with" and "$//$" to "in parallel with." Brackets are used to indicate groups.

To find all complete graphs, two $v$-branches are added systematically between all possible node-combinations. The separate $s$-branch is either left separate and tested for common mode insensitivity of the transfer function (for floating input graphs), or connected to each node of the rest of the graph (nonfloating input graphs). This is done by introducing a special node "sref" (see the graphs in the low half of Fig. 9). During the automated graph generation and analysis procedure, the sref-node is systematically connected to all other nodes in the graph. The "any" node of a separate $i$-branch acting as a norator could be handled in the same way. However, as discussed above the analysis results are not affected by changing this node-connection, so one analysis for the graph is sufficient. Note that each of the graphs with an "any" node has several alternative implementations with the same transfer function. This will be exemplified in the voltage follower circuit generation in Section VII.

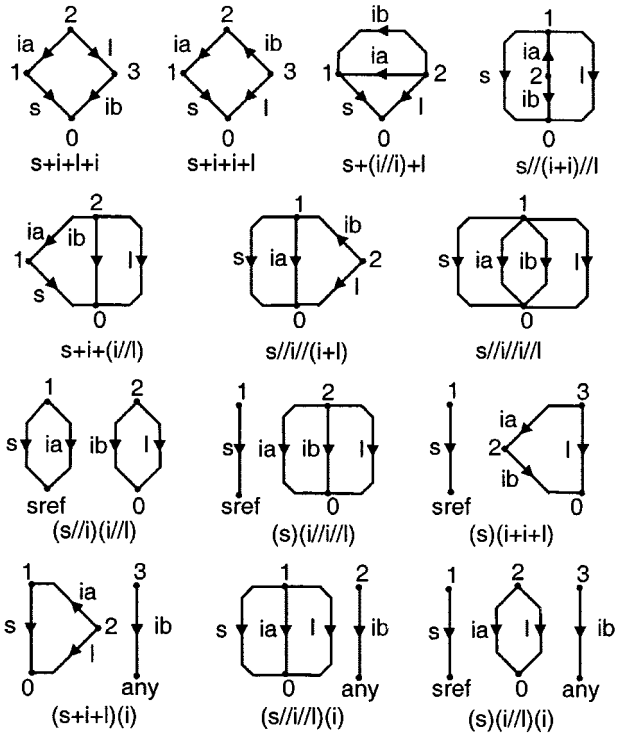



Fig. 9. The 13 directed labeled KCL graphs for two-ports with two VCCSs. By adding $v_a$- and $v_b$-branches systematically between all possible combinations of nodes, all graphs for two-ports with two VCCSs are generated.

## V. Types of Possible Two VCCS Two-Ports

The graph generation and analysis discussed in the previous paragraph leads to 145 graphs with at least one nonzero transmission parameter. Appendix A lists them all, grouped on nonzero transmission parameters. As circuits with floating input are more flexible and have different applications, they are printed separately at the end of the Appendix (12 cases). For each two-port graph the following data are given:

- graph name referring to graphs in Fig. 9;
- equations for the voltage $v_a$ and $v_b$ and, if applicable, for the voltage on node sref. Node 0 is the reference node;
- expressions for the transmission parameters $[A, B, C, D]$ of the two-port.

Table II shows a summary of the results in Appendix A in terms of different combinations of nonzero transmission parameters, and the number of graphs having this property. Obviously, the transmission parameters are a function of transconductance $g_a$ and $g_b$ of the two VCCSs. For simplicity, only the main functional dependence on transconductance is shown. For this purpose a transconductance $g_i$ is introduced, $i$ being an arbitrary index, that represents one of the following expressions:

$$g_i \in \left\{ \pm g_a, \pm g_b, \pm(g_a \pm g_b), \frac{\pm g_a g_b}{g_a \pm g_b} \right\}. \qquad (10)$$

These expressions can also be derived in a systematic way from considerations regarding different possible sets of Kirchhoff relations that can be forced in circuits with two VCCSs [8].

TABLE II
DIFFERENT COMBINATIONS OF NON-ZERO TRANSMISSION PARAMETERS OF TWO VCCS CIRCUITS FROM APPENDIX A. EXPRESSION $g_i$ IS DEFINED IN (10), WHERE $i$ IS AN ARBITRARY INDEX

| Case | A | B | C | D | # |
|---|---|---|---|---|---|
| **A** | 1 | 0 | 0 | 0 | 3 |
| **B** | 0 | $1/g_1$ | 0 | 0 | 37 |
| **D** | 0 | 0 | 0 | 1 | 3 |
| **AB** | 1 or $g_1/g_2$ | $1/g_3$ | 0 | 0 | 24 |
| **AD** | 1 | 0 | 0 | 1 | 6 |
| **BC** | 0 | $1/g_1$ | $g_2$ | 0 | 2 |
| **BD** | 0 | $1/g_1$ | 0 | 1 or $g_2/g_3$ | 24 |
| **ABC** | 1 or $g_1/g_2$ | $1/g_3$ | $g_4$ | 0 | 3 |
| **ABD** | 1 or $g_1/g_2$ | $1/g_3$ | 0 | 1 or $g_4/g_5$ | 24 |
| **ACD** | 1 | 0 | $g_1$ | 1 | 9 |
| **BCD** | 0 | $1/g_1$ | $g_2$ | 1 or $g_3/g_4$ | 3 |
| **ABCD** | 1 or $g_1/g_2$ | $1/g_3$ | $g_4$ | 1 or $g_5/g_6$ | 7 |

As expected from considerations of dimension, the voltage gain $(1/A)$ and current gain $(1/D)$ of the two-port described in Table II are either 0, 1 or a ratio of transconductance expression $g_i$. The transconductance $(1/B)$ is equal to $g_i$ and transimpedance $(1/C)$ equal to $1/g_i$.

Table III lists the nine commonly desired types of linear two-ports discussed in Section II, with either very low, very high, or accurate port impedances. The fourth column shows which two-port of Table II can be used to implement the desired nonzero transmission parameters.

Although there are certainly limitations to what is possible (e.g., there are only two degrees of freedom via $g_a$ and $g_b$), it can be concluded that even with only two VCCSs many useful circuits can be implemented. As might be expected for circuits with VCCSs, cases with high and finite port impedances are readily available. For low port impedance, high transconductance is usually needed (except in cases where one VCCS acts as a nullor).

Care was taken to find equivalent circuit graphs by detecting the existence of equal sets of transmission parameters. In cases where this was observed, equivalent graphs have been rejected. Quite some graphs have transmission parameters that depend only on one transconductance. The other VCCS is "invisible" from the two-port parameters, suggesting that the other is not doing anything useful. However, this is not necessarily the case: it might for instance act as a nullor (e.g., voltage followers in Section VII). In some other cases, the "invisible" VCCS is just an impedance or current follower in series with the current source of the "visible" VCCS. Assuming ideal VCCSs this is useless. However, in practical transistor circuits with only approximate VCCS behavior, it still can be useful. An example is a cascode transistor: it improves the output impedance but this is not evident from a circuit with ideal VCCSs! (they already have infinite output impedance). As our goal was to find all two-port circuits, we decided to maintain graphs in the database, unless we could prove that they are useless or identical to another one that is already there. In other words: we consider graphs "potentially useful," unless it is proven they are not.

TABLE III
OVERVIEW OF THE IMPLEMENTATION POSSIBILITIES OF 9 DESIRED TWO-PORTS USING TWO VCCS CIRCUITS

| $Z_{in}$ | $Z_{out}$ | Desired | Realizable with case | Additional conditions |
|---|---|---|---|---|
| $\infty$ | 0 | A | **AB** | $B \ll A \cdot Z_l$ |
| $\infty$ | $\infty$ | B | **B** | - |
| 0 | 0 | C | **BC** | $B \ll C \cdot Z_s \cdot Z_l$ |
| 0 | $\infty$ | D | **BD** | $B \ll D \cdot Z_s$ |
| $\infty$ | $= Z_l$ | AB | **AB** | - |
| 0 | $= Z_l$ | CD | **BCD** | $B \ll D \cdot Z_s$ |
| $= Z_s$ | 0 | AC | **ABC** | $B \ll A \cdot Z_l$ |
| $= Z_s$ | $\infty$ | BD | **BD** | - |
| $= Z_s$ | $= Z_l$ | ABCD | **ABCD** | $A \cdot D = B \cdot C$ |

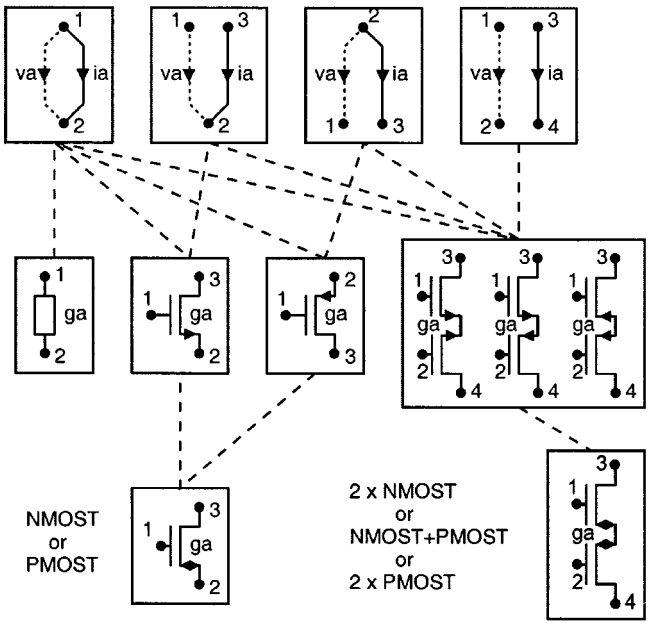



Fig. 10. The interconnections between the $v$- and $i$-branches, and the relative orientation of the branches determines the possibilities to implement a VCCS. Dashed lines show alternative implementations. The double arrow MOST symbol refers to either NMOST or PMOST.

## VI. FROM GRAPH TO CIRCUIT

Now we have a database of graphs of potentially useful circuits, the question is how to implement them on transistor level. Every VCCS in a graph can in principle be implemented using an arbitrary 4-terminal transconductor implementation. However, a single MOST or even a single resistor is sufficient in many cases. Whether this is possible depends on the interconnection and the orientation of the $v$- and $i$-branch of a VCCS in a graph. Fig. 10 illustrates this point. From the figure, we see that three different situations occur.

1) If there is *no* connection between the $v$- and $i$-branch, a VCCS with isolated input and output ports is necessary (right most case). This can be implemented by common

source MOST pairs, either of the same or of different type (biasing is not shown).

2) If one connection exists between the $v$- and $i$-branch, and the branches have the same orientation (both arrows pointing to or from the common node), a single MOST can be used (a PMOST or NMOST depending on the branch orientation). Alternatively, common source MOST pairs can be used.
3) If the branches are connected at both ends (left-most case), and also have the same orientation, then a simple resistor can be used, apart from single MOSTs or common source MOST pairs.

Thus, it appears that branch direction has large impact on the implementation possibilities. Furthermore, it has a strong impact on stability (e.g., reversal of the $v$-terminals may turn a self-connected positive impedance in a negative impedance as exploited in oscillators). Therefore, the direction of the branches will now be considered. The effect of $v$- or $i$-branch reversal is as follows:

- change the direction of the $v$- or $i$-branch: sign change of the related transconductance-term in transmission parameters expressions;
- change both the direction of the $v$- and $i$-branch of the same VCCS: no effect on the transfer function. However, according to Fig. 10, this changes an NMOST into a PMOST and vice versa. This transformation has no effect on the transfer function, but can be useful for instance for biasing purposes to "fit" circuits in a low supply voltage.

As a PMOST implementation can always be replaced by an NMOST by changing both the $v$- and $i$- orientation without changing the transmission parameter equations, it is useful to have a symbol available which represents *either an NMOST or a PMOST*. The symbol that will be used in this paper for this purpose is a MOST symbol with double arrow, as shown at the bottom of Fig. 10.

Note that it is important to indicate the source terminal, even though a MOS transistor physically is a symmetrical device. However, we assume it to implement a transconductor, which is NOT symmetrical anymore: the source is both a voltage-sense and current-source terminal, while the drain is only a current-source terminal.

As an example of the effect of branch reversal on the VCCS implementation possibilities, consider Fig. 11. It shows one of the $(s)(i+i+l)$ transconductor graphs found in Appendix A. In Fig. 11(a) the orientation of the $v$- and $i$-branches are different for $\mathrm{VCCS}_a$ as well as for $\mathrm{VCCS}_b$. Therefore, common source pairs have to be used for both $g_a$ and $g_b$.

By changing the direction of the $v_b$ branch, $v_b$ and $i_b$ get the same orientation [Fig. 11(b)]. Since they are also in parallel, a simple resistor can be used. If the direction of $i_a$ is also changed [Fig. 11(c)], $\mathrm{VCCS}_a$ can be implemented by a single MOST, and the familiar source degenerated MOS circuit results.

Because of these direction changes, transmission parameter $B$ changes, as indicated above the graphs in Fig. 11. Note that

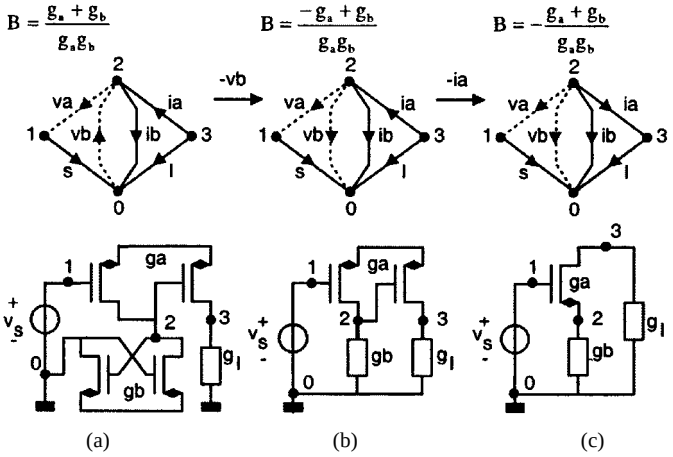



Fig. 11. Example of the effect of $v_a$ and $v_b$ sign changes on the transmission parameter expressions and the complexity of the circuit implementation.

changing the direction of $v_b$ or $i_a$ results in a sign change of respectively $g_b$ and $g_a$ in $B$.

In this place, a note on stability is appropriate. Although the graph analysis renders solutions for the node voltages, it is not guaranteed that the solutions are stable. Many branch orientations render negative impedances, because of positive feedback loops. Therefore, a careful stability consideration is needed, and positive overall node impedances should be guaranteed. By inspection of the graphs, the occurrence of a negative impedance can easily be recognized by qualitative reasoning. In Fig. 11(a), both $\mathrm{VCCS}_a$ and $\mathrm{VCCS}_b$ introduce a negative impedance (note the cross-coupled structure often used in latches). In Fig. 11(b) only $\mathrm{VCCS}_a$ does so, while case Fig. 11(c) has all positive node impedances.

## VII. Circuit Examples

To demonstrate the power of systematic circuit generation, and illustrate some previously mentioned issues, some examples of circuits found with the technique will be given. First, in Section VII-A, current amplifier are generated. In Section VII-B, voltage followers are discussed as an example of circuits where one VCCS acts as a nullor. Finally, a practical LNA IC design with matched input impedance will be discussed in Section VII-C. Examples of variable gain amplifiers can be found elsewhere [12].

### A. Current Amplifiers

As discussed in Section V, in some cases the ideal desired combination of transmission parameters is not available. Still a practical useful approximation of the desired transfer function is often possible. Consider for example a current amplifier. Ideally this should only have nonzero $D$ so that $Z_{\mathrm{in}}$ is 0, $Z_{\mathrm{out}}$ is infinite and the current gain is $1/D$. Unfortunately, only unity gain current amplifiers (current followers) are readily available in Appendix A. However, as shown in Table III an approximation with case $BD$ is possible, provided that $B \ll D \cdot Z_s$. Also, case $ABD$ with $A = 1$ can be used, provided that it is acceptable that voltage changes at the output are copied to the input. When driving with a high ohmic current source these conditions

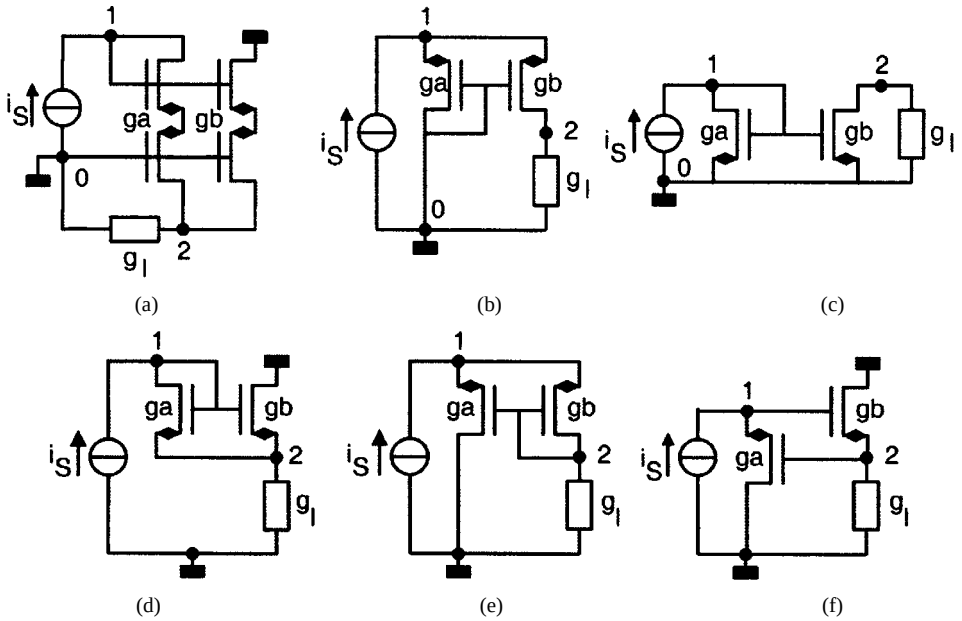



Fig. 12. Current amplifier approximations derived from the $BD$ graphs ($a, b$, and $c$) and $ABD$ ($d, e, f$) graphs with nonunity $D$. The current gain of the circuits is either higher than 1 ($a, d$), lower than 1 ($b, e$), or arbitrary ($c, f$).

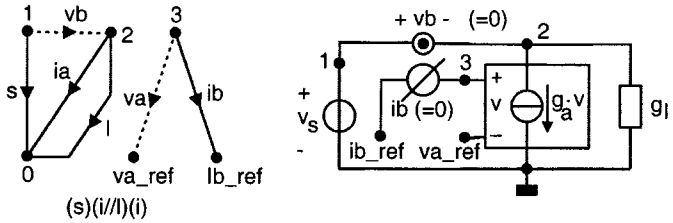



Fig. 13. The voltage follower graph $(s)(i//l)(i)$ in which $\mathrm{VCCS}_b$ acts as a nullor, that forces the load voltage equal to the source voltage.

are often satisfied. Alternatively large transconductance values for $g_a$ can be used. Fig. 12 shows circuit implementations derived from the 3 $BD$ and 3 $ABD$ graphs in Appendix A with nonunity $D$-expressions.

Note that the ubiquitous current mirror is one of them (case c). This example demonstrates that even if the ideally desired two-port can not be implemented directly, practical useful approximations are often available.

### *B. Voltage Followers*

In Section V, it was mentioned that one of the VCCSs may act as a nullor. This is the case for the unity gain voltage followers in the Appendix ($A$ graphs, all of type $(s)(i//l)(i)$). These graphs can be jointly represented as shown in Fig. 13. The nodes $v_{a\_\mathrm{ref}}$ and $i_{b\_\mathrm{ref}}$ can be connected to node 0, 1 and 2 in 9 different combinations. $\mathrm{VCCS}_a$ drives the load $g_l$ and $\mathrm{VCCS}_b$ acts as a nullor (since current $i_b = 0$, voltage $v_b$ is also). This is illustrated in the right part of Fig. 13.

Although not necessary, suppose for simplicity that $v_{a\_\mathrm{ref}}$ and $i_{b\_\mathrm{ref}}$ are grounded. Now, node 2 will follow voltage $v_s$ due to the nullator ($v_b$ branch), provided that $i_b$ acts as a norator providing negative feedback to the $v_b$ terminals. Indeed, $\mathrm{VCCS}_a$ provides this feedback from node 3 (norator node) to node 2 (nullator node). If for instance $v_s$ increases, $\mathrm{VCCS}_b$ will drive the voltage of node 3 down. As a result $\mathrm{VCCS}_a$ drives additional current in the load impedance and the load voltage increases until $v_b$ is zero.

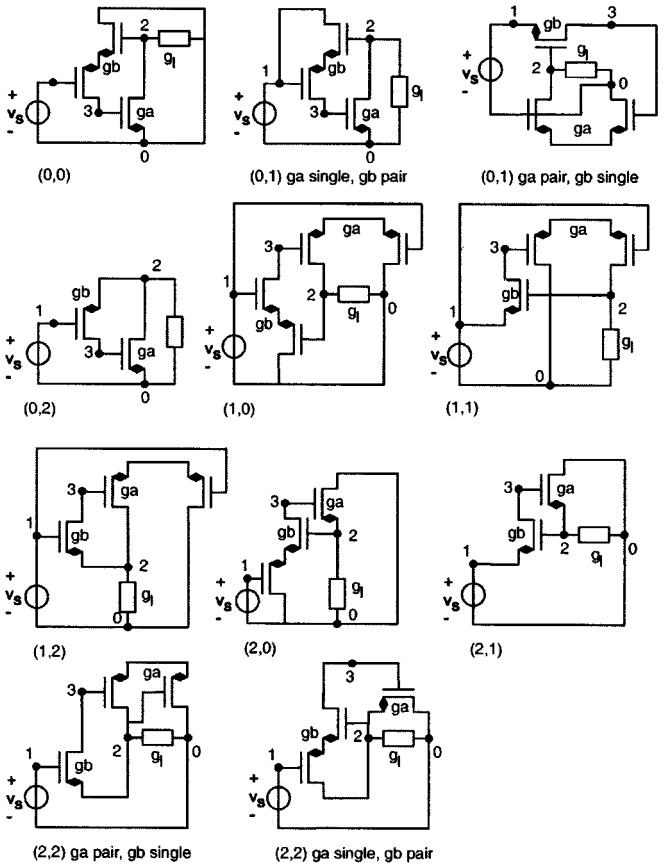



Fig. 14. Voltage follower circuits derived from the graph in Fig. 13 by systematically connecting the $v_{a\_\mathrm{ref}}$ and $i_{b\_\mathrm{ref}}$ nodes to all other nodes in the circuits (their node numbers are indicated between brackets).

Working out all nine different connections of node $v_{a\_\mathrm{ref}}$ and $i_{b\_\mathrm{ref}}$ to other nodes in the circuit, 11 different voltage-follower

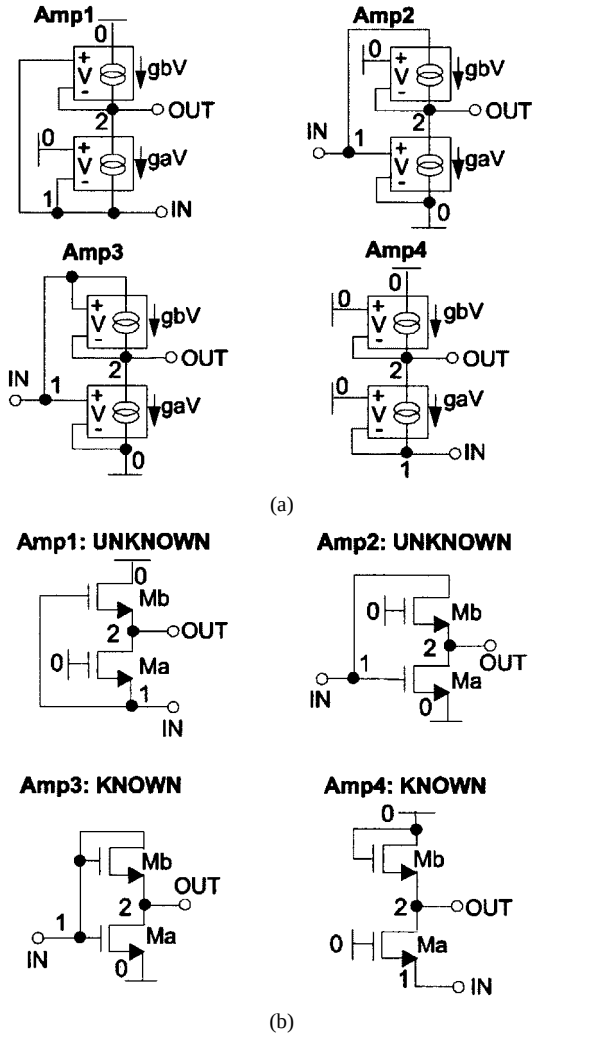



Fig. 15. All two-VCCS wide-band two-port amplifiers (a) that can be implemented with two NMOS transistors and (b) biasing is not shown (voltage bias sources replaced by short-cut to ground, current source by open).

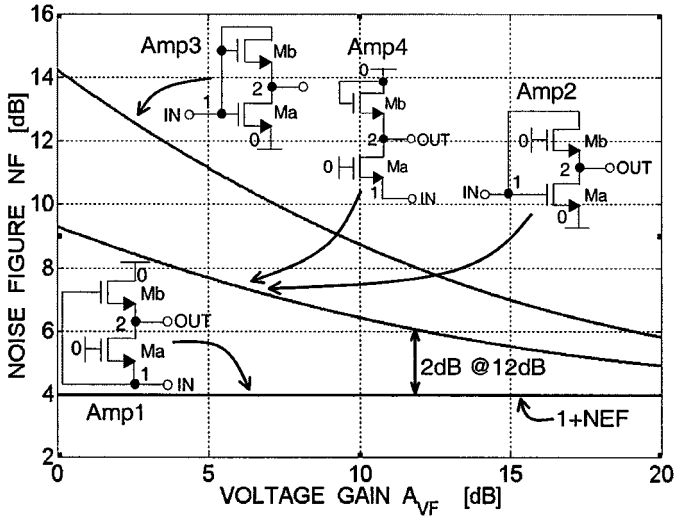
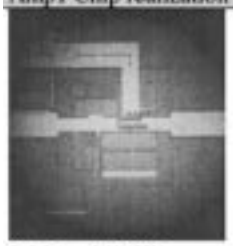



Fig. 16. Simulated NF versus gain $A_{\mathrm{VF}}$ for the generated amplifiers upon input matching (assuming noise spectral density $S_{\mathrm{Id}} = 4kT \cdot \mathrm{NEF} \cdot g_m$ and $\mathrm{NEF}_a = \mathrm{NEF}_b = 1.5$).

TABLE IV
EXPERIMENTAL RESULTS OF AMP1 OF FIG. 15 [10]

| Amp1 Chip realization | Measurement Results | |
|---|---|---|
|  | Forward Gain | 11 dB |
| | -3dB bandwidth | 50-900 MHz |
| | Standing Wave Ratio (75ohm) | < 1.6 |
| | Reverse Gain | < -30dB |
| | IIP2 (2nd order intercept Point) | 27 dBm |
| | IIP3 (3rd order intercept Point) | 15 dBm |
| 0.35μm CMOS<br>Die area 0.06mm²<br>Supply 3.3V | Noise Figure | < 4.4dB |
| | Supply current | 1.5mA |

implementations can be derived as shown in Fig. 14. This example clearly demonstrates the power of the systematic approach: many alternative circuits are generated that are not easily found otherwise.

### C. Matched Input Impedance Low-Noise Amplifiers

Generating circuits is one thing, selecting ones with practical benefits is another issue. To show that this work is not just of academic interest, an example of a practical LNA design will now be discussed briefly. We explored the two VCCS graph database to find all two-transistor wide-band LNA implementations and found two new ones. Detailed amplifier design considerations and measurement results can be found in [10]. Here, we will summarize the main results. The main requirements for the LNA were wide bandwidth (50–900 MHz for a cable modem), input impedance matching to 75 Ω, good linearity (both second and third order) and a maximum noise figure (NF)<6 dB. All two-port graphs of amplifiers with input impedance matching and a capacitive load impedance have been selected from the graph database and additional constraints on gain, stability and wide-band operation were posed. Four graphs resulted which can be implemented with two NMOS transistors. These are shown in Fig. 15 along with the corresponding two-VCCS circuits.

Next to well-known wide-band amplifiers such as the common gate amplifier (Amp4) and the shunt feedback common source amplifier (Amp3, usually implemented with a resistor instead of Mb), two other wide-band amplifiers Amp1 and Amp2 are found. The latter, as far we know, are new two-MOS transistors circuits, although they are related to Amp4 and Amp3, respectively. Amp1, can be derived from Amp4 if the "+" terminal of $\mathrm{VCCS}_b$ is disconnected from the node (0) and connected to the node (1). Amp2 is obtained from Amp3 if the "+" terminal of $\mathrm{VCCS}_b$ is disconnected from the node (1) and connected to the node (0). It turns out that this change in interconnection is beneficial for noise in Amp1 due to partial noise cancellation, as explained in more detail in [2] and [10]. As Fig. 16 shows, Amp1 has a relatively low and gain independent NF, which is more than 2 dB lower than the other amplifiers up to 12-dB gain.

Because of its attractive noise properties Amp1 was realized on chip. Table IV shows a chip photograph along with an overview of the measurement results at 11-dB gain. The measurement results confirm the attractive noise properties and also show good linearity.

## VIII. Conclusion

All elementary transconductance-based two-port circuits with one or two VCCSs have been generated systematically using linear graphs, leading to 150 finite transactance two-ports with at least one nonzero transmission parameter. Many commonly required types of two-ports can be implemented based on these graphs. Each VCCS in the graphs can be implemented in various ways, the simplest being a resistor or a single transistor. Hence, hundreds of elementary circuits can be found starting from the graphs. The usefulness of the circuit generation is illustrated via circuit examples for current amplifiers, voltage followers, and a new wide-band LNA. The latter has attractive noise and linearity properties as was verified by a chip realization and measurements.

## Appendix
## All Graphs With Two VCCSs

NON-FLOATING INPUT GRAPHS

THE THREE CASES WITH NONZERO PARAMETERS $A$:

$(s)(i//l)(i)[v_a = v_3, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = 0, C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = -v_2 + v_3, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = 0, C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = 0, C = 0, D = 0]$.

THE 28 CASES WITH NONZERO PARAMETERS $B$:

$(s)(i//i//l) \quad [v_a = v_1, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/(g_a + g_b)), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_2, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 0, B = (-(-g_a + g_b)/g_b/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_2 - v_1, v_b = v_2, \text{sref} = 0]$
$[A = 0, B = ((-g_a + g_b)/g_b/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_1, v_b = v_2, \text{sref} = v_2]$
$[A = 0, B = (-(-g_a + g_b)/g_b/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_2, v_b = v_1, \text{sref} = v_2]$
$[A = 0, B = ((-g_a + g_b)/g_b/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_1, v_b = v_2, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_1, v_b = -v_2 + v_3, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_1, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_2, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_b), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = -v_2 + v_3, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_b), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_2 - v_1, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_b), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_1, v_b = v_2 - v_1, \text{sref} = v_2]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_2, v_b = v_2 - v_1, \text{sref} = v_2]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = v_3 - v_1, v_b = v_2 - v_1, \text{sref} = v_2]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i+i+l) \quad [v_a = -v_2 + v_3, v_b = v_2 - v_1, \text{sref} = v_2]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = v_3, \text{sref} = 0]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_1, v_b = v_3, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_1, v_b = -v_2 + v_3, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_1, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3, v_b = v_1, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = -v_2 + v_3, v_b = v_2 - v_1, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_2 - v_1, v_b = -v_2 + v_3, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = v_3, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = -v_2 + v_3, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = v_2 - v_1, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = v_1, \text{sref} = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_1, v_b = v_3, \text{sref} = v_3]$
$[A = 0, B = (-1/g_a), C = 0, D = 0]$.

THE THREE CASES WITH NONZERO PARAMETERS $D$:

$(s+i+l)(i) \quad [v_a = v_3 - v_1, v_b = v_1]$
$[A = 0, B = 0, C = 0, D = 1]$
$(s+i+l)(i) \quad [v_a = -v_2 + v_3, v_b = v_1]$
$[A = 0, B = 0, C = 0, D = 1]$
$(s+i+l)(i) \quad [v_a = v_3, v_b = v_1]$
$[A = 0, B = 0, C = 0, D = 1]$.

THE 23 CASES WITH NONZERO PARAMETERS $AB$:

$(s)(i//i//l)\quad [v_a = v_1, v_b = v_2, \text{sref} = 0]$
$[A = (-g_b/g_a), B = (-1/g_a), C = 0, D = 0]$
$(s)(i//i//l)\quad [v_a = v_1, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = (g_b/(-g_a + g_b)), B = (1/(-g_a + g_b)), C = 0, D = 0]$
$(s)(i//i//l)\quad [v_a = v_2, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = ((g_a + g_b)/g_b), B = (1/g_b), C = 0, D = 0]$
$(s)(i//i//l)\quad [v_a = v_2 - v_1, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/(g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = -v_2 + v_3, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_b/g_a * (g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_2 - v_1, v_b = -v_2 + v_3, \text{sref} = 0]$
$[A = 1, B = (1/g_b/g_a * (g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_1, v_b = -v_2 + v_3, \text{sref} = v_2]$
$[A = -1, B = (-1/g_b/g_a * (g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_3 - v_1, v_b = v_2, \text{sref} = v_2]$
$[A = 1, B = (1/g_b/g_a * (g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_2, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_b), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_3 - v_1, v_b = v_2, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_3 - v_1, v_b = -v_2 + v_3, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_3 - v_1, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = -v_2 + v_3, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_b), C = 0, D = 0]$
$(s)(i + i + l)\quad [v_a = v_2 - v_1, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_b), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = -v_2 + v_3, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 1, B = (-1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_2 - v_1, v_b = v_3, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_2 - v_1, v_b = -v_2 + v_3, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_2 - v_1, v_b = v_3 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_3 - v_1, v_b = -v_2 + v_3, \text{sref} = 0]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_3, v_b = v_2 - v_1, \text{sref} = v_3]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = -v_2 + v_3, v_b = v_1, \text{sref} = v_3]$
$[A = -1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_2 - v_1, v_b = v_3, \text{sref} = v_3]$
$[A = 1, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i)\quad [v_a = v_1, v_b = -v_2 + v_3, \text{sref} = v_3]$
$[A = -1, B = (-1/g_a), C = 0, D = 0]$.

THE SIX CASES WITH NONZERO PARAMETERS $AD$:

$s//(i + i)//l [v_a = v_2, v_b = v_2]$
$[A = 1, B = 0, C = 0, D = 1]$
$(s//i//l)(i)\quad [v_a = v_2, v_b = v_2]$
$[A = 1, B = 0, C = 0, D = 1]$
$(s//i//l)(i)\quad [v_a = v_2 - v_1, v_b = v_2 - v_1]$
$[A = 1, B = 0, C = 0, D = 1]$
$(s + i + l)(i)\quad [v_a = v_3 - v_1, v_b = v_2 - v_1]$
$[A = 1, B = 0, C = 0, D = 1]$
$(s + i + l)(i)\quad [v_a = -v_2 + v_3, v_b = v_2 - v_1]$
$[A = 1, B = 0, C = 0, D = 1]$
$(s + i + l)(i)\quad [v_a = v_3, v_b = v_2 - v_1]$
$[A = 1, B = 0, C = 0, D = 1]$.

THE ONE CASE WITH NONZERO PARAMETERS $BC$:

$(s//i)(i//l)\quad [v_a = v_2, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_b), C = g_a, D = 0]$.

THE 23 CASES WITH NONZERO PARAMETERS $BD$:

$s + i + l + i\quad [v_a = v_2, v_b = v_2 - v_1]$
$[A = 0, B = (-1/g_b/g_a * (g_a + g_b)), C = 0, D = 1]$
$s + i + l + i\quad [v_a = v_2 - v_1, v_b = v_2]$
$[A = 0, B = (1/g_b/g_a * (g_a + g_b)), C = 0, D = 1]$
$s + i + i + l\quad [v_a = v_2 - v_1, v_b = v_2]$
$[A = 0, B = ((-g_a + g_b)/g_b/g_a), C = 0, D = 1]$
$s + i + i + l\quad [v_a = v_2, v_b = v_2 - v_1]$
$[A = 0, B = (-(-g_a + g_b)/g_b/g_a), C = 0, D = 1]$
$s + (i//i) + l\quad [v_a = v_1, v_b = v_1]$
$[A = 0, B = (1/(g_a + g_b)), C = 0, D = 1]$
$s + i + (i//l)\quad [v_a = v_1, v_b = v_1]$
$[A = 0, B = (-1/(g_a + g_b)), C = 0,$
$D = (1/(g_a + g_b) * g_a)]$
$s//i//(i + l)\quad [v_a = v_1, v_b = v_1]$
$[A = 0, B = (-1/g_b), C = 0, D = ((-g_a + g_b)/g_b)]$
$(s//i)(i//l)\quad [v_a = v_1, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_b), C = 0, D = (-g_a/g_b)]$
$s + i + l + i\quad [v_a = v_1, v_b = v_2]$
$[A = 0, B = (-1/g_a), C = 0, D = 1]$
$s + i + l + i\quad [v_a = v_1, v_b = v_3]$
$[A = 0, B = (-1/g_a), C = 0, D = 1]$
$s + i + l + i\quad [v_a = v_1, v_b = v_2 - v_1]$
$[A = 0, B = (-1/g_a), C = 0, D = 1]$
$s + i + l + i\quad [v_a = v_1, v_b = v_3 - v_1]$
$[A = 0, B = (-1/g_a), C = 0, D = 1]$

$s+i+i+l \quad [v_a=-v_2+v_3, v_b=v_1]$
$[A=0, B=(-1/g_b), C=0, D=1]$
$s+i+i+l \quad [v_a=v_2-v_1, v_b=v_1]$
$[A=0, B=(-1/g_b), C=0, D=1]$
$s+i+i+l \quad [v_a=v_2, v_b=v_1]$
$[A=0, B=(-1/g_b), C=0, D=1]$
$s+i+i+l \quad [v_a=v_1, v_b=-v_2+v_3]$
$[A=0, B=(-1/g_a), C=0, D=1]$
$s+i+i+l \quad [v_a=v_1, v_b=v_2-v_1]$
$[A=0, B=(-1/g_a), C=0, D=1]$
$s+i+i+l \quad [v_a=v_1, v_b=v_2]$
$[A=0, B=(-1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_3-v_1, v_b=v_3]$
$[A=0, B=(1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_3, v_b=v_3-v_1]$
$[A=0, B=(-1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_1, v_b=v_3-v_1]$
$[A=0, B=(-1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_1, v_b=-v_2+v_3]$
$[A=0, B=(-1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_1, v_b=v_3]$
$[A=0, B=(-1/g_a), C=0, D=1]$.

THE THREE CASES WITH NONZERO PARAMETERS $ABC$:

$s+i+(i//l) \quad [v_a=v_2, v_b=v_2-v_1]$
$[A=((g_a+g_b)/g_b), B=(1/g_b), C=(-g_a), D=0]$
$s+i+(i//l) \quad [v_a=v_2, v_b=v_1]$
$[A=(-g_a/g_b), B=(-1/g_b), C=(-g_a), D=0]$
$(s//i)(i//l) \quad [v_a=v_2, v_b=v_2-v_1, \text{sref}=0]$
$[A=1, B=(1/g_b), C=g_a, D=0]$.

THE 24 CASES WITH NONZERO PARAMETERS $ABD$:

$s+i+l+i \quad [v_a=v_2, v_b=v_3-v_1]$
$[A=-1, B=(-1/g_b/g_a*(g_a+g_b)), C=0, D=1]$
$s+i+l+i \quad [v_a=v_3, v_b=v_2-v_1]$
$[A=1, B=(-1/g_b/g_a*(g_a+g_b)), C=0, D=1]$
$s+i+l+i \quad [v_a=v_2-v_1, v_b=v_3]$
$[A=1, B=(1/g_b/g_a*(g_a+g_b)), C=0, D=1]$
$s+i+l+i \quad [v_a=v_3-v_1, v_b=v_2]$
$[A=-1, B=(1/g_b/g_a*(g_a+g_b)), C=0, D=1]$
$s+i+i+l \quad [v_a=-v_2+v_3, v_b=v_2-v_1]$
$[A=1, B=(1/g_b/g_a*(g_a+g_b)), C=0, D=1]$
$s+i+i+l \quad [v_a=v_2-v_1, v_b=-v_2+v_3]$
$[A=1, B=(1/g_b/g_a*(g_a+g_b)), C=0, D=1]$
$s+(i//i)+l \quad [v_a=v_2, v_b=v_2-v_1]$
$[A=((g_a+g_b)/g_b), B=(-1/g_b), C=0, D=1]$
$s+(i//i)+l \quad [v_a=v_2, v_b=v_1]$
$[A=(-g_a/g_b), B=(1/g_b), C=0, D=1]$
$s+(i//i)+l \quad [v_a=v_2-v_1, v_b=v_2-v_1]$
$[A=1, B=(-1/(g_a+g_b)), C=0, D=1]$
$s+(i//i)+l \quad [v_a=v_2-v_1, v_b=v_1]$
$[A=(-1/(-g_a+g_b)*g_a), B=(1/(-g_a+g_b)),$
$C=0, D=1]$
$s+i+(i//l) \quad [v_a=v_2-v_1, v_b=v_2-v_1]$
$[A=1, B=(1/(g_a+g_b)), C=0, D=(1/(g_a+g_b)*g_a)]$
$s//i//(i+l) \quad [v_a=v_2-v_1, v_b=v_2-v_1]$
$[A=1, B=(1/g_b), C=0, D=((-g_a+g_b)/g_b)]$
$(s//i)(i//l) \quad [v_a=v_2-v_1, v_b=v_2-v_1, \text{sref}=0]$
$[A=1, B=(1/g_b), C=0, D=(-g_a/g_b)]$
$s+i+i+l \quad [v_a=-v_2+v_3, v_b=v_3-v_1]$
$[A=1, B=(1/g_b), C=0, D=1]$
$s+i+i+l \quad [v_a=v_3-v_1, v_b=-v_2+v_3]$
$[A=1, B=(1/g_a), C=0, D=1]$
$s+i+i+l \quad [v_a=v_3-v_1, v_b=v_2-v_1]$
$[A=1, B=(1/g_a), C=0, D=1]$
$s+i+i+l \quad [v_a=v_3-v_1, v_b=v_2]$
$[A=1, B=(1/g_a), C=0, D=1]$
$s+i+i+l \quad [v_a=v_2-v_1, v_b=v_3-v_1]$
$[A=1, B=(1/g_b), C=0, D=1]$
$s+i+i+l \quad [v_a=v_2, v_b=v_3-v_1]$
$[A=1, B=(1/g_b), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_3-v_1, v_b=-v_2+v_3]$
$[A=1, B=(1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=-v_2+v_3, v_b=v_3-v_1]$
$[A=1, B=(-1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_2-v_1, v_b=v_3-v_1]$
$[A=1, B=(1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_2-v_1, v_b=-v_2+v_3]$
$[A=1, B=(1/g_a), C=0, D=1]$
$(s+i+l)(i) \quad [v_a=v_2-v_1, v_b=v_3]$
$[A=1, B=(1/g_a), C=0, D=1]$.

THE NINE CASES WITH NONZERO PARAMETERS $ACD$:

$s//(i+i)//l [v_a=v_2, v_b=v_2-v_1]$
$[A=1, B=0, C=(-g_b*g_a/(g_a+g_b)), D=1]$
$s//(i+i)//l \quad [v_a=v_2-v_1, v_b=v_2]$
$[A=1, B=0, C=(g_b*g_a/(g_a+g_b)), D=1]$
$s//i//i//l \quad [v_a=v_1, v_b=v_1]$
$[A=1, B=0, C=(g_a+g_b), D=1]$
$s//(i+i)//l \quad [v_a=v_1, v_b=v_2]$
$[A=1, B=0, C=(-g_a), D=1]$
$s//(i+i)//l \quad [v_a=v_1, v_b=v_2-v_1]$
$[A=1, B=0, C=(-g_a), D=1]$

$(s//i//l)(i) \quad [v_a = v_1, v_b = v_2]$
$[A = 1, B = 0, C = g_a, D = 1]$
$(s//i//l)(i) \quad [v_a = v_1, v_b = v_2 - v_1]$
$[A = 1, B = 0, C = g_a, D = 1]$
$(s//i//l)(i) \quad [v_a = v_2, v_b = v_2 - v_1]$
$[A = 1, B = 0, C = g_a, D = 1]$
$(s//i//l)(i) \quad [v_a = v_2 - v_1, v_b = v_2]$
$[A = 1, B = 0, C = (-g_a), D = 1]$.

THE THREE CASES WITH NONZERO PARAMETERS $BCD$:

$s//i//(i+l) \quad [v_a = v_2, v_b = v_1]$
$[A = 0, B = (-1/g_b), C = g_a, D = 1]$
$s//i//(i+l) \quad [v_a = v_2 - v_1, v_b = v_1]$
$[A = 0, B = (-1/g_b), C = g_a, D = ((g_a + g_b)/g_b)]$
$(s//i)(i//l) \quad [v_a = v_2 - v_1, v_b = v_1, \text{sref} = 0]$
$[A = 0, B = (-1/g_b), C = g_a, D = (g_a/g_b)]$.

THE SEVEN CASES WITH NONZERO PARAMETERS $ABCD$:

$s + i + (i//l) \quad [v_a = v_2 - v_1, v_b = -v_1]$
$[A = g_a/(g_a + g_b), B = 1/(g_a + g_b),$
$C = -g_a * g_b/(g_a + g_b), D = g_a/(g_a + g_b)]$
$s + i + (i//l) \quad [v_a = v_2 - v_1, v_b = v_2]$
$[A = ((g_a + g_b)/g_a), B = (1/g_a), C = g_b, D = 1]$
$s + i + (i//l) \quad [v_a = -v_1, v_b = v_2 - v_1]$
$[A = g_b/(g_a + g_b), B = 1/(g_a + g_b),$
$C = g_a * g_b/(g_a + g_b), D = g_a/(g_a + g_b)]$
$s + i + (i//l) \quad [v_a = v_1, v_b = v_2]$
$[A = (-g_b/g_a), B = (-1/g_a), C = g_b, D = 1]$
$s//i//(i+l) \quad [v_a = v_1, v_b = v_2 - v_1]$
$[A = 1, B = (1/g_b), C = g_a, D = ((g_a + g_b)/g_b)]$
$s//i//(i+l) \quad [v_a = v_2, v_b = v_2 - v_1]$
$[A = 1, B = (1/g_b), C = g_a, D = 1]$
$(s//i)(i//l) \quad [v_a = v_1, v_b = v_2 - v_1, \text{sref} = 0]$
$[A = 1, B = (1/g_b), C = g_a, D = (g_a/g_b)]$.

FLOATING INPUT GRAPHS

THE NINE CASES WITH NONZERO PARAMETERS $B$:

$(s)(i//i//l) \quad [v_a = v_3 - v_1, v_b = v_3 - v_1]$
$[A = 0, B = (1/(g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l) \quad [v_a = v_4 - v_2, v_b = v_2 - v_1]$
$[A = 0, B = (1/g_b/g_a * (g_a + g_b)), C = 0, D = 0]$
$(s)(i + i + l) \quad [v_a = v_3 - v_2, v_b = v_4 - v_1]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i + i + l) \quad [v_a = v_4 - v_2, v_b = v_4 - v_1]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i + i + l) \quad [v_a = v_2, v_b = v_4 - v_1]$
$[A = 0, B = (1/g_b), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_3 - v_1, v_b = v_4 - v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_4 - v_1, v_b = v_3]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_4 - v_1, v_b = v_3 - v_1]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$
$(s)(i//l)(i) \quad [v_a = v_4 - v_1, v_b = v_3 - v_2]$
$[A = 0, B = (1/g_a), C = 0, D = 0]$.

THE ONE CASE WITH NONZERO PARAMETERS $AB$:

$(s)(i//i//l) \quad [v_a = v_2, v_b = v_3 - v_1]$
$[A = (g_a/g_b), B = (1/g_b), C = 0, D = 0]$.

THE ONE CASE WITH NONZERO PARAMETERS $BC$:

$(s//i)(i//l) \quad [v_a = v_2, v_b = v_3 - v_1]$
$[A = 0, B = (1/g_b), C = g_a, D = 0]$.

THE ONE CASE WITH NONZERO PARAMETERS $BD$:

$(s//i)(i//l) \quad [v_a = v_3 - v_1, v_b = v_3 - v_1]$
$[A = 0, B = (1/g_b), C = 0, D = (-g_a/g_b)]$.

## REFERENCES


[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2000.
[2] E. A. M. Klumperink. (1997) Transconductance based CMOS circuits: circuit generation, classification and analysis. Univ. of Twente, Enschede, The Netherlands. [Online]. Available: http://icd.el.utwente.nl
[3] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.
[4] E. H. Nordholt, *Design of High-Performance Negative-Feedback Amplifiers*. Amsterdam, The Netherlands: Elsevier, 1983.
[5] H. Schmid, "Approximating the universal active element," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 1160–1169, Nov. 2000.
[6] S. Seshu and M. B. Reed, *Linear Graphs and Electrical Networks*. Reading, MA: Addison-Wesley, 1961.
[7] N. Balabanian, T. A. Bickart, and S. Seshu, *Electrical Network Theory*. New York: Wiley, 1969.
[8] E. A. M. Klumperink, "A systematic approach to circuit design and analysis: Classification of two-VCCS circuits," *IEEE Trans. Circuits Syst. I*, vol. 46, pp. 810–819, July 1999.
[9] B. W. Char, K. O. Geddes, G. H. Gonnet, B. L. Leong, M. B. Monagan, and S. M. Watt, *Maple V Language Reference Manual*. New York: Springer-Verlag, 1991.
[10] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Generating all two-MOS-transistor amplifier leads to new wide-band LNAs," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1032–1040, July 2001.
[11] P. W. Li, M. J. Chin, P. R. Gray, and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 828–836, 1984.
[12] E. A. M. Klumperink and A. J. M. V. Tuijl, "Systematic generation of transconductance based variable gain amplifier topologies," presented at the 1998 Int. Symp. Circuits and Systems, CD-ROM Paper TAA8-3, Monterey, CA, May 31–June 3 1998.

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