TRANSCONDUCTANCE BASED CMOS CIRCUITS

Circuit Generation, Classification and Analysis

Eric A. M. Klumperink

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Aan mijn ouders

("Leer'n hoef neet, moar a'j 't wilt en könt, zo'k 't wal do'n").

Aan Angela, Iris en Lisa,

voor de vele uren dat ik wel thuis was, maar niet thuis gaf.

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Selected Symbols and Abbreviations

Symbol	Meaning
1VCCS circuit	Circuit with 1 VCCS connected to ideal voltage or current sources such that a primary Kirchhoff relation is established (section 5.4.3).
2VCCS circuit	Circuit with 2 VCCSs connected to ideal voltage and/or current sources such that 2 independent Kirchhoff relations amongst the VCCS variables are established, at least one of them being a secondary relation (section 5.4.3).
$\mathbf{a_c}$	Ratio between the maximal and nominal transconductance of a VCCS.
A	Transmission parameter v_{in}/v_{out} (inverse of the voltage gain).
A,B,C,D-determined Transactor	Transactor that is driven and loaded in such a way, that one transmission parameter (A, B, C or D) entirely determines the transfer properties (i.e. zero or infinite source and load impedance).
$\mathbf{A_i}$	Current gain from short-circuit source current to load current.
$\mathbf{A_v}$	Voltage gain from open terminal source voltage to load voltage.
B	Transmission parameter v_{in}/i_{out} (inverse of the transadmittance).
BW	-3 dB bandwidth of a circuit.
C	Transmission parameter i_{in}/v_{out} (inverse of the transimpedance).
D	Transmission parameter i_{in}/i_{out} (inverse of the current gain).
EVCCS	Exponential Voltage Controlled Current Source.
$\mathbf{g\ (= g_1)}$	Transconductance of a VCCS; see also list of indices.
$\mathbf{g_o}$	Nominal transconductance (square-root of $g_{min} \cdot g_{max}$).
$\mathbf{g_1, g_2, g_3}$	1st, 2nd and 3rd order Taylor coefficiets of the I(V) relation of a VCCS.
$\mathbf{g_{min}, g_{max}}$	Minimum and maximum value of the transconductance of a VCCS.
$\mathbf{g_P}$	Transconductance of a VCCS (primary current divided by primary voltage).
$\mathbf{g_\Delta}$	Difference g_a-g_b.
$\mathbf{g_{\Pi/\Delta}}$	Product of g_a and g_b, divided by their difference: $g_a g_b/(g_a-g_b)$.
$\mathbf{g_{\Pi/\Sigma}}$	Product of g_a and g_b, divided by their sum: $g_a g_b/(g_a+g_b)$.
$\mathbf{g_{\Sigma\Delta}}$	Sum g_a+g_b or difference g_a-g_b.
G	Transconductance of a LVCCS.
$\mathbf{i_{n,ga}, i_{n,gb}}$	Independent noise current source values associated with g_a and g_b.
$\mathbf{i_{n,a}, i_{n,b}}$	(Dependent) noise current flowing through $VCCS_a$ and $VCCS_b$ respectively.
$\mathbf{i_{neq,in}}$	Equivalent input noise current.
$\mathbf{I_0}$	Biasing Current.
$\mathbf{I_a, I_b}$	Controlled current of $VCCS_a$ and $VCCS_b$.
$\mathbf{I_{ind}}$	Independent Current Source value.
$\mathbf{I_E}$	Current parameter occuring in the EVCCS equation.
$\mathbf{I_{IP2}, I_{IP3}}$	2nd and 3rd order intercept current (extrapolated amplitude for HD2,

respectively HD3, equal to 100%).

Symbol	**Meaning**
$\mathbf{I_L}$	Offset Current in the LVCCS model.
$\mathbf{I_P}$	Primary VCCS current variable.
$\mathbf{I_{SS}}$	Supply Current.
$\mathbf{I_\Delta}$	Difference of VCCS currents I_a and I_b.
$\mathbf{I_\Sigma}$	Sum of VCCS currents I_a and I_b.
k	k-factor in a SVCCS relation (not Bolzman's constant!).
$\mathbf{k_{nom}}$	Nominal value of k (used to compare different designs).
$\mathbf{k_B}$	Bolzman's constant.
KCL	Kirchhoff's Current Law.
KVL	Kirchhoff's Voltage Law.
LVCCS	Linear Voltage Controlled Current Source.
LVCCSθ	LVCCS model with mobility reduction effect added.
m	Scaling factor (ratio between the g-coefficients of $VCCS_b$ and $VCCS_a$).
mult	multiplier relating k to k_{nom} (used to compare different designs).
n	Subthreshold slope parameter of a MOST (see also indices).
N	Number of nodes of a graph or circuit.
NBW	Noise BandWidth.
NEF	Noise Excess Factor of a transconductor ($i^2_{n,out} / 4 \cdot k_B \cdot T \cdot G_m \cdot \Delta f$).
NDR	Dynamic Range, Normalised to HD3=100% and NBW=1Hz.
pwr	Power to which a_c is raised to control the transconductance of VCCSs.
Primary variable	Collective name for the VCCS input voltage V_P and output current I_P variables.
$\mathbf{r_1, r_2, r_3}$	1^{st}, 2^{nd} and 3^{rd} order Taylor coefficiets of the V(I) relation of a VCCS.
sgn	Sign in the equation with a_c and pwr, controlling transconductance values.
$\mathbf{S_c, S_{in}, S_{out}}$	Control, input and output signal of a VCCS circuit (voltage or current).
Secondary variable	Collective name for the sum or difference of two primary variables (voltages V_Σ and V_Δ, and currents I_Σ and I_Δ)
SVCCS	Square-law Voltage Controlled Current Source.
SVCCSθ	SVCCS model with mobility reduction effect added.
Transactor	Collective noun for two-port circuits connected between a signal source and load, transfering information from source to load (non-zero transfer function).
Transmission parameters	Set of two-port parameters, relating the input voltage and input current to the output voltage and output current (parameters A, B, C, D).
$\mathbf{v_{n,a}, v_{n,b}}$	(Dependent) noise voltage at the input of $VCCS_a$ and $VCCS_b$ respectively.
$\mathbf{v_{neq,in}}$	Equivalent input noise voltage.
$\mathbf{V_0}$	Biasing voltage.
$\mathbf{V_a, V_b}$	Input voltage of $VCCS_a$ and $VCCS_b$, controlling I_a and I_b respectively.
$\mathbf{V_{ind}}$	Independent Voltage Source value.
$\mathbf{V_{min}, V_{max}}$	Minimum and maximum voltage limits for model validity (see also indices).
VCCS	Voltage Controlled Current Source (ideal network theoretical element).

$VCCS_a$,$VCCS_b$	Names assigned to the VCCSs in a circuit with two VCCSs.
VCCS variable	Input voltage or output current of a VCCS, occuring in its I(V) relation.
Symbol	**Meaning**
$\mathbf{V_{GT}}$	Effective gate-source voltage of a MOST (V_{GS}-V_T).
$\mathbf{V_{IP2}}$, $\mathbf{V_{IP3}}$	2^{nd} and 3^{rd} order intercept current (extrapolated amplitude for HD2, respectively HD3, equal to 100%)
$\mathbf{V_P}$	Primary VCCS voltage variable (see above).
$\mathbf{V_T}$	Threshold voltage of a SVCCS or MOS Transistor (see also indices).
$\mathbf{V_{-TP}}$	Threshold voltage of a PMOST, defined ***positive*** for an enhancement MOST.
$\mathbf{V_\Sigma}$	Sum of VCCS input voltages V_a and V_b.
$\mathbf{V_\Delta}$	Difference of VCCS control voltages V_a and V_b.
$\mathbf{U_T}$	Thermal voltage k_BT/q.
W	Channel Width of a MOS Transistor.
$\mathbf{Y_t}$	Transadmittance from open-terminal source voltage to load current.
$\mathbf{Z_t}$	Transimpedance from short-circuit source current to load voltage.
α	Coefficient in KVL relation ($\alpha \in \{-1,0,1\}$); index refers to related voltage.
β	Coefficient in KCL relation ($\beta \in \{-1,0,1\}$); index refers to related current.
μ	Mobility.
θ	Mobility Reduction parameter.

Often used Indices

$[\,]_a$ $[\,]_b$	Quatity relating to $VCCS_a$ and $VCCS_b$ respectively.
$[\,]_{in}$ $[\,]_{out}$	Quantity relating to an input and output of a two-port respectively.
$[\,]_l$ $[\,]_s$	Quantity relating to a source and load respectively (or s- and l-branch).
$[\,]_v$ $[\,]_i$	Quantity relating to v- and i-branch of a VCCS respectively.
$[\,]_E$ $[\,]_L$ $[\,]_S$	Quantity relating to a EVCCS, LVCCS and SVCCS respectively.
$[\,]_N$ $[\,]_P$	Quantity relating to an NMOST and PMOST respectively.

1

Introduction

1.1 Motivation

During the last two decades, research in the field of analog CMOS circuits has gained a lot of interest. Continuous improvements in CMOS technology enabled the integration of (largely digital) complete electronic systems on a single chip. Usually, analog and mixed analog-digital circuits are now found at the interface of such systems with the "analog real world". Furthermore, analog signal processing can be favourable in terms of speed, chip area and power dissipation, especially for low and moderate precision circuits [11].

Linear circuits, like amplifiers and filters, are indispensable analog building blocks. Their properties often critically determine system performance. In order to achieve high performance, circuits are usually designed in such a way, that the transfer function is mainly determined by a few carefully chosen components. *Passive* components, especially resistors and capacitors, are predominantly used for this purpose. In this approach, *active* devices like MOS transistors, are used to provide sufficient gain. Ideally, they do not influence the transfer function. The underlying motivation is that passive devices are superior with respect to e.g. linearity, accuracy and noise.

Although the use of passive components is preferable in many cases, there are also drawbacks. A major one is that electronic control of the value of these components is hardly possible. Such control is often desired in order to compensate for deviations from nominal component values due to fabrication tolerances, temperature variations and ageing [9]. Without (self-)correction, these deviations will change the transfer function of linear circuits, e.g. resulting in a shift of the pass-band of a filter. Moreover, electronic control of the transfer function is needed in applications with varying signal conditions, e.g. to handle signals with a variable signal amplitude or frequency content.

Of course, it is possible to change the value of passive components in discrete steps, e.g. by means of MOS transistor switches. However, if the required resolution is high, this approach becomes impractical. Furthermore, the resistance of the switches often introduces problems and finally, the switching transients may give problems with full continuous-time signal processing.

Transconductance Based CMOS Circuits

Because electronic control is often needed, many MOST circuits with continuous electronic variability of the transfer function have been proposed [13]. The present thesis deals with circuits that rely on the *transconductance of a MOS transistor*. Instead of relying on passive components, *active devices* now have a *direct intended* effect on the *transfer function*. The transconductance of a MOST depends on gate geometry and biasing. Hence, designers both can dimension the nominal value of the transfer function, and adjust it electronically, as done in the well-known Transconductance-C filters [9]. Furthermore filters with an electronically programmable transfer function are feasible [23].

Although transconductors or V-I converters are probably the best known representatives of circuits based on the transconductance of a MOST, they are not the only ones. Linear circuits with an electronically variable I-V transfer characteristic, voltage amplification or current amplification have also been proposed [13]. In this thesis the collective noun *"transactors"* will be used for circuits that are connected between a signal source and load, transferring information sensed at the source to the load (non-zero transfer function) [21].

In addition to electronic control, there are some other features of transconductance based circuits that make them attractive solutions for certain design problems. Their simplicity often gives them good high-frequency performance. This is a major reason for the predominant use of Transconductance-C filters at high frequencies [9]. Furthermore, MOST transconductance values can be chosen in a very large range by means of gate geometry and biasing (example in chapter 3: 10^{-9} to 10^{-1} S). On the other hand, integrated resistors typically have values between 10 ohm and 100 Kohm. Transconductance based circuits can be a good alternative, e.g. in low power circuits with high impedance level. Finally, transconductor circuits often constitute "minimum complexity" implementations of a certain function, since a single MOST can often implement the desired transconductor. This makes them potentially suitable for massively parallel analog neural networks [11].

Present Thesis: Circuit Generation, Classification and Analysis

The present thesis deals with *linear transactors* based on the *transconductance* of MOS transistors. It aims at *generalisation* and *systematisation* of the design and analysis of these transactors. The main subjects that will be addressed are:

1. The *systematic generation* of linear transactor circuits by means of linear graphs.
2. The *classification* of these circuits in classes with common properties.
3. The *analysis* of important performance aspects of *classes of circuits*.

Although there are many papers on transactor circuits, the author is not aware of a generalised systematic treatment of the subject. Most publications focus on some aspects of one proposed circuit, with often only rather loose reference to other work. Apparently, it is often not realised that many circuits are "variations on a theme", having many properties in common. By looking less at circuit implementation details and concentrating on the *"functional kernel"* of circuits, such similarities can be made explicit. This is one of the objectives of this thesis. For the purpose of generalisation, a *Voltage Controlled Current*

Source (VCCS) will be introduced, to state explicitly that the transconductance is of crucial importance. Although most discussions relate to MOST circuit implementations, many results in this thesis can also be used for other transconductance implementations.

Many analog designers like to keep their circuits as simple as possible, and "squeeze" as much functionality as possible out of a small number of components. This is not only because of chip area, but also since extra components tend to add noise, increase the power consumption and worsen the HF behaviour. These considerations support a design philosophy aiming at a minimum circuit complexity, in which extra components are only added if justified by distinct performance improvements. In order to find the simplest possible implementation of a required function, an overview of *all possible* circuits, could be of great use. In this thesis *all graphs of two-port circuits consisting of two VCCSs are generated*.

It will appear that, even with two VCCSs, there are already several hundreds of circuit implementations. Fortunately, it is possible to create overview by *classifying* the circuits in a limited number of different classes. Circuits belonging to the same class share many properties and can be analysed in one run. This classification and analysis is performed in order to reach another aim of this thesis: to *predict the performance* of different transactors. Since symbolic design equations are of great help to designers, these will be used extensively. The resulting models can be considered as macro-models for transconductance based circuits.

To summarise, this thesis aims at a *generalisation* and *systematisation* of the design of transconductance based CMOS circuits. It is built on two main pillars:

1. The *generation of all graphs* of two-port circuits consisting of *two VCCSs*.
2. The *classification* of the resulting circuits in classes with common properties, that can be analysed in one run.

1.2 Analog CMOS Circuits: a Historical Overview

Before dealing with the actual subject of the thesis, first the existing literature on analog CMOS circuits will be shortly reviewed in order to place the subject in perspective. Although the overview is by no means exhaustive, it tries to identify some main-streams in the "river of papers" on the subject (for a more elaborate overview, see for instance [1], [20], [4], [5], [6], [9] and [13]).

CMOS IC technology evolved in the seventies from NMOS and PMOS processes as an attractive technology for the realisation of digital circuits. The availability of complementary enhancement N- and PMOS transistors results in a low static power dissipation. Together with the continuous reduction of feature sizes, this lead to the integration of more and more dense and complex digital circuits. However, up to the mid-seventies, analog integrated circuits were commonly implemented using bipolar transistor technologies.

Two circuit developments in the mid-seventies were very important for the progressive use of MOS technologies for analog circuits [5]: that of the precision-ratioed capacitor array and the internally compensated MOS operational amplifier. In combination with MOS switches, powerful switched capacitors circuits were devised which were used amongst others in novel A/D converters, PCM codecs and switched-capacitor filters [1],[6].

These early switched-capacitor circuits were often used in stand-alone chips. MOS technology was used because it offered possibilities to exploit specific properties of MOS transistors that were difficult to implement with bipolar processes. However, towards the beginning of the eighties, a new motivation for the use of analog MOS circuits evolved. By that time the integration of large digital electronic systems on a single chip became feasible. These systems can be cheaper, smaller and more reliable, if the analog and mixed analog-digital interface circuits are integrated on the same chip. As a result, analog and mixed analog-digital CMOS circuit research was stimulated. Now, MOS transistors were not used primarily because of their attractive properties, but just since they are the only active devices available in digital CMOS technologies. The challenge remained to find concepts that take advantage of the properties of MOS transistors.

Since switched-capacitor circuits use sampling techniques, they are subject to the Nyquist constraints and need anti-aliasing and smoothing filters. Furthermore, the switched noise aliases into the baseband, deteriorating the signal to noise ratio. Finally the high-frequency potential is limited. These problems were an important motivation for the development of continuous-time MOS filter techniques. The two main approaches are often denoted as "MOSFET-C" filters and "G_m-C filters" [9]. In MOSFET-C filters a MOST in the triode region is used as a resistor, constituting an integrator together with a capacitor and an OPAMP. In G_m-C filters, a transconductor usually based on the transconductance of a MOST, together with a capacitor are used as an integrator. In both types of filters, the integrator time-constant is electronically variable since both the drain-source resistance and the transconductance of a MOST depend on its biasing point. Because of these filter developments, the design of linearised MOS transconductors and resistor circuits became a popular research topic [38-131]. A lot of these circuits are based on the approximate square-law characteristic of a MOS transistor operating in strong inversion and saturation, given by:

$$I_D = k \cdot \left(V_{GS} - V_T\right)^2 \tag{1.1}$$

where I_D is the drain current of a MOS transistor, V_{GS} is the voltage between the gate and source, k is the conversion factor of the MOST and V_T is the threshold voltage. To the best of the authors knowledge, analog four-quadrant multipliers were the first circuits to explicitly use this square-law characteristic. An early publication in 1972 [132] describes a multiplier core existing of 6 MOS transistors. In 1979 a direct-coupled MOS squaring circuit was proposed [133], suitable for the implementation of multipliers according to the "quarter-square principle", well-known from analog computers [154]:

$$\frac{1}{4} \cdot \left((a+b)^2 - (a-b)^2 \right) = a \cdot b \tag{1.2}$$

With two squaring circuits a multiplier can be made. Alternatively, the quarter-square principle can be used to implement V-I converters, by keeping one input of the multiplier constant. This and also other techniques that exploit the square-law characteristic, were the starting point for the design of several early linear V-I converter circuits [38,40,49]. Later, also circuits with a linear current gain, were proposed [61]. The above mentioned circuits will be discussed in more detail in chapter 8. Another application of the square-law characteristic was found in non-linear circuit synthesis [141,145,147,106].

Apart from the use of the square-law relation eqn. (1.1), transconductors can also be implemented using MOSTs operating in the triode region [41]. Usually the following simplified model is used for circuit synthesis:

$$I_D = 2 \cdot k \cdot \left(\left(V_{GS} - V_T \right) \cdot V_{DS} - \tfrac{1}{2} \cdot V_{DS}^2 \right) \tag{1.3}$$

Two different approaches can be distinguished: in the first one, the drain-source conductance dI_D/dV_{DS} is used, while in other case the transconductance dI_D/dV_{GS} is exploited. However, in both cases additional cascode stages are needed, as the output resistance of a triode MOST is rather low, while a transconductor should have a high output resistance.

Linear circuits using MOS transistors operating in the weak inversion region have also been proposed [28]. The MOST has an exponential characteristic in this region which maximises the transconductance for a given current. Furthermore the exponential characteristic enables the design of translinear circuits as proposed by Gilbert [145]. However, the price paid in terms of speed and noise is rather high, which mainly limits the application to low precision, low power and low voltage applications.

A more recent development in analog CMOS circuit design is the conception of switched-current circuits as a replacement for switched-capacitor circuits [157]. In this approach the gate-source capacitance of a MOST is used as a charge storage element, while its drain current is used as the output variable. Together with MOST switches, effectively a kind of "current memory" results, which allows current copiers and filter functions to be implemented.

To summarise, continuous innovations have occurred in the field of analog CMOS circuit design during the last two decades. Many advances in this field were established by exploiting the intrinsic properties of the MOST device to advantage. Thus it has been proposed to use a MOST as a switch, an amplifier, an electronically variable linear resistance, a sampling capacitance and a voltage controlled current source with a linear, square-law or exponential characteristic. In a field of research with turbulent changes, a lot of "first shot" ideas are generated and published, which are sometimes not very useful on second thought. Hence, although the challenge certainly remains to find new concepts, it is also very useful to aim at a consistent description and generalisation of already proposed circuits, and a critical evaluation of the performance that can be achieved. This thesis is an attempt to do this for circuits, based on the transconductance of a MOS transistor.

1.3 Outline of the Thesis

The outline of this thesis is described below.

Chapter 2: Requirements and Design Techniques for Linear Transactors

Chapter 2 starts with a discussion on the need for linear signal processing and the requirements to be posed on linear transactors as building blocks. Useful transactors are then defined, mainly from the viewpoint of optimum information transfer as proposed in [21]. Furthermore, the suitability for self-correcting or programmable systems and the compatibility with voltage-mode and current-mode signal processing are considered. This results in the definition of 9 useful transactors, which are formally defined as two-ports described with transmission parameters. The useful cases have port impedances that are either very low, very high, or well-defined. Transmission parameters should either be accurately determined or electronically variable. After these functional considerations, important performance aspects of linear transactors are defined, starting from fundamental limitations that threaten high quality signal transfer. Finally, existing design techniques to cope with these threats are discussed, especially the use of negative feedback.

Chapter 3: Generation of All Graphs of Transactors with Two VCCSs

Chapter 3 deals with the possibilities to implement the 9 desired linear transactors by means of the transconductance of MOS Transistors. It is shown that a MOS Transistor, operating under certain conditions, can be considered as a Voltage Controlled Current Source (VCCS) with an electronically variable transconductance. Depending on its operating region an approximate linear, square-law or exponential I(V) characteristic is found ("Generalised VCCS-models"). Using *two* of these *VCCSs* as building blocks, *all possibilities* to implement linear transactors are systematically explored using *linear graphs*. For this purpose a graph generation and analysis program has been developed. In this way 145 potentially useful VCCS graphs are found. Furthermore, it is shown that the 9 useful transactors defined in chapter 2, can either be implemented directly or at least approximated. Finally practically achievable values of the transmission parameters of transactors and their electronic controllability are examined.

Chapter 4: Application Examples I

Chapter 4 shows how the results of chapter 2 and 3 can be used to design circuits. First transistor level implementations of VCCS graphs are considered. It appears that common-source MOST-pairs can always be used to implement a VCCS. Depending on the connections and orientations of branches in the graphs, sometimes single MOSTs or even resistors can also be used. With this knowledge, the possibilities to implement often used transactors, like transconductors, current amplifiers, transimpedance amplifiers and voltage amplifiers are examined. Several well-known, but also less familiar circuits are systematically generated in this way. Finally the design of an impedance matching AGC-amplifier-stage is considered in detail. The design requirements are analysed, and VCCS graphs satisfying the requirements are found. These graphs are then implemented using MOST differential pairs and compared with respect to several important performance

criteria. It appears that significant differences in performance exist, but that the desired specifications are not achieved. In order to understand and improve the performance, design equations that relate performance to design parameters are useful. It is concluded that automation of the derivation of such equations is desirable, because of the large number of VCCS graphs to be considered.

Chapter 5: Classification of Circuits with Two VCCSs

Chapter 5 gives an answer to the need for automated analysis of design equations by means of a systematic classification method. The large number of circuits found in chapter 3 is classified in a limited number of classes, based on sets of two independent Kirchhoff relations. Since circuits belonging to the same class share properties, they can be analysed in one run. Furthermore, the *classification* provides an *overview*, as it *covers all possible different ways of using two VCCSs*. It appears that some of the circuits with two VCCSs can be considered as two independent circuits with each one VCCS ("*1VCCS- circuits*"). In other cases this is not possible ("*2VCCS circuits*"). The 1VCCS and 2VCCS circuits are formally defined and divided in classes: two classes result for the 1VCCS circuits, and 3 main classes and 14 subclasses for the 2VCCS circuits. As an example of the usefulness of the classification, the transfer functions of all 2VCCS circuits are analysed in only three analysis runs. Chapter 5 ends with a discussion on the relation between VCCS graphs and transmission parameters on the one hand, and the classification based on Kirchhoff relations on the other hand. Finally limitations of the analysis techniques based on the proposed classification are discussed.

Chapter 6: Large Signal Characteristics of 2VCCS Circuits

Chapter 6 deals with the analysis of the large signal transfer characteristics of 2VCCS circuits, for the cases of the linear, square-law and exponential VCCSs. Design equations are derived to estimate the biasing point, and determine the transmission parameters in this biasing point. Using these equations the current consumption, tuning range, and limits to the input and output swing can be determined, as well as trade-offs between them. On the fly also some useful non-linear circuits are discussed. The second subject of chapter 6 is the estimation of the non-linearity of 2VCCS circuits in the weakly non-linear region, based on third order Taylor series approximations. Estimation formulas for the distortion of different VCCS circuits are derived and discussed.

Chapter 7: Noise Analysis of 2VCCS Circuits

In order to estimate the dynamic range of a transactor, apart from distortion, noise is important. Therefore, chapter 7 analyses the noise performance of transactors implemented with two VCCSs. Again the classification presented in chapter 5 is of great use to automate the noise analysis.

Chapter 8: Application Examples II

Chapter 8 discusses applications of the results of the chapters 5, 6 and 7. First the classification is applied to transconductance based circuits, described in literature. It is shown that many of them are implementations of a limited number of 2VCCS classes.

Therefore they share at least certain fundamental limitations. Then the dynamic range of all possible V-I converter Kernels with two matched MOSTs is analysed and compared, as an example of the usefulness of the classification and analysis of 2VCCS circuits. Finally, the impedance matching AGC-amplifier example of chapter 4 is considered again. An attempt is made to predict the performance of different amplifier designs using symbolic expressions and to find clues for design improvements.

Chapter 9: Summary & Conclusions

In chapter 9 conclusions are drawn and the original contributions of this thesis are summarised. Finally recommendations for further research are given.

2

Requirements and Design Techniques for Linear Transactors

2.1 Introduction

This chapter deals with linear transactors, used as building blocks for linear signal processing, with two aims. The first aim is to find out which *requirements* a transactor has to fulfil to be useful for linear signal processing. The second aim is to give a brief overview of *existing design techniques* used to implement linear building blocks, in order to place the circuits presented in this thesis in perspective. Furthermore, quality criteria that can serve to evaluate these merits are discussed.

The chapter starts with a short discussion on what linear signal processing is and why it is useful. Then, the desired signal transfer of building blocks is dealt with from three points of view: firstly the adaptation to the signal source and load, secondly the desired transfer function and thirdly, the compatibility with voltage-mode and current-mode signal processing. Having established the ideal signal transfer, causes of deviations from this ideal behaviour are identified.

The discussion concerning the signal source and destination and quality criteria is based on the work of Nordholt [21] and Davidse [24]. It is partly repeated here in order to make the basic considerations of their work explicit. This is especially important since this thesis deviates from some of these assumptions.

2.2 The Need for Analog Linear Signal Processing

Linear signal processing can be described as performing linear operations on electrical signals. Within the field of analog CMOS circuits, time-continuous linear circuits play an important role. Some reasons for this will be shortly discussed, in order to have an idea of application areas of these circuits.

2.2.1 Interface to the Analog World

Amplification is an indispensable Analog function in order to decrease the contaminating effect of noise and interference [24]. The term "noise" is generally used to indicate the stochastic variations that fundamentally accompany all physical processes. The term interference is used to indicate unwanted signals, that may pollute the signal, e.g. by means of parasitic capacitive or inductive coupling to signal paths. Analog signals that come from the outside world for instance by means of sensors are often weak. Since operations on the signal will add noise, the ratio between the signal power and the noise power (S/N ratio) and thus the quality of the information is at danger. By amplification of weak signals, the signal power can be kept well above the noise power, and the information is only slightly disrupted. A similar reasoning holds for the ratio of the signal level to the interference level.

Apart from low noise amplification, an important function of analog circuits is to provide energy to actuators with high efficiency. Furthermore anti-aliasing and reconstruction filtering are often needed analog interface functions. Thus, in the majority of cases where a sensor or actuator is used, analog circuits are indispensable.

2.2.2 Spectral Bandwidth Scarcity

A further reason for the need for linear analog signal processing is the ever increasing need for electronic information transfer, while spectral bandwidth is a scarce commodity. Therefore, many signals are transmitted simultaneously via the same communication channel using different frequency bands with preferably a minimum use of bandwidth. The use of analog signals has in principle advantages in this case, since for a given bandwidth, much more information can be transferred than with a binary valued signal, especially for channels with large S/N ratio [152]. On the other hand, the growing use of digital data compression techniques often result in acceptable use of bandwidth, even for binary valued signals. However, for applications with a given limited bandwidth, the use of analog signals may be mandatory (e.g. high-speed modems using a standard telephone channel).

For the separation of the different frequency bands and compensation of communication channel non-idealities, analog filtering techniques are essential. At the high frequencies which are often involved, analog time-continuous filtering is often the only feasible solution. Furthermore, although there is a clear tendency to do more and more filtering using digital filters, at least analog anti-aliasing filtering remains required. For this purpose linear analog building blocks remain important.

2.2.3 Digital Solution not Feasible or not Effective

Although digital circuits replace many kinds of traditionally analog circuit applications, they can not replace analog circuits in all cases. Especially for applications that require high operating frequencies and large dynamic signal ranges (e.g. antenna signal strengths varying from μVolts to Volts), analog implementations are often (still) the only feasible solution for a large part of the signal path.

In other cases, both analog and digital solutions are possible, but analog is preferred because of lower chip-area and power-dissipation. An analog signal with a given dynamic range, can alternatively be represented with a n-bit digital word, where n increases with roughly 1 bit for every 6 dB of dynamic range. However, the functional density of analog circuits is in general much higher. A simple low-pass filtering operation can for instance be performed by a few MOSTs and a capacitor, while its digital equivalent may take several hundreds of transistors, depending on the required dynamic range (number of bits). For low dynamic ranges, the higher functional density also results in a lower power dissipation [10]. However, the power dissipation increases linearly with the dynamic range, while it only grows logarithmically for the digital case. For a 1µCMOS technology a typical break-even-point may be a dynamic range of 60dB. However, the break-even-point changes in favour of digital circuits for newer CMOS-technologies.

Thus, especially in systems with low or moderate dynamic range requirements, analog implementations are often more effective in terms of chip area and power. An application area in which this effectiveness may be a compelling reason to choose for analog is in massively parallel perception circuits [11] and other neural networks [164]. Furthermore, in systems that require a modest amount of signal processing, going from analog to digital and back again may result in a lot of overhead, which can also be a good reason to choose for an all analog design.

2.3 Linear Transactors: Function and Requirements

In order to simplify the design process of electronic systems, the "divide and conquer" strategy is often used: the system is partitioned in smaller parts, down to the level of designable building blocks. Linear transactors are such building blocks used for linear signal processing operations. This paragraph discusses their function and requirements, based on three points of view: the adaptation to the signal source and load, the desired transfer function and the compatibility with voltage- and current-signals.

2.3.1 Adaptation to the Signal Source and Load

Linear transactors operate on electrical signals, which represent information that has to be transferred from a source to a load. The actual information that they represent is often non-electrical, for instance a physical quantity like a sound pressure or a temperature. Since the information is of primary importance, optimum information transfer should be the aim. Thus during the design of electronic circuits, the crucial question should be: what is the *"best reproducing relation"* between an input quantity and an output quantity [21]. Thus, the electrical quantity that has the best linear and accurate relation to a physical quantity should be decisive for the choice of the linear transactor.

A general representation of a linear transactor and its environment is given in Figure 2-1, where it is represented by a linear two-port, with an input port and output port with voltages and currents labelled V_{in}, I_{in}, V_{out} and I_{out}. The information source is represented by a voltage source with voltage V_s and a source impedance Z_s and the information receiver by a load impedance Z_l. In general the signal transfer from the input port to the output port

will now be determined by: (1) the source impedance Z_s, (2) the load impedance Z_l, and (3), the two-port parameters. The key question is now: what is the best reproducing relation between the input and output quantities?

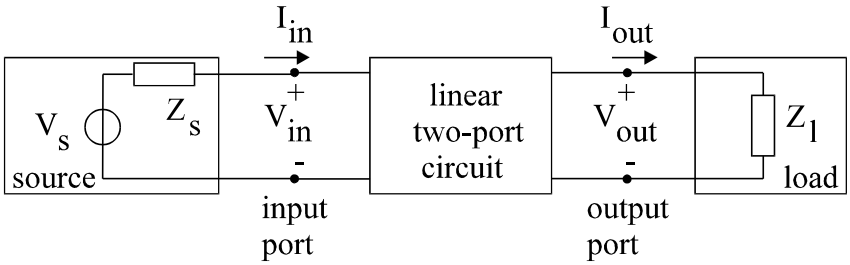


Figure 2-1: A linear two-port connected between a source and load.

An important item in this respect is the source impedance Z_s. This impedance may be non-linear and/or inaccurate, so that it is not acceptable that the transfer function depends on it. Furthermore it is sometimes intolerable to withdraw energy from a signal source [19] (e.g. when the signal source is a sensor, energy flow may disturbs the measurement process in which the sensor is involved). Both requirements can be met if $I_{in}=0$ or $V_{in}=0$. In the first case the source voltage is sensed without current flow, implying an infinite input impedance of the amplifier (see Figure 2-2a). In the second case the source current is sensed without voltage drop, implying zero input impedance of the amplifier (see Figure 2-2b, with a Norton equivalent circuit representation of the signal source). In both cases the source impedance does not influence the transfer function and the energy withdrawn from the source is zero. If the source impedance is linear and accurately known, and withdrawing energy from the source is no problem, than an amplifier with a linear and accurately known input impedance Z_{in} can be used (see Figure 2-2c). The value of Z_{in} can then be chosen equal to Z_s in order to avoid power reflection, which may be required in characteristic impedance systems. Alternatively, other optimisation criteria may exist.

Obviously, port impedances of zero and infinity can only be approximated in practical circuits. In practice, the design objective will be to realise a certain application dependent ratio between the port-impedance and the source or load-impedance, where the ratio is, for instance, derived from accuracy considerations.

With respect to the influence of the load impedance on the overall transfer function, a similar chain of reasoning as for the source impedance can be followed. This leads to the conclusion that Z_l has no influence if the two-ports output impedance is either very high or very low. Also, if Z_l is linear and accurately known, a two-port with a linear and well-determined output impedance can be used.

Thus it can be concluded that two-ports with port impedances that are either high or low compared to the source and load impedance are particularly useful for linear signal processing. Furthermore two-ports with a linear, accurately known port impedance can be useful in some applications (e.g. characteristic impedance matching).

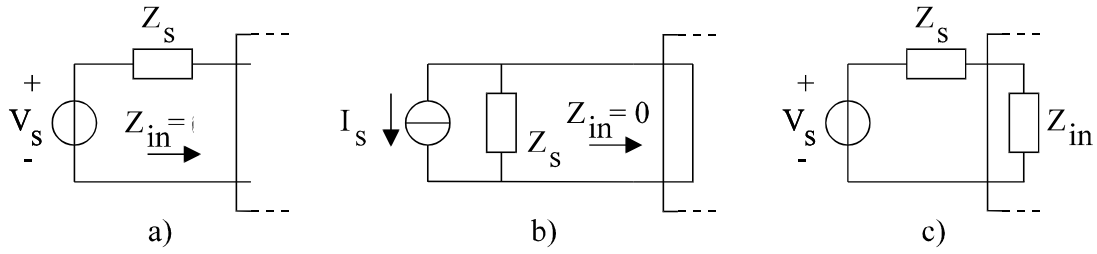


Figure 2-2: Useful adaptations of the two-port input impedance Z_{in} to the signal source impedance Z_s: voltage sensing (a), current sensing (b) and impedance adaptation (c). In a similar way Z_{out} can be adapted to the load impedance.

2.3.2 Desired Transfer Function

Apart from the adaptation to the source and load impedance, a linear transactor should have a well-defined prescribed transfer function. The exact specifications depend strongly on the application of the circuit and the type of signals to be processed. However, if we confine ourselves to linear time-invariant circuits, it can be shown that all finite time-invariant circuits can be generated from a finite number of resistors, capacitors, inductors, transformers, and gyrators [151]. Thus, if these "generating elements" are either readily available, or can be replaced by equivalent circuits with the same behaviour, in principle all required functions can be implemented.

Different sets of generating elements satisfy this requirement, yet the most widely used one is probably the set consisting of the operational amplifier, the capacitor and the resistor. However, an alternative set consists of the differential voltage controlled current source in conjunction with a capacitor [18]. Moreover, since this building block often has an electronically variable transconductance, it can easily be made time variable so that linear time-variable circuits can also be generated. Apart from the above discussed possibilities, other linear circuit building blocks have been proposed, e.g. a current controlled current source, current controlled voltage source, current conveyer [16,17], OFA and OMA [19,26]. Despite of all the differences, a common aim can be distinguished in all of these approaches: a transfer functions, depending on as less component parameters as possible. To reach this aim, the building blocks ideally have zero or infinite port impedances. As discussed in the previous paragraph, the transfer function is then entirely determined by a few carefully chosen components. Unfortunately, striving for zero or infinity has its limitations, as we will discuss in section 2.6.

An aspect that has not been addressed until now is the uni-lateralness of a building block. A uni-lateral circuit is a circuit with a one-directional transfer function from input to output (the reverse transfer function is zero). Uni-lateralness is a useful property of a building block, since it minimises the interaction between cascaded building blocks, and thus simplifies design. Although practical circuits have a non-zero reverse transfer function, they can often be designed in such a way that it is much smaller than the forward transfer function.

The set of generating elements actually used by designers does not only depend on their properties, but also on aspects like designers knowledge and design experience and available cell libraries and CAD tools. Nevertheless, the performance that can be achieved with building blocks, taking into account practical non-idealities that hamper the "equivalence" with ideal network elements, is very important. Since some realisations of a function are more bothered by imperfections than others, this may lead to distinct preferences for certain application areas. Considering for example the design of active integrated filters, for lower frequencies usually MOSFET-C circuits are encountered [44], while for high frequencies Transconductance-C filters are commonly used [9]. This is mainly because opamps with both a high gain and a large bandwidth are hard to design, while transconductors with a good high-frequency behaviour are quite feasible.

Summarising, it appears that different sets of building blocks can be used to implement linear transfer functions. The set of a differential VCCS and a capacitor is one of the possibilities. Furthermore, in general linear circuits are designed in such a way that their transfer function depends on a minimum number of component parameters. Again building blocks with either a high or a low input and output impedance appear to be useful to reach this aim.

2.3.3 Suitability for Self-correcting or Programmable Systems

In the previous paragraph it was mentioned that the transfer function of a linear transactor should be accurately known. In practice systematic and stochastic variations occur due to component parameters variations, e.g. because of IC processing tolerances and temperature variations. However, the development of so-called self-correcting, self-compensating, or self-calibrating techniques, has helped to overcome errors traditionally associated with time-continuous analog circuits like offset, low-frequency noise, and the above mentioned parameter variations [5]. As discussed in the motivation in chapter 1, the application of these techniques requires transactors with electronic variability or digital programmability.

Apart from using the tunability to establish a desired nominal performance, the tuning possibilities can also be used to implement circuits with a time-variable transfer function. This can be used to adapt the transfer function to the users desire in an electronic programmable way. Furthermore circuits that adapt their transfer function dependent on the incoming signal are possible (e.g. automatic gain control circuits or channel equalisers). Especially in mixed A/D systems, it is often desired that the analog part is to some extend controllable or programmable.

Thus it can be concluded that electronic control of the transfer function of a linear transactor is a useful feature for self-correcting and programmable linear circuits.

2.3.4 Voltage-mode and Current-mode Compatibility

In principle it is possible to perform linear signal operations in the voltage and current domain, referred to as voltage-mode and current-mode signal processing. However, certain operations are easier on voltage variables and others on current variables. To illustrate this

point, the linear operations addition, distribution, integration and differentiation will be considered with reference to Figure 2-3.

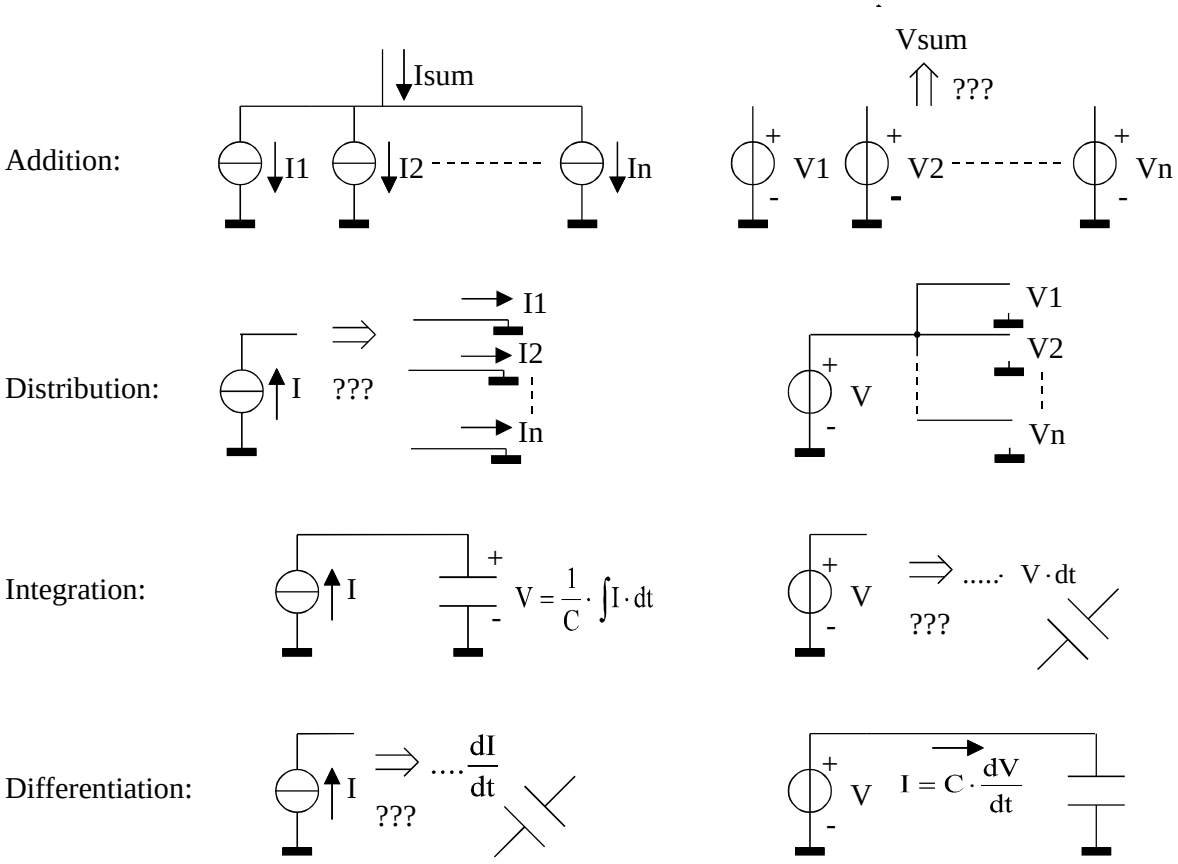


Figure 2-3: Some operations are easier on voltages, while others are easier on currents.

The following observations can be made:

- Addition is easy if signal sources can be represented as current sources: by just connecting the sources to a summing node the addition is performed. Addition of voltages requires floating voltage sources, which are hard to realise. Subtraction is possible by means of sign inversion (multiplication by -1) and addition.
- On the other hand, distribution of a signal to several single ended inputs of multiple circuits is easily done by just connecting the inputs together. Distribution of a current to more nodes involves copying the current, which is more complex.
- Integration of a current variable over time is easy: the voltage across a capacitor is proportional to the integral of the current flowing through that capacitor. Integrating a voltage variable would be possible using an inductor, yet these can hardly be integrated on a chip. Thus integrating a voltage variable generally involves some kind of voltage to current conversion, followed by an integration of the resulting current variable.
- Differentiation of a voltage variable is easy by means of a capacitor: the current through a capacitor is proportional to the derivative of the capacitor voltage with respect to time. Again, an inductor could in principle perform the differentiation for currents, which is however not practical on a chip. Thus differentiating a current generally

requires some form of current to voltage conversion, followed by differentiation of the resulting voltage variable.

From the above considerations it appears that choosing the appropriate variables makes the implementation of some linear operations easier. Of coarse the above discussed operations can always be performed on either voltages or currents, by using additional V-I or I-V converters. However, this leads to an increase in circuit complexity and, moreover, additional non-idealities like noise, distortion and inaccuracies introduced by the extra conversions.

Thus it appears that in some cases there is a preference for voltage-mode and in other cases for current-mode signal processing. As a consequence, a useful set of building blocks should preferably include blocks that are compatible with both types of variables.

2.4 Transactors suitable for Linear Signal Processing

Based on the discussion in the previous paragraphs, a set of transactors suitable for linear signal processing will now be defined, formally described as two-port.

2.4.1 Suitable Two-ports

Based on the results of paragraph 2.3, two-ports suitable for linear signal processing can be defined in terms of their port impedances and their transfer function.

The source and load characteristics ask for either a low, a high or an accurately known linear impedance for the two-port input and output ports. These three types of input and output port impedances lead to 9 different useful transactors, shown in Figure 2-4 and Table 2-1. Using voltage or current sensing, the entire source voltage or source current is sensed, while for the impedance adaptation case a fraction of the source current or voltage is sensed, depending on the input impedance. If $Z_{in}=\alpha_{zi}\cdot Z_s$, then V_{in} and I_{in} are given by:

$$V_{in} = \frac{\alpha_{zi}}{1+\alpha_{zi}} \cdot V_s \tag{2.1}$$

$$I_{in} = \frac{1}{1+\alpha_{zi}} \cdot I_s \tag{2.2}$$

Clearly, for $\alpha_{zi}=1$, one to one impedance adaptation of the two-port to the source takes place, resulting in maximum power transfer and a voltage and current attenuation of a factor 2. Eqn. 2.1 and eqn. 2.2 also show that for α_{zi} going from zero to infinity the two-port behaviour gradually changes from current sensing to voltage sensing.

For the output port a similar reasoning holds, resulting in either a complete transfer of the output voltage or current to the load or a partial transfer in case of impedance adaptation. If $Z_{out}=\alpha_{zo}\cdot Z_l$, then V_{out} and I_{out} are given by:

$$V_l = \frac{1}{1+\alpha_{zo}} \cdot V_{out} \tag{2.3}$$

$$I_l = \frac{\alpha_{zo}}{1+\alpha_{zo}} \cdot I_{out} \tag{2.4}$$

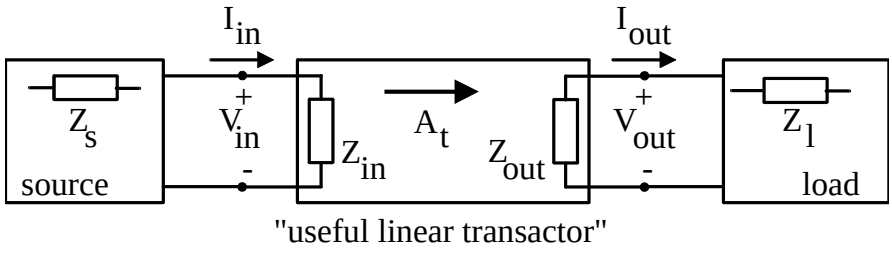


Figure 2-4: Useful linear transactors have port impedances adapted to the source and load impedance (see Table 2-1) and a transactance A_t which is uni-lateral.

Based on the above mentioned adaptation possibilities, the processed signal is a voltage in case of voltage sensing and a current in case of current sensing. For the impedance adaptation case, it doesn't matter which variable is chosen, since voltage and current are linearly related by the port impedance. To represent the output signal, either a voltage source or current source can be used, where again the choice is immaterial for the linear port impedance case. This leads to 4 basically different types of transfer functions from source to load, listed in the last column of Table 2-1.

Input port impedance Z_{in}	**Output port impedance Z_{out}**	**Transactance A_t**
$>> Z_s$	$<< Z_l$	$A_v = V_l / V_s$ (voltage-gain)
$>> Z_s$	$>> Z_l$	$Y_t = I_l / V_s$ (transadmittance)
$<< Z_s$	$<< Z_l$	$Z_t = V_l / I_s$ (transimpedance)
$<< Z_s$	$>> Z_l$	$A_i = I_l / I_s$ (current-gain)
$= \alpha_{zi} \cdot Z_s$	$<< Z_l$	A_v or Z_t
$= \alpha_{zi} \cdot Z_s$	$>> Z_l$	A_i or Y_t
$>> Z_s$	$= \alpha_{zo} \cdot Z_l$	A_v or Y_t
$<< Z_s$	$= \alpha_{zo} \cdot Z_l$	A_i or Z_t
$= \alpha_{zi} \cdot Z_s$	$= \alpha_{zo} \cdot Z_l$	A_v, Y_t, Z_t or A_i

Table 2-1: Two-ports that are useful for linear signal processing (see also Figure 2-4).

These transfer functions are:

1. Voltage-gain: $$A_v = \frac{V_l}{V_s} \tag{2.5}$$
2. Transadmittance: $$Y_t = \frac{I_l}{V_s} \tag{2.6}$$
3. Transimpedance: $$Z_t = \frac{V_l}{I_s} \tag{2.7}$$
4. Current-gain: $$A_i = \frac{I_l}{I_s} \tag{2.8}$$

In order to refer to one or more of the above defined transfer functions, the term transactance will be used in this thesis.

Looking back to the requirements defined in section 2.3, we can conclude that the requirement of adaptation to the source and load impedance is satisfied. Moreover, the different types of port impedances also establish the compatibility with voltage and current signals. In general, it is desired that the transactance has an accurately determined value. Alternatively, in a self-correcting system, the transactance value should be tuneable over a sufficient range to compensate for the influence of practically occurring variations in IC processing and temperature. In programmable systems, it depends on the application how large the tuning range needs to be.

Summarising, it appears that 9 useful transactors can be defined with either very high, very low, or linear and accurate port impedances. The thus implemented transactances are: voltage gain, transadmittance, transimpedance and current gain. The transactance should either have an accurate value, or be electronically variable.

2.4.2 Two-port Description using Transmission Parameters

In order to describe the transactor as a linear two-port, 6 sets of two-port parameters can be used [150]. In this thesis transmission parameters (also called chain parameters) will be used. As illustrated in Figure 2-5, the input voltage and input current of a two-port are related to the output voltage and current according to:

$$V_{in} = A \cdot V_{out} + B \cdot I_{out} \tag{2.9a}$$

$$I_{in} = C \cdot V_{out} + D \cdot I_{out} \tag{2.9b}$$

Note that the direction of I_{out} is opposite to the usual direction adopted in network theory, because of historical reasons.

At first glance it might look strange to describe input quantities as a function of output quantities (this is sometimes called anti-causal). However, designers are quite familiar with the reciprocal values of the transmission parameters:

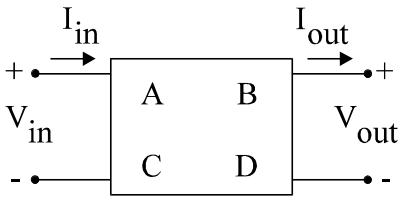
Voltage-gain factor: $$\mu = \frac{1}{A} = \left(\frac{V_{out}}{V_{in}} \right)_{I_{out}=0} \tag{2.10}$$

Transadmittance: $$\gamma = \frac{1}{B} = \left(\frac{I_{out}}{V_{in}} \right)_{V_{out}=0} \tag{2.11}$$

Transimpedance: $$\zeta = \frac{1}{C} = \left(\frac{V_{out}}{I_{in}} \right)_{I_{out}=0} \tag{2.12}$$

Current-gain factor: $$\alpha = \frac{1}{D} = \left(\frac{I_{out}}{I_{in}} \right)_{V_{out}=0} \tag{2.13}$$

Note that the above formulas contain two-port input and output variables and not source and load quantities as for the transactance definitions eqn. 2.5-2.8.



$$\begin{pmatrix} V_{in} \\ I_{in} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \cdot \begin{pmatrix} V_{out} \\ I_{out} \end{pmatrix} \tag{2.14}$$

Figure 2-5: Linear two-port modelled with transmission parameters.

The transmission parameter description is naturally suited to describe a cascade or chain connection of two-ports, which we will encounter later on. Moreover, all of the 9 useful transactors of Table 2-1 can be described with transmission parameters. In case of y-, z-, h- or g- parameters, the 4 cases of ideal controlled sources (zero or infinite port impedances) can only be described by one of these sets. For a VCCS with transconductance g for instance, only g-parameters exist ($I_{in}=0$, $I_{out}=g \cdot V_{in}$). However, transmission parameters also exist ($V_{in}=I_{out}/g$, $I_{in}=0$).

2.4.3 Linear Transactor Design Objective

In the previous section, transmission parameters were introduced as a means to formally describe linear two-ports. In this section, the port impedances and transfer function of a linear transactor will be analysed using the transmission parameter representation. The design objectives for useful linear transactors, as defined in section 2.4.1, are then expressed in term of transmission parameter requirements.

Using the transmission parameters to describe a linear transactor, the transfer function from a source via a transactor to a load can be calculated. For a voltage source as shown in Figure 2-6a this leads to a voltage gain and a transadmittance given by:

$$A_v = \frac{V_l}{V_s} = \frac{Z_l}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s} \tag{2.15}$$

$$Y_t = \frac{I_l}{V_s} = \frac{1}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s} \tag{2.16}$$

For a current source as shown in Figure 2-6b the results are a transimpedance and current gain given by:

$$Z_t = \frac{V_l}{I_s} = \frac{Z_s \cdot Z_l}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s} \tag{2.17}$$

$$A_i = \frac{I_l}{I_s} = \frac{Z_s}{A \cdot Z_l + B + C \cdot Z_s \cdot Z_l + D \cdot Z_s} \tag{2.18}$$

In both cases the input and output impedance of the two-port which is connected to the source and load can be expressed as:

$$Z_{in} = \frac{A \cdot Z_l + B}{C \cdot Z_l + D} \tag{2.19}$$

$$Z_{out} = \frac{B + D \cdot Z_s}{A + C \cdot Z_s} \tag{2.20}$$

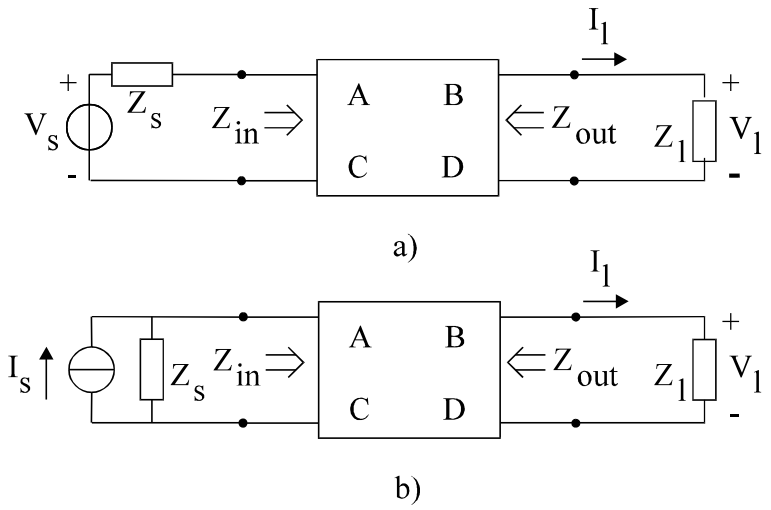


Figure 2-6: Linear transactors modelled as linear two-ports connected to a voltage source (a) or current source (b).

The above relations show how the transmission parameters and the source and load impedance value influence the transactances and port impedances. In section 2.4.1, useful transactors were defined in terms of port impedance requirements. The question to be answered now, is how the transmission parameters should be chosen to satisfy these requirements. Table 2-2 summarises the results.

The input and output impedance of the transactor are given in eqn. 2.19 and 2.20. By nullifying certain transmission parameters, both zero and infinite impedances can be established: zero if the numerator of the impedance expressions is zero, and infinity if the denominator is zero. For example, Z_{in} given in eqn. 2.19 becomes zero if A and B are zero, and infinite if C and D are zero. In order to acquire an accurate impedance, at least two transmission parameters should have a well-determined value. In case of Z_{in}, for example, parameter A or B should be non-zero, and also parameter C or D. In some of the cases, e.g. non-zero A and D, Z_l influences the input impedance, which is only acceptable if the load impedance is linear and accurately known. This can, however, be avoided by fixing a well chosen set of transmission parameters: if, for example, only A and C are non-zero, then Z_l is dropped (Z_{in}=A/C). Alternatively B and D can be chosen (Z_{in}=B/D). A third, more involved, possibility is to choose the ratio A/C equal to ratio B/D (Z_{in}=A/C=B/D).

For the output impedance similar considerations hold, leading to the useful combinations B and A (Z_{out}=B/A), D and C (Z_{out}=D/C) and B/A equal to D/C (Z_{out}=B/A=D/C). Fortunately, the condition for an accurate input impedance does not preclude an accurate output impedance: both are simultaneously possible if A·D=B·C. Thus transactors with both an accurate input and output impedance, independent of the source and load impedances, are possible. However, this requires fixing all four transmission parameters, which can be rather complex to implement. If this is, for instance, done by means of feedback, every parameter that needs to be fixed corresponds to a additional feedback loop [21]. In the next chapter it will be shown how this can alternatively be done by means of the transconductance of MOSTs.

Desired Transactor Properties	Measures taken to fix Z_{in}	Measures taken to fix Z_{out}	Measures taken to fix the Transactance
$Z_{in}=\infty$, $Z_{out}=0$, A_v	C=0, D=0	B=0, D=0	$A = 1/A_v$
$Z_{in}=\infty$, $Z_{out}=\infty$, Y_t	C=0, D=0	A=0, C=0	$B = 1/Y_t$
$Z_{in}=0$, $Z_{out}=0$, Z_t	A=0, B=0	B=0, D=0	$C = 1/Z_t$
$Z_{in}=0$, $Z_{out}=\infty$, Y_t	A=0, B=0	A=0, C=0	$D = 1/A_i$
$Z_{in}=\alpha_{zi}\cdot Z_s$, $Z_{out}=0$, A_v or Z_t $(=A_vZ_s)$	$\frac{A}{C}=\alpha_{zi}\cdot Z_s$	B=0, D=0	$A=\frac{\alpha_{zi}}{A_v\cdot(1+\alpha_{zi})}, C=\frac{1}{A_v\cdot Z_s\cdot(1+\alpha_{zi})}$
$Z_{in}=\alpha_{zi}\cdot Z_s$, $Z_{out}=\infty$, A_i or Y_t $(=A_i/Z_s)$	$\frac{B}{D}=\alpha_{zi}\cdot Z_s$	A=0, C=0	$B=\frac{\alpha_{zi}\cdot Z_s}{A_i\cdot(1+\alpha_{zi})}, D=\frac{1}{A_i\cdot(1+\alpha_{zi})}$
$Z_{in}=\infty$, $Z_{out}=\alpha_{zo}\cdot Z_l$, A_v or Y_t $(=A_v/Z_l)$	C=0, D=0	$\frac{B}{A}=\alpha_{zo}\cdot Z_l$	$A=\frac{1}{A_v\cdot(1+\alpha_{zo})}, B=\frac{\alpha_{zo}\cdot Z_l}{A_v\cdot(1+\alpha_{zo})}$
$Z_{in}=0$, $Z_{out}=\alpha_{zo}\cdot Z_l$, A_i or Z_t $(=A_i Z_l)$	A=0, B=0	$\frac{D}{C}=\alpha_{zo}\cdot Z_l$	$C=\frac{1}{A_i\cdot Z_l\cdot(1+\alpha_{zo})}, D=\frac{\alpha_{zo}}{A_i\cdot(1+\alpha_{zo})}$
$Z_{in}=\alpha_{zi}\cdot Z_s$, $Z_{out}=\alpha_{zo}\cdot Z_l$, A_v, Y_t $(=A_v/Z_l)$, Z_t $(=A_v Z_s)$ or A_i $(=A_v\cdot Z_s/Z_l)$	$\frac{A}{C}=\frac{B}{D}=\alpha_{zi}\cdot Z_s$	$\frac{D}{C}=\frac{B}{A}=\alpha_{zo}\cdot Z_l$	$A=\frac{\alpha_{zi}}{A_v\cdot(1+\alpha_{zi}+\alpha_{zo}+\alpha_{zi}\cdot\alpha_{zo})}$ $B=A\cdot Z_l\cdot\alpha_{zo}, \quad C=\frac{A}{\alpha_{zi}\cdot Z_s}$ $D=A\cdot\frac{\alpha_{zo}}{\alpha_{zi}}\cdot\frac{Z_l}{Z_s}$

Table 2-2: Measures that can be taken to fix the input impedance, output impedance and transactance of a transactor in accordance with Table 2-1.

Apart from suitable port impedances, a transactor should have a designable transactance value. Equations 2.15-2.18 relate the transactance value to transmission parameters of the transactor and source and load impedances. For zero or infinite input and output port impedances, only one well-determined transactance exists, namely, the relation between the sensed source quantity and the "driving" load quantity (e.g. the transimpedance, if $Z_{in}=0$ and $Z_{out}=0$). If one of the port impedances has a well-determined value, voltage and current are directly related at that port. Thus the choice is immaterial, since they are accurately related by the port impedance. Consequently two transactances can be used as design objectives (e.g. for $Z_{in}=\alpha_{zi}\cdot Z_s$ and $Z_{out}=\infty$, the transadmittance and current gain can be used). By similar reasoning, all four transactances can be used if both port impedances are linear and accurate.

Based on the above considerations, the requirements for the 9 different transactors defined in Table 2-1 can be expressed in terms of transmission parameters. Table 2-2 shows which measures can be taken to give Z_{in}, Z_{out} and A_t the desired values, assuming that as many

parameters as possible are chosen equal to zero, and that Z_{in} and Z_{out} be fixed independently. Other solutions are possible, but need more transmission parameters to be fixed, which usually leads to more complex circuits. The first 4 cases in the table show that only one transmission parameter needs to have a well-determined non-zero value, if both port impedances should be either zero or infinite. In the following 4 cases one of the port impedances has a well-determined value, which is possible by fixing two transmission parameters. Finally if both the input and output impedance need to be accurate, 4 transmission parameters need be fixed.

2.5 Quality Criteria for Linear Transactors

In the previous sections, requirements on linear transactors were discussed mainly in terms of their functional behaviour (Which information should the transactor transfer and what should the transfer function be?). Now quality criteria for linear transactors will be addressed (How good should the transactor do “it”?).

In analog circuits a continuum of signal levels is used to represent information. Furthermore, the value of signals in analog continuous-time circuits is relevant all the time. This makes it possible to convey a lot of information in a short time using only one signal. Moreover, many operations on signals can be implemented in a very efficient way using very simple analog circuits. On the other hand, analog signals are prone to many kinds of disruptions, which complicates analog circuit design. Consequently an analog designer is not ready if he has a functional correct design, since he has to guarantee that practical disruptions do not decrease the circuit performance with more than an "allowed amount". In order to specify this "allowed amount", many quantitative quality criteria for circuits have been defined. These are often application specific, and can for instance be found in IC-datasheets. However, as this thesis aims at a generalised treatment of transactors, more general quality criteria are sought after.

The performance of linear transactors depends on the properties of the components that are used to implement them. Practical components show several imperfections that limit the achievable performance:

- *Inaccuracy:* component parameter values always have an inaccuracy due to IC fabrication tolerances, temperature variations and ageing, resulting in inaccurate transactance and port impedance values.
- *Nonlinearity:* the transfer characteristic of electronic components are non-linear. Especially active components suffer from significant nonlinearities. As a result the transactance and port impedances depend on the value of the input signal.
- *Noise:* noise fundamentally accompanies physical charge transfer processes. This noise puts a lower limit to the signal levels that can be processed by transactors.
- *Speed limitations*: charge transfer processes take time, and result in an upper bound for the signal frequencies that can be processed with sufficient accuracy by a transactor.
- *Power limitations*: components can deliver and withstand only a finite amount of power.

The five above mentioned limitations are fundamental limitation originating from device physics. Although their effect can often be reduced by careful design, it can never be avoided completely. Therefore, an attempt will be made to analyse the influence of these phenomena on transactor performance. Application specific quality criteria can often be related to the fundamental limitations.

2.6 Design Techniques for Linear Transactors

2.6.1 Introduction

In section 2.4.3 the design objective for useful linear transactors was established in terms of transmission parameters. Dependent on the type of desired transactor, one, two, or four transmission parameters should be given a well-determined value. This section discusses how this can be done by means of existing circuit design techniques, concentrating on continuous-time techniques and especially on negative feedback. In the next paragraphs the use of feedback is shortly reviewed, discussing the main concept and important design choices. The aim of the discussion is to identify essential underlying assumptions on which the quality of the resulting circuits is based. This is useful, since the approach adopted in this thesis is different in a number of aspects, as will be shown.

2.6.2 Principle of Negative Feedback

As discussed in the previous section, many threats for the achievement of high-performance transactors exist. A generally used technique to cope with a lot of these problems is the use of negative feedback. Figure 2-7 shows a widely used arrangement, implementing this method. In this block schematic representation, the symbol S is used for variables that can be either voltages or currents.

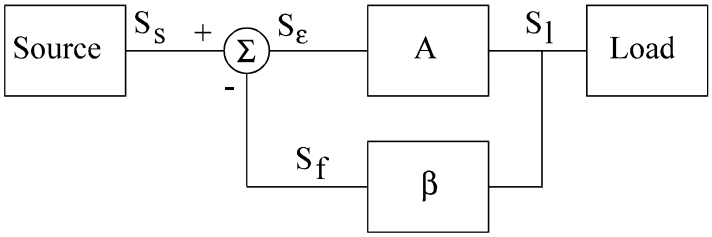


Figure 2-7: Principle of negative feedback

The feedback signal S_f is derived from the load signal S_l by means of an accurate linear "β-network". At the input this signal S_f is subtracted form the source signal S_s, resulting in a error signal S_ε. Amplifier "A" amplifies this signal, resulting in S_ε=0 for large values of the loop-gain Aβ. Hence, the feedback signal S_f becomes equal to the source signal S_s. Since S_f is directly related to S_l by means of block "β", the relation between S_l and S_s depends in the limit only on this network:

$$\frac{S_l}{S_s} = \lim_{A\cdot\beta\to\infty} \frac{A}{1+A\cdot\beta} = \frac{1}{\beta} \tag{2.21}$$

In an actual electronic circuit, the amplification A is implemented by active devices. In network theoretical terms these devices behave as a nullor [14] for large values of the loopgain (both the input voltage and input current are zero). By means of the feedback, the influence of parameter variations in the active device is reduced by the loop gain. The same holds for non-linearities and interfering signals that occur at the output of the amplifier A.

2.6.3 Choice of the β-Network

Since the β-network determines the transfer function, its choice is of crucial importance. Usually passive components are used for this purpose, since these are in general much less afflicted by inaccuracies, nonlinearities and noise than active components are. A careful classification of the available options, and the resulting consequences is presented by Nordholt in [21]. Although in Figure 2-7 only one β-network is shown, in fact up to four simultaneous feedback loops can exist, each defining a ratio between feedback signal V_f or I_f and the load signal V_l or I_l. Each of these feedback loops fixes the value of 1 transmission parameter. Thus with one feedback loop all transactors with either infinite or zero input and output impedance described in Table 2-2 can be realised. With two or four feedback loops also all two-ports with a linear input and/or output impedance are possible.

If the input current and input voltage of the active element are both zero, the active elements behaves like a nullor, and the input signal is equal to the feedback signal. In that case the feedback element(s) entirely determine the transfer function.

From a theoretical point of view, transformers and gyrators would be the components of choice for the β-network, because of their non-energeticness (they neither store nor dissipate power, but only transfer power; transformers fix voltage and current ratios, gyrators define a transadmittance and transimpedance relation). From a practical point of view the gyrator can only be realised using active devices, which introduce noise, nonlinearity and power dissipation. Furthermore, transformers are rather expensive components afflicted by many parasitic effects, and can only be tolerated in a very restricted class of applications. Consequently, in the majority of applications resistors, capacitors and occasionally inductors are used, in spite of their energeticness [24]. However, because these are one-ports, only an transimpedance amplifier can be implemented if a nullor with grounded input and output ports is used [21,19]. For voltage comparison at the input, a floating input port is required. The widely used OPAMP is such a nullor. For current sensing at the output, also a floating output port is needed. Based on an active device with floating ports six basically different transactors can be implemented: all four one-loop configurations (infinite or zero port impedances, the first four cases of Table 2-2) and two cases with accurate port impedances [21].

2.6.4 Limitations of Negative Feedback

Although the use of overall negative feedback in combination with passive components is a very powerful technique for the design of high performance linear transactors, it also has its limitations. In this section some of them will be discussed.

Functional Limitations

In the previous paragraph, it was mentioned that 6 transactors out of the 9 useful ones can be implemented using a nullor and passive resistors. Moreover, there are restrictions to the sign of the transactances that can be implemented [21](e.g. an inverting current-amplifier is not possible with one nullor and resistors). Thus either cascades of local feedback amplifiers have to be used (whereas overall feedback is to be preferred [21]) or alternative feedback networks, which will be discussed shortly.

Nullor Implementation Problems

The negative feedback design technique uses active devices to implement a nullor function. However, it is often hard to obtain a sufficiently good nullor approximation. Several amplification stages are usually cascaded to achieve sufficient gain. However, this easily leads to stability problems in case of overall feedback. This can be solved by suitable frequency compensation techniques, yet unfortunately at the cost of bandwidth. Furthermore, the gain decreases with frequency and thus do the beneficial effects of feedback. Thus, the high frequency potential of overall negative feedback is limited.

Another problem concerning the nullor approximation relates to the often required floating input and output ports. For perfect voltage comparison, the common-mode rejection of the active devices connected to the input port must be infinitely large (i.e. equal but opposite voltage sensitivities of the inputs). This is commonly achieved by using isolation and balancing circuit techniques [19]. However, especially the isolation technique only works well at low frequencies, since inevitable parasitic capacitive coupling effects dominates at higher frequencies. On the other hand, a floating output port is also hard to implement. For accurate current sensing the in- and out-going current of the output port should be exactly equal. Especially for class AB circuits this is hard to achieve [19,26]. Furthermore, again parasitic capacitive coupling hinders the realisation of a floating output at higher frequencies.

Passive Resistor Problems

Often, especially in older textbooks, it is assumed that active components can not provide the linearity and accuracy needed for linear signal processing. Thus it is considered necessary to resort to passive components, especially resistors. Indeed discrete resistors are usually very linear and can be very accurate (linearity is typically expressed in ppm/Volt, and an accuracy better than 1% is almost standard, while 0.01% is possible. Furthermore, the matching of discrete transistors is very poor and good thermal coupling can only be accomplished at considerable costs. In contrast, with careful layout, integrated MOS transistors can have a transconductance matching which is only slightly worse than achievable with integrated resistors. However, with respect to linearity, poly- and even diffusion-resistors are superior to MOSTs. On the other hand, high valued resistors, often required especially in low-current circuits, are a major problem. If they can be implemented at all, their properties are often rather poor: typical batch to batch spread in resistance may be more than 50%, mismatch 2-5%, and nonlinearity 2-5%/Volt [2]. Moreover, as was already discussed in chapter 1, a major disadvantage of passive resistors is their fixed resistance value. Thus they are not useful for self-correcting and

programmable systems, requiring electronically variable transactance values. Thus in some situations, MOS transistors are preferred above resistors. Fortunately, the MOS transistor has a rather weakly non-linear characteristic in strong inversion. Moreover, since even order distortion terms are the most important, significant linearity improvements can be achieved by means of balancing techniques.

Although striving for the best achievable information transfer is a noble aim, a sub-optimal transfer will do for a lot of applications and is likely to render a more economical solution. A problem with this type of "minimum requirement" design is how to guarantee proper operation of a circuit under all circumstances. Especially if the source and load conditions of an amplifier are not well known, or if production tolerances are not well characterised, over-designing may be a viable way to prevent a lot of trouble. There are, however, some reasons why this may be less of a problem in some cases. If a circuit is to be designed that is part of a fully integrated system, the source and load conditions of the amplifier circuit are usually well known. Furthermore, the components manufactured in IC-processes, that are also extensively used for analog circuits, are often intensively characterised, so that a lot of statistical information about component parameter variations is available. If simulation programs are available with component models that include statistical variations [158], correct operation of a circuit over process spread may be verified by simulations.

2.6.5 Alternatives for Direct Negative Feedback

In order to cope with the problems of negative feedback, other design techniques have been developed. Some of these will briefly be discussed, since they relate to some extend to the circuits to be discussed in this thesis.

Active and Indirect Feedback

In the previous paragraphs it appeared that not all desired transfer functions can be implemented based on passive elements, even if an amplifier with a floating input and output port are available. Furthermore, the use of current sensing at the output and voltage comparison at the input involves series connection of elements, which may be intolerable in low voltage applications [27]. The use of active feedback and indirect feedback can sometimes solve the above mentioned problems. Figure 2-8 shows an example of these two alternative feedback techniques, together with the "ordinary" so called direct feedback method. The example shows different implementations of a transconductance amplifier.

Figure 2-8a shows the direct feedback solution: the nullor forces the voltage across the resistor to be equal to V_s and conveys the resulting current V_s/R_f to the load impedance Z_l. In the direct feedback transconductor, the load current is bound to be negative for positive values of V_s. An output current with a positive sign can be obtained using the active feedback network shown in Figure 2-8b. In this case the upper nullor with feedback resistor R_f enforces implements a sign inversion. The disadvantages is that noise and distortion is added by the active devices in the feedback network.

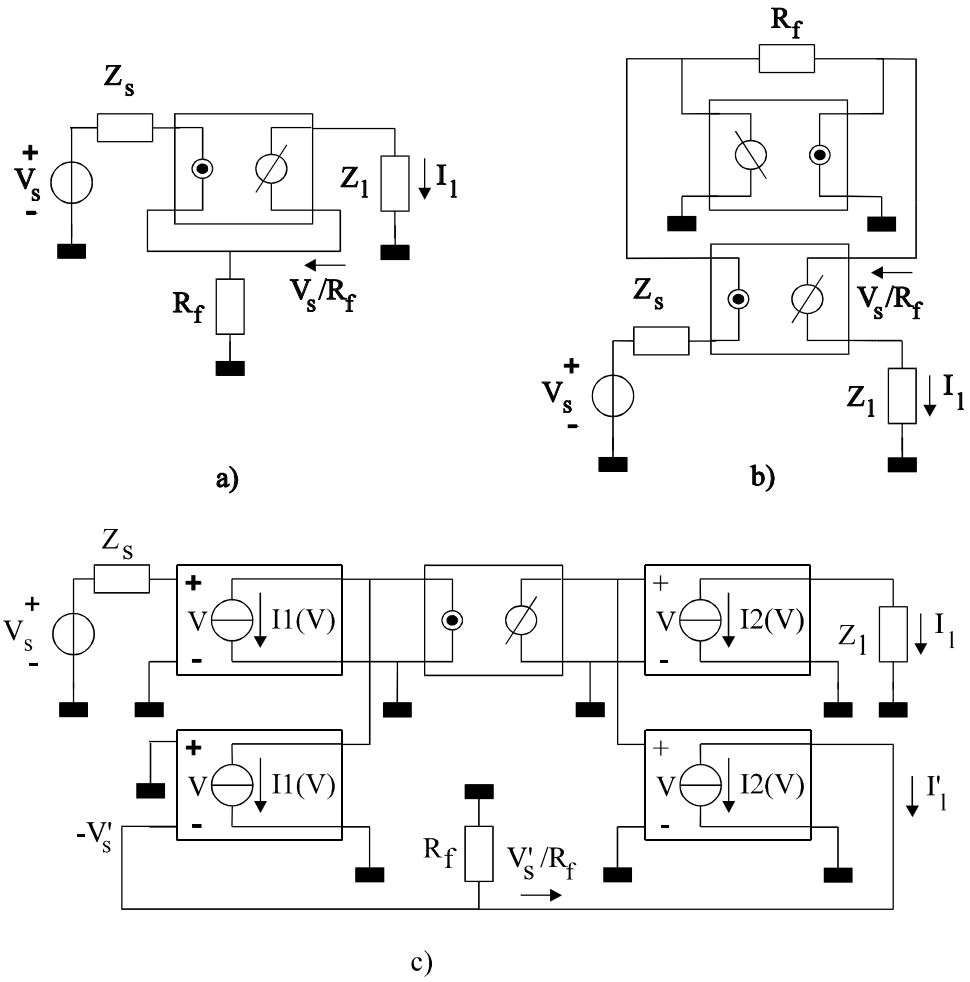


Figure 2-8: A transconductance amplifier implemented using direct feedback (a), active feedback (b) and indirect feedback (c: indirect current sensing at the output and indirect voltage comparison at the input, see text).

Even more design freedom exists is the indirect feedback transconductor of Figure 2-8c. In this example, V-I converters[1] are used for indirect load current sensing (the lower I2(V) V-I converter) and indirect voltage comparison (the I1(V) V-I converters). Again resistor R_f determines the transconductance. The current sensing is indirect, since it is not the actual load current that is sensed, but a copy of it, relying on matching of the I2(V) V-I converters. Similarly, it is not the actual input voltage that is compared to the feedback voltage $I_l' \cdot R_f$. Instead, these voltages are first converted to currents, and are then subtracted (note that the V- terminal of the lower I1(V) converter is connected to resistor R_f). The nullor forces this current-difference equal to zero, so that a voltage $-V_s$' results over resistor R_f.

The voltage comparison again relies on matching, which makes indirect feedback mainly useful for ICs. In principle the indirect feedback technique is inferior to direct feedback, since apart from R_f also (differences of) V-I converter transmission parameter influence the transactance. On the other hand it allows for the realisation of some transactors that cannot

[1] A more elaborate treatment of indirect feedback and the resulting transactor properties can be found in references [21] and [27].

be implemented by direct feedback. Furthermore, this technique uses parallel operating two-ports for current sensing and voltage comparison, instead of series connected ports. This has significant advantages if the voltage headroom is limited, as in low-voltage applications [27].

Compensation techniques

If the actual input-output relation of a network differs from the desired input-output relation, but in such a way that there is a unique relation between the input and the output quantities, there is no irretrievable loss of information. It is therefore possible to pass the signal through a second network which compensates for the error in the original input-output relation [27]. In a cascade connection of two-ports, for instance, an exact non-linearity compensation is acquired if the cascaded two-ports have inverse input-output relations. In other cases only a partial compensation is possible: in a balanced circuit, for instance, only the even order distortion terms cancel. Such compensations are only considered as reliable, if they rely on the same physical mechanism [21]. Because there is no feedback involved, compensation techniques do not have stability problems, and can potentially work up to high frequencies. On the other hand, the technique is sensitive to production tolerances, which limits the achievable performance.

Transconductance based Circuits

This thesis deals with the implementation of linear transactors using transconductors or VCCSs. However, some of the circuits found in this way can also be considered as circuits based on direct, indirect or active feedback. The main difference in approach lies in the choice of the basic generating elements used to implement a transactor. Often a nullor and passive components are used for this purpose. In this thesis, a VCCS will be used. However, both a nullor and a VCCS can sometimes be implemented using a single MOST.

2.7 Summary and Conclusions

In summary, requirements and design techniques for linear transactors were treated in this chapter. The need for analog linear signal processing was motivated, and the role of linear transactors as building blocks was discussed. The requirements that useful linear transactors should satisfy were established, followed by a short review of existing design techniques to implement them. The main conclusions that were drawn are summarised below.

Requirements for Linear Transactors

- For optimum information transfer, the port impedances of linear transactors should be adapted to the signal source and load. If the source or load impedance is inaccurate or non-linear, either a very large or very low transactor port impedance is desired. In case of a linear and accurate source or load impedance, a linear and accurate port impedance can be used, e.g. for characteristic impedance matching.
- Linear transactors should be able to implement all linear time-invariant transfer functions. Amongst others, this is possible with a VCCS and a capacitor.

- Some linear operations are preferably implemented using voltage signals, while currents are preferred for others. To be compatible with both, four types of transactors are desired: V-V, V-I, I-V and I-I.
- Self-correcting or programmable integrated systems require electronic tunability of the transactance of a transactor. If this is not necessary, an accurate value of the transactance is required.

Useful Transactors for Linear Signal Processing

- The port impedances of useful transactors are either very high, very low or accurate and linear.
- Starting from these three types of port impedances, 3x3=9 different useful transactors can be defined as shown in Table 2-1.
- The relevant transactances are voltage gain A_v, transadmittance Y_t, transimpedance Z_t, and current gain A_i.
- The transactance value should either be accurate or electronically variable.
- The 9 useful transactors can formally be defined as two-ports, described with transmission parameters. Table 2-2 shows how they can be implemented, with either 1, 2 or 4 non-zero transmission parameters.

Existing Design Techniques for Linear Transactors

- Although the use of overall negative feedback with passive feedback networks is a very powerful design technique, there are also limitations: not all desired types of transactors can be implemented, and a good nullor approximation is hard to achieve, especially if floating ports or high frequencies are involved. Furthermore, passive components lack electronic controllability and are usually only available with low resistance values.
- Alternative design techniques like active feedback and indirect feedback can implement some lacking useful transactors. However, they are in principle inferior to the commonly used “direct” feedback, since extra (active) device parameters influence the transfer function.
- Compensation techniques can improve the linearity of circuits, and can be useful up to very high frequencies. On the other hand, the achievable improvement is limited by production tolerances.

3

Generation of All Graphs of Transactors with Two VCCSs

3.1 Introduction

In the previous chapter the requirements for linear transactors have been established. The present chapter examines the possibilities to implement transactors based on the transconductance of MOS transistors. Section 3.2 introduces some basic models for the electrical behaviour of the MOST. It will be shown that a single MOST or combination of MOSTs can often be considered as a Voltage Controlled Current Source (VCCS). Depending on the operating regime three types of "generalised" I(V) characteristics are defined: a linear, square-law or exponential one. These will be used throughout the thesis. Then, section 3.3 deals with a method to find all different transactors with two VCCSs. The proposed method uses graphs to represent different topologies. All topologies with one VCCS are generated in section 3.4, followed by an analysis of their transfer functions. It will appear that only a subset of the 9 useful transactors defined in the previous chapter can be implemented in this way. Therefore topologies with two VCCSs are generated and analysed in section 3.5. Finally in section 3.6 the results are discussed to show that they satisfy the requirements derived in the previous chapter.

3.2 The MOST as a VCCS

In the following subsections it will be shown that a single MOS transistor or simple MOST circuits can often be considered as a VCCS.

3.2.1 MOST DC-Characteristics

The electrical device characteristics of a MOST play an important role in the design of MOST circuits. Figure 3-1a shows a long channel NMOST, biased by voltage sources V_{GS} and V_{DS}, and the resulting V-I characteristics in strong inversion [30]. At a given gate-

source voltage, the drain current $I_D(V_{DS})$ is more or less constant for drain-source voltages larger than the so-called saturation voltage (Figure 3-1b). Thus the MOST behaves as a current source in that region. Since the current depends on the gate-source voltage, it is a Voltage Controlled Current Source (VCCS). As shown in Figure 3-1c, for large drain-source voltages $I_D(V_{GS})$ is roughly a square-law relation above threshold voltage V_T. In the weak inversion operating region (gate-source voltages well below V_T, not shown in Figure 3-1), again a current source behaviour is found for large drain-source voltages. However, in that case an approximately exponential relation $I_D(V_{GS})$ is found.

The VCCS model is only a first order approximation. In practice, the current also depends on the drain-source voltage, especially in short channel devices. However, if this is a problem, it can often be solved, e.g. by increasing the channel length or by using cascoding circuit techniques.

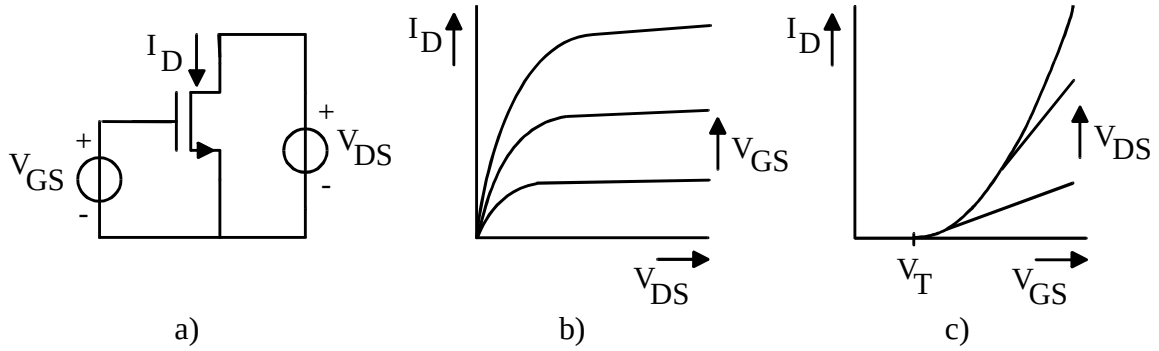


Figure 3-1: An NMOST and its I(V) characteristics in strong inversion.

Many models for the electrical behaviour of the MOS transistor in its various operating regions exist [32]. In choosing an appropriate model for circuit synthesis or analysis, in general a trade-off between accuracy on the one hand and complexity on the other hand must be made. Especially if nonlinearities are to be taken into account, the use of a simple model is often mandatory to enable finding a solution. Furthermore, as discussed in chapter 1, this thesis aims at a generalised treatment of VCCS circuits, concentrating on the principal functional properties. This requires a modelling approach that grasps the main features of a circuit. If we take into account all details, every circuit is different, and a generalisation becomes impossible. Therefore, simple first order model equations will be used. Only if this leads to useless results, for instance zero distortion, second order effects will be modelled. Especially mobility reduction will be taken into account. This is because it is known from literature as the principal cause of nonlinearity in linearised transconductors [e.g. 50, 54, 111], while no practical techniques are known to compensate the effect. In contrast, the body effect and channel length reduction can often be minimised by suitable circuit design techniques. Therefore, for first-cut design these effects are ignored in this thesis. This leads to performance predictions that can be considered as best achievable performance estimations. Despite of their inaccuracy, these estimations can be useful orientation points in the complex design landscape.

NMOST Model

The first order model that will be used for the current of an NMOST operating in strong inversion and in the triode region, respectively saturation region is:

$$I_{DSN} = \frac{W}{L}\mu_N C_{ox}\left(V_{GSN} - V_{TN} - \tfrac{1}{2}V_{DSN}\right)V_{DSN} \quad (V_{GSN} > V_{TN}\,;\, V_{DSN} \le V_{GSN} - V_{TN}) \qquad (3.1)$$

$$I_{DSN} = \frac{W}{2L}\mu_N C_{ox}\left(V_{GSN} - V_{TN}\right)^2 \qquad (V_{GSN} > V_{TN}\,;\, V_{DSN} \ge V_{GSN} - V_{TN}) \qquad (3.2)$$

In these expressions, I_{DSN} is the current that flows from drain to source, V_{TN} is the threshold voltage of the MOST, W and L are the channel width and length of the MOST, C_{ox} is the oxide capacitance per unit area, and μ_N is the mobility of the electrons in the channel. If necessary, the mobility reduction effect will be taken into account, by substituting the following expression for μ_N [30]:

$$\mu_N = \frac{\mu_{0N}}{1 + \theta_N\left(V_{GSN} - V_{TN}\right)} \qquad (3.3)$$

where μ_{0N} is the mobility for zero vertical field and θ_N is a model parameter that models the dependence of the mobility on the gate-source voltage. The value of θ is roughly inversely proportional to the gate-oxide thickness [31], leading to higher values for newer submicron CMOS processes. Short channel MOSTs also suffer from mobility reduction due to high lateral fields (velocity saturation). In saturation, this can be taken into account without changing eqn. 3.3, by increasing θ_N [31].

For the weak inversion operating region, the following first order model will be used [28,32,24] (assumption $V_{SBN}=0$, $V_{GSN} >> n_N U_T$):

$$I_{DSN} = \frac{W}{L} I_{DN0} \cdot e^{V_{GSN}/n_N U_T} \qquad \left(I_{DSN} << \frac{W}{L}\mu_{0N} C_{ox} U_T^2\,;\, V_{DSN} > \kappa_N\, U_T\right) \qquad (3.4)$$

In this relations, I_{DN0} is an IC-process dependent parameter, U_T is the thermal voltage $k \cdot T/q$, n_N is the subthreshold slope parameter (typically about 1.6), and κ_N is a (rather arbitrary) parameter indicating the onset of current saturation (typically 2.5).

In the above equations, a strong and weak inversion model are given. In fact, a transition region of several tenths of a Volt exists in between, denoted as moderate inversion [32]. In terms of current, weak inversion occurs for currents much smaller than $W/L\,\mu_{0N} C_{ox} U_T^2$, and strong inversion for currents that are significantly larger than that value. Since there is no tractable model expression for the moderate inversion operating region lacks, it will not be modelled separately.

PMOST Model

Obviously, a PMOST can also be used instead of an NMOST. Usually, the model equations for a PMOST are derived from eqn. 3.1 up to eqn. 3.4 by sign-changes. However, the use of different equations for the NMOST and PMOST would complicate the analysis of circuits in the rest of this thesis. Therefore, a less usual way of writing the PMOST equations is adopted in which the threshold voltage of an enhancement PMOST is

defined as positive. To avoid confusion, the threshold voltage will be designated V_{-TP}. The following relations are used for a PMOST:

$$V_{-TP} > 0 \tag{3.5}$$

$$I_{SDP} = \frac{W}{L}\mu_P C_{ox}\left(V_{SGP} - V_{-TP} - \tfrac{1}{2}V_{SDP}\right)V_{SDP} \quad (V_{SGP} > V_{-TP}; V_{SDP} \le V_{SGP} - V_{-TP}) \tag{3.6}$$

$$I_{SDP} = \frac{W}{2L}\mu_N C_{ox}\left(V_{SGP} - V_{-TP}\right)^2 \qquad (V_{SGP} > V_{-TP}; V_{SDP} \ge V_{SGP} - V_{-TP}) \tag{3.7}$$

$$I_{SDP} = \frac{W}{L} I_{DP0} e^{V_{SGP}/n_P U_T} \qquad (I_{SDP} << \frac{W}{L}\mu_{0P} C_{ox} U_T^2; V_{SDP} > \kappa_P U_T) \tag{3.8}$$

These equations have the same basic form as eqn. 3.1 up to eqn. 3.4. This is achieved by exchanging the terminal indices compared to those of an NMOST. As for the NMOST, the mobility reduction effect will, if necessary, be modelled as:

$$\mu_P = \frac{\mu_{0P}}{1 + \theta_P\left(V_{SGP} - V_{-TP}\right)} \tag{3.9}$$

Sometimes it will be useful to substitute numerical values in expressions, to get an impression of the performance that can be achieved in practice. Such calculations will be based on typical values for some MOST parameters of an industrial 1μCMOS process, shown in Table 3-1.

Parameter	Typical Value	Dimension
$\mu_{0N}C_{ox}, \mu_{0P}C_{ox}$	100, 40	$\mu A/V^2$
V_{TN}, V_{-TP}	0.8	V
θ_N, θ_P (long channel)	0.1	V^{-1}
n_N, n_P	1.6	-
I_{DN0}, I_{DP0}	1.5, 0.5	fA

Table 3-1: Typical values for some MOST parameters (1μCMOS process).

3.2.2 A VCCS with a Floating Input and Output Port

According to eqn. 3.2 and eqn. 3.4, an NMOST operating at sufficiently high drain-source voltage shows saturation of the current and thus acts as a (gate-source) Voltage Controlled (drain) Current Source. By adding a cascode circuit, a triode NMOST (eqn. 3.1) can also be used as a VCCS (see also section 3.2.3). Similarly, eqns. 3.6-3.8 for the PMOST can be exploited.

The symbol used for an NMOST and its equivalent VCCS representation is shown in Figure 3-2a, where $V=V_{GSN}$ and $I(V)=I_{DSN}(V_{GSN})$. The bulk of the MOST is not shown, since the body effect is neglected, as discussed in section 3.2.1. It is important to note that the VCCS in Figure 3-2a has a connection between the V- voltage-sense terminal and the current terminal, at which the current flows out of the device. As the input and output port of the VCCS have a terminal in common, it is a so-called *common-terminal two-port* or *common-terminal VCCS*. Similarly, the PMOST represented in Figure 3-2b can be

modelled as a common-terminal VCCS with its V+ voltage-sense terminal connected to the current-source terminal, at which the current enters the VCCS.

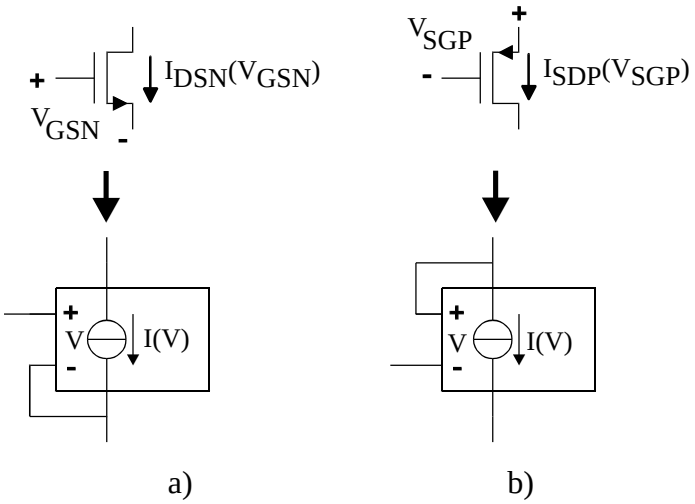


Figure 3-2: An NMOST and PMOST modelled as a VCCS with a common- and common+ terminal respectively. Relation I(V) corresponds to $I_{DSN}(V_{GSN})$ and $I_{SDP}(V_{SGP})$ respectively (see eqn. 3.1-3.8). For triode region operation, additional circuitry is needed to establish VCCS behaviour (see also section 3.2.3).

The presence of a common-terminal limits the usefulness of the device. This is because one of the voltage-sense terminals looses its high-ohmic nature because of this connection. Fortunately, a VCCS with floating ports can be constructed by series or anti-series connection of two common-terminal VCCSs. The two common-terminal VCCSs are joined at their common-terminal. The different possibilities to join common-terminals are shown in Figure 3-3. If necessary a biasing current can be supplied to the common-terminal node. The resulting circuits are well-known from literature as, respectively, a complementary, PMOST and NMOST differential pair.

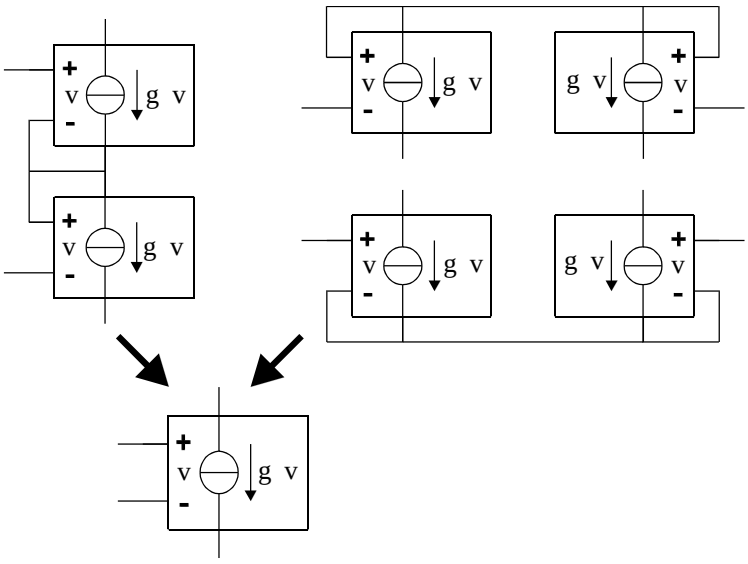


Figure 3-3: A VCCS with a floating input and output port can be implemented by a series connection of a common- and common+ VCCS, or a anti-series connection of two identical common+ or common- VCCSs.

Since a VCCS with a floating input and output port is a more flexible device, it will be used as a generating element in this thesis. If, in the topologies to be generated, connections exist between a voltage-terminal and a current-terminal, a single MOST can do the job, resulting in a simpler circuit on transistor level.

3.2.3 Generalised I(V) Models: LVCCS, SVCCS, EVCCS

In the previously discussed square-law (eqn. 3.2 and 3.7) and exponential equations (eqn. 3.4 and 3.8), the drain-current does not depend on the drain-source voltage, and satisfies the requirement for a VCCS. In contrast, a MOST in the triode region (eqn. 3.1) has a drain-current which strongly depends on its drain-source voltage. However, by means of a cascode device, and a feedback loop as shown in Figure 3-4a, a current output can be implemented[1], while the drain-source voltage is kept constant at V_{tune} [41]. According to eqn. 3.1, a VCCS with a linear V-I transfer characteristic results. The transconductance of this VCCS is linearly tuneable over a large range by means of V_{tune}. Alternatively, it is also possible to use the drain-source conductance of a MOST as a V-I conversion element. For small values of V_{DS} a linear $I_D(V_{DS})$ is found. Figure 3-4b illustrates this possibility: the opamp and the cascode MOST buffers the input voltage to the encircled triode MOST and convey the resulting drain-current to the output. Alternatively wide cascode MOS transistor can be used [43, 45]. The gate voltage V_{tune} of the triode NMOST determines the value of the channel conductance and thus the transconductance of the VCCS.

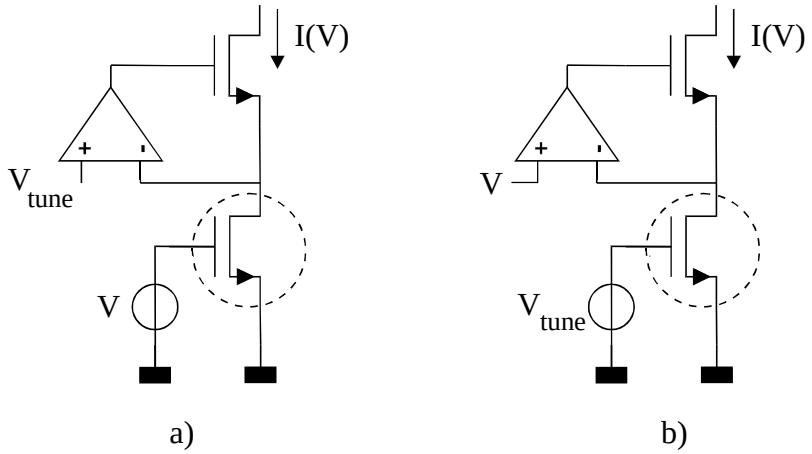


Figure 3-4: VCCS implementation based on a triode NMOST (encircled) used as a tunable transconductance (a) and as a tunable conductance (b).

According to its title, this thesis deals with transconductance based MOST circuits. Nevertheless, it is worthwhile to investigate whether the results of this thesis can also be applied to other VCCS realisations, e.g. based on the conductance of MOSTs or resistors, or on the transconductance of bipolar transistors. Aiming at a general scope, three *generalised VCCS* transfer characteristics will be defined, that cover many VCCS implementations.

---

[1] A MOST operating in the "non-saturated" weak inversion region can also be used. This option is neglected, as it results in an exponential I(V) curve as for high drain-source voltages, yet with more complex circuitry.

These *generalised VCCSs* are (see also Figure 3-5):

1. The *Linear VCCS (LVCCS)*. Well-known MOST-implementations include circuits exploiting the transconductance of a triode MOST (Figure 3-4a), but also its drain-source conductance (Figure 3-4b) or a passive resistor.
2. The *Square-law VCCS (SVCCS)*, to cover the MOST in strong inversion and saturation.
3. The *Exponential VCCS (EVCCS)*, to cover a VCCS exploiting a weak inversion MOST, but also a bipolar transistor.

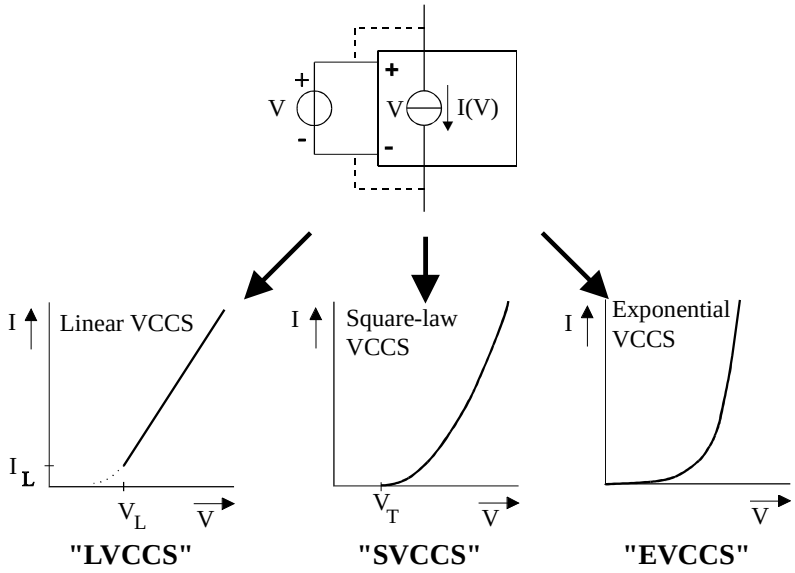


Figure 3-5: The three VCCSs with generalised I(V) characteristics: LVCCS (Linear), SVCCS (Square-law) and EVCCS (Exponential).

As there are different possible implementations, a notation without MOST specific terms is appropriate. Furthermore, equations will be written in their simplest possible form, since they have to be used frequently. The equations are shown in Table 3-2, and will be discussed briefly.

VCCS type	I(V) Equation	Boundary Conditions	Equation Reference
LVCCS	$I = G \cdot (V - V_L) + I_L$	$V_{min,L} < V < V_{max,L}$	(3.10)
SVCCS	$I = k \cdot (V - V_T)^2$	$V_{min,S} < V < V_{max,S}$	(3.11)
EVCCS	$I = I_E \cdot e^{V/V_E}$	$V_{min,E} < V < V_{max,E}$	(3.12)

Table 3-2: Equations for the three generalised VCCSs

The VCCS model equations are presumed to be valid over a voltage range $V_{min} < V < V_{max}$ (column "Boundary Conditions" in Table 3-2). These boundary conditions are somewhat arbitrary as they depend on the required model accuracy. Some of these conditions directly result from device physics, and will be specified. Other restrictions are of more practical nature and depend on a specific circuit implentation or application. The maximum value of V can for instance be determined by the available supply voltage. Also, an output circuit of

a VCCS might pose voltage restrictions, e.g. because a cascode device needs voltage headroom. Such consideration can play an important role during circuit design. However, a generally valid boundary condition can not be specified. Instead, this aspect needs to be considered at transistor implementation level.

In the circuits to be generated, the "self-connected" topology of a VCCS is often encountered (one of the VCCS current output terminals is connected to one of its voltage terminals). Hence, it is of practical importance that the VCCS V-I relation is at least valid under this condition, and allows for some voltage swing.

LVCCS

For the LVCCS case, a transconductance G models the linear increase of I with V. This transconductance is presumed to be constant over a large biasing range. The parameters V_L and I_L allow for an offset in voltage and current. Table 3-3 gives the LVCCS model parameters for 4 often used implementations of a LVCCS:

1. A gate-source-voltage driven triode NMOST with constant V_{DS} (Figure 3-4a)
2. A drain-source voltage driven triode NMOST (Figure 3-4b)
3. A saturated NMOST with degeneration resistor (for large W/L, so that the resistor mainly determines the I(V) characteristic).
4. An NMOST differential pair with tail current source.

The corresponding relations for the PMOST can easily be found by comparison of eqn. 3.1-3.2 and eqn. 3.6-3.7.

LVCCS implementation	**G**	**V_L**	**I_L**	**Boundary conditions for V**
Triode NMOST, transconductance	$\frac{W}{L}\mu_N C_{ox} V_{DSN}$	$V_{TN} + V_{DSN}$	$\frac{W}{2L}\mu_N C_{ox} V_{DSN}^2$	$V_{TN} + V_{DSN} < V$
Triode NMOST, conductance	$\frac{W}{L}\mu_N C_{ox}\left(V_{GSN} - V_{TN}\right)$	0	0	$0 < V < V_{GSN} - V_{TN}$ $V_{DSN} << 2\left(V_{GSN} - V_{TN}\right)$
Resistively degenerated NMOST (large W/L)	$1/R$	V_{TN}	0	$V_{TN} < V$
NMOST differential pair with tail current	$\frac{1}{2}\sqrt{\frac{W}{L}\mu_N C_{ox} I_{tail}}$	0	0	$\lvert V\rvert < \sqrt{\frac{2I_{tail}L}{W\mu_N C_{ox}}}$

Table 3-3: Parameters for different LVCCS implementations.

SVCCS

The SVCCS relation is given in eqn. 3.11 in Table 3-2, and is a simplified form of eqn. 3.2 or 3.7. A commonly used implementation is a MOST operating in strong inversion and saturation. The equations for the SVCCS parameters are given in Table 3-4. Apart from these common-terminal VCCSs, a SVCCS with a floating input and output port is also possible using a common-source CMOS pair [50]. Figure 3-6 shows the three implementation options.

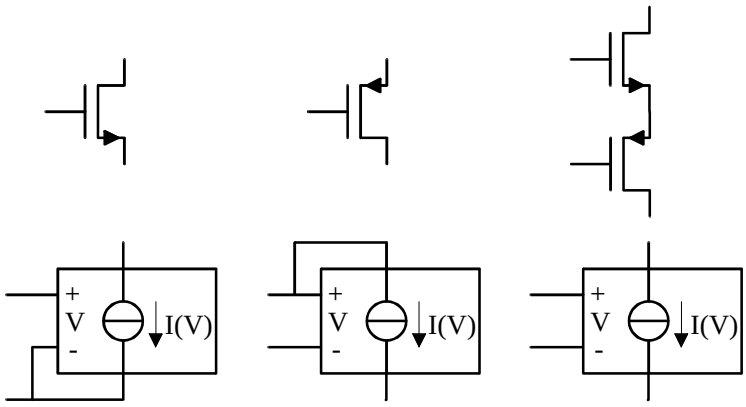


Figure 3-6: Three SVCCS realisations: an NMOST, a PMOST and a CMOS pair [50].

The lower limit of validity of the SVCCS equation is taken to be $V=V_T$. Apart from this lower limit, there will in general also be a maximum to the VCCS voltage. For a saturated NMOST in strong inversion, this limit is determined by the gate-source voltage $V_{DSN}+V_{TN}$, at which the NMOST enters the triode region. This limit depends on circuit details.

SVCCS implementation	**k**	**V_T**	**Boundary conditions for V**
Strong Inversion, saturated NMOST	$\frac{W}{2L}\mu_N C_{ox}$ (=k_N)	V_{TN}	$V_{TN} < V < V_{DSN} + V_{TN}$
Strong Inversion, saturated PMOST	$\frac{W}{2L}\mu_N C_{ox}$ (=k_P)	V_{-TP}	$V_{-TP} < V < V_{SDP} + V_{-TP}$
Complementary CMOS pair [50] (common source)	$\frac{k_p \cdot k_N}{k_P + k_N}$	$V_{TN}+V_{-TP}$	$V_{TN} + V_{-TP} < V$ $V_{SGP} < V_{SDP} + V_{-TP}$ $V_{GSN} < V_{DSN} + V_{TN}$

Table 3-4: Parameter equations for three well-known SVCCS implementations: an NMOST, a PMOST and a complementary CMOS pair [50] (see also Figure 3-6).

EVCCS

The I(V) relation for an EVCCS is given by eqn. 3.12 in Table 3-2. The values of V_E and I_E for a weak inversion MOST and a bipolar transistor are given in Table 3-5. In practice, leakage current considerations often determine a lower limit to the useful operating range. The upper boundary condition for the validity of the weak inversion mode is usually taken equal to V_T-150mV (half of the range of the moderate inversion region). For practical MOS transistors, typically 3 decades of exponential current can be used.

EVCCS implementation	**V_E**	**I_E**	**Boundary Conditions**
Weak Inversion, "saturated" NMOST	$n_N \cdot U_T$	$\frac{W}{L} \cdot I_{DN0}$	$V >> V_E \cdot \ln(I_{leakage} / I_E)$ $V < V_{TN}$ - 150mV
Bipolar transistor	U_T	I_S	$V >> V_E \cdot \ln(I_{leakage} / I_E)$

Table 3-5: EVCCS parameters for a weak inversion MOST and Bipolar transistor.

3.2.4 Transconductance of VCCSs

In this thesis, the small signal transconductance g of the VCCS plays a crucial role, since it determines the transmission parameters of transactors. The small signal equivalent model that will be used is a VCCS with current g·v as shown in Figure 3-7.

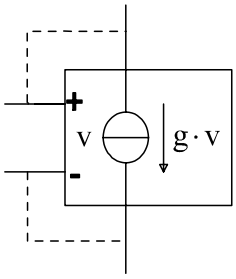


Figure 3-7: The linearised small-signal equivalent circuit for a VCCS.

By differentiation of eqn. 3.10-3.12 in Table 3-2, the values for g for the three Generalised VCCSs are easily found. The results are shown in Table 3-6. The column with $g(V_0)$ expresses the transconductance as a function of the VCCS quiescence voltage V_0, while $g(I_0)$ expresses it as a function of quiescence bias current I_0. For both cases, the dependence of g on W/L for a MOST implementation of the VCCS is also shown.

VCCS type	$g(V_0)$	$g(V_0)$ (MOST)	$g(I_0)$	$g(I_0)$ (MOST)
LVCCS	G	$\propto$ W/L	G	$\propto$ W/L
SVCCS	$2 \cdot k \cdot (V_0 - V_T)$	$\propto$ W/L	$2 \cdot \sqrt{k \cdot I_0}$	$\propto \sqrt{W/L}$
EVCCS	$\frac{I_E}{V_E} \cdot e^{V_0/V_E}$	$\propto$ W/L	I_0 / V_E	-

Table 3-6: Transconductance equations for the Generalised VCCSs and a MOST implementation ($\propto$ means proportional with; - means independent).

From Table 3-6 we can draw some interesting conclusions with respect to differences between the three VCCS types:

- The transconductance of the LVCCS is equal to G, independent of the value of V_0 and I_0. If it is tuneable, the tuning is achieved by means of another electrical variable than V or I (e.g. the drain-source voltage of a triode MOST). The value of G is linearly proportional to W/L.
- For the SVCCS, the transconductance is proportional to V_0 and to the square-root of I_0. For voltage biasing, it proportional to W/L. For current biasing, it is proportional to the square-root of W/L.
- For the EVCCS, the transconductance only depends on V_E and on the current, if the EVCCS is biased by a current. In that case it is independent of device geometry. If the device is biased by a voltage, the transconductance is very sensitive to V_0 via an exponential relation, and proportional to W/L.

Practical Values

In order to get a feeling for practical values, some numerical calculations have been made. As this was done for voltage biasing, the results can easily be compared, since all transconductance values are proportional to W/L. The results were obtained using the parameters of Table 3-1, and are shown in Table 3-7 along with the assumptions made.

VCCS implementation	g-value (μS)	Assumptions
LVCCS (g_m of a triode NMOST)	0.6-60 $\cdot W/L$	V_{DSN}= 0.01...1V V_{GS} = 3V
LVCCS (g_{ds} of a triode NMOST	10-150 $\cdot W/L$	V_{GSN}-V_{TN} = 0.1...2 Volt V_{DS}=0 Volt
LVCCS (Poly resistor)	10000 $\cdot (W/L)_{RESISTOR}$	Ideal voltage buffer
LVCCS (Nwell resistor)	1000 $\cdot (W/L)_{RESISTOR}$	Ideal voltage buffer
SVCCS (NMOST)	10-140 $\cdot W/L$	V_{GSN}-V_{TN}= 0.1...2 V
EVCCS (NMOST)	0.00015-0.15 $\cdot W/L$	$\frac{W}{L}\mu_{0N}C_{ox}U_T^2 / I_{DSN}$ = 10000..10

Table 3-7: Typical values for the transconductance of different VCCS implementations for NMOSTs based on the parameters in Table 3-1.

For an LVCCS, the value of G depends on the implementation, but is always proportional to W/L. For a triode MOST the transconductance is proportional to V_{DS}, while the conductance is proportional to V_{GT}=V_{GS}-V_T. Typical values for V_{DS} are in the range of 0.01-1Volt, and 0.1-2Volt for V_{GT} (for smaller values of V_{GT}, the MOST enters the moderate inversion region). Since the ratio between the maximum and the minimum value of V_{DS} is larger than for V_{GT}, the transconductance control range is larger for the triode transconductance case. The achievable maximum G is in the same order of magnitude, about 100μS times W/L. If a LVCCS is realised with a resistor, it is proportional to W/L of the resistor, assuming that a buffer circuit transfers the entire input voltage across the conversion resistor. Since typical values for the conductance per square are about 10mS for poly resistors and 1mS for nwell-resistors, large conductance values are easily implemented, but small values are hard to obtain. However, the conductance of these resistors is not electronically variable.

For the SVCCS, implemented with a strong inversion saturated NMOST, the transconductance takes values between 5 and 100μS, for V_{GT}=0.1...2V.

For the EVCCS, implemented with a weak inversion saturated MOST, much lower values can be obtained. Usually, I_{DSN} can at least vary over 3 decades, without running into leakage current problems. This corresponds to a V_{GS}-range of about 280mV, some tenths of a volt below V_T, and results in a transconductance value between 0.00015 to 0.15μS times W/L (assuming that the current is at least 10 times smaller than $W\mu_{0N}C_{ox}U_T^2 / L$).

Summarising, we can conclude that the conductance of all types of VCCSs is proportional to W/L, assuming voltage biasing. Typical conductance values for MOSTs operating in strong inversion are in the range of 1-100μS times W/L. For passive resistors, typical values are 10 to 100 times larger. For weak inversion, 10 to 10000 times smaller values can be obtained. The tuneability of the transconductance is maximal for the EVCCS: g_E is typically tuneable over at least 3 decades. A LVCCS based on a triode MOST has the second best tuning range: it is typically tuneable over 2 decades. Finally, the SVCCS is roughly tuneable over one decade, while tuning is not possible with transconductors based on passive resistors.

3.3 Generation and Evaluation of Transactor Graphs

The aim of this chapter is to examine whether the 9 useful transactors defined in the previous chapter can be implemented using MOST VCCSs. The question is now: how can we find out which transactors can be implemented? A possibility is*: generate all possible circuit topologies* with a certain number of VCCSs and *analyse* their *transfer functions*. The "certain number" has to be chosen. One VCCS fixes a relation between a voltage and a current. As discussed in the previous chapter, voltage and current ratios are also useful, so that at least two VCCSs are needed. Since there is no clear justification for more than two VCCSs, topologies will be generated for that case.

3.3.1 Topological considerations

The main question is now: which topologies are possible with two VCCSs? A well-known way of representing the topology of a circuit is by means of a directed linear graph [148, 149, 152]. As a matter of fact, Kirchhoff founded the theory of graphs specifically for its application to electrical networks and used it to generalise his voltage and current law. Our problem can now be restated as: how many different directed graphs with two VCCSs connected to a source and load exist? In these graphs 3 types of so called *generating elements* are to be represented: an independent source, VCCS and load impedance. Figure 3-8 shows the graph representations that will be used. The labels *s* (source), *v* (control voltage), *i* (controlled current) and *l* (load) are used to identify the branch to generating element correspondence.

Before starting a job, it is useful to estimate the amount of work to be done. In this case the number of possible topologies is a relevant quantity. The number of nodes and branches plays an important role in the enumeration of the number of different graphs [154]. Assuming the use of one independent source, one load and two VCCSs, we have:

- 1 branch with 2 nodes for the source
- 1 branch with 2 nodes for the load
- 2 x (2 branches with 4 nodes) for the two VCCSs.

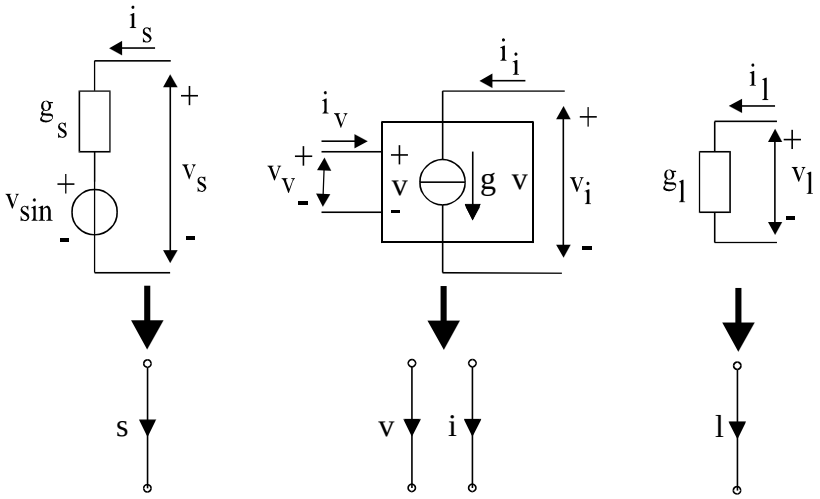


Figure 3-8: The generation elements and their graph representations: an independent source (s-branch), a VCCS (v- and i-branch) and a load impedance (l-branch).

This sums up to 6 branches with 12 nodes. However, it only makes sense to assume that all branches are connected in loops. If this is not true for a certain branch, then its current is zero (KCL), while the branch voltage does not occur in any KVL equation (it is not present in any voltage loop). Hence, the element corresponding to the branch does not "contribute" to the operation of the transactor, and will be designated as non-functional. More precisely, we are in search of two-ports with at least one non-zero transmission parameter (conclusions chapter 2) and will define non-functionality as follows:

Non-functionality

If omission of a VCCS from a two-port circuit does not affect any of its transmission parameters, the VCCS is designated as non-functional. A two-port circuit is designated as non-functional, if it contains one or more non-functional VCCSs or if one or more of its transmission parameters do not exist (no or zero solution for the network equations).

Graphs corresponding to non-functional circuits will also be designated as non-functional, and will not be examined further. This rejection based on non-functionality results in the following conclusions:

1. *All VCCS-branches must be connected in loops.* The transmission parameters are derived from source and load variables (section 3.3.3). A VCCS can only affect these variables by means of KVL and/or KCL relations involving variables of the VCCS *and other elements in the network*. If a VCCS-branch is not connected in any loop, its current is zero, while the VCCS-branch voltage does not occur in any KVL-loop. Hence, the VCCS has no effect on any of the variables of other elements, nor has removal of the VCCS, i.e. it is non-functional.

2. *No self-loops are allowed*. A self-loop corresponds to a short-cut across a branch. For the source and load, this results in nonexisting transmission parameters, hence non-functionality. For a VCCS, a self-loop gives a net current contribution of zero to KCL equations (either because v=0 or since the current enters and leaves the same node). Hence the VCCS can be omitted without any effect, and is non-functional.

With every node at least connected to 2 branches (required to establish loops), a maximum of 6 nodes for 6 branches can exist. To estimate the number of possible graphs some numbers were gathered from tables given in [154], rendering data on the number of graphs with certain given properties. Unfortunately no numbers were found for the present case of interest, with at least 2 connections for every node. However, an estimate can be based on the number of trees for a given number of nodes.

A tree is a maximally connected subgraph without loops. Trees play an important role in network analysis methods for circuits [148, 149, 152]. By adding a so called link to a tree, a fundamental loop is formed, for which Kirchhoff's voltage law holds (the number of independent Kirchhoff voltage equations is equal to the number of fundamental loops [148]). As we are in search of graphs with all branches connected in loops, trees are a good starting point (any graph with all branches connected in loops can be decomposed in a tree and links). From trees, we can find the graphs that we search for by adding additional branches until all 6 are used, requiring that all branches are connected in loops. If we start with *all trees* with 6 nodes or less, and *systematically* check all possibilities to *add links*, *all relevant graphs* are found.

For the case of 6 branches and up to 6 nodes, 20 different undirected unlabelled graphs are found starting from tree graphs. For every branch in these graphs, any of the six branches of the generating elements can be used. Hence, 720 permutations exist (6!), resulting in 14.400 graphs. Although this is a large number, it is much lower than found for other graphs with 6 branches on which less restrictions are imposed. Looking at it optimistically, this indicates that adding a restriction can drastically reduce the number of possibilities. By looking at a number of simple examples, we will try to find additional restrictions to be posed on transactor graphs. Since the case of one VCCS and a source and load (4 nodes and 4 branches) appears manageable, this case will be examined first.

3.3.2 All Graphs with one VCCS

In case of one VCCS and a source and load, four branches with 8 nodes exist. However, some of the interconnection possibilities can be excluded on forehand. The following considerations help to reduce the number of possibilities:

- With all 4 branches connected in loops, at most 4 different nodes are possible. The number of nodes can be less than 4, if parallel branches exist. However, the number of nodes should be larger than 1, to avoid self-loops. Thus relevant graphs have at least 2 and at most 4 nodes, and always four branches and no "self-loops".
- A graph may consist of two pieces (two loops with each two parallel branches). Since elements are required to be connected in loops, more subgraphs are not possible.
- A non-directed graph can be used to represent the circuit topology, in order to limit the number of possibilities. The sign information contained in the directedness of the graph can also be added in a different way. For linear circuits, reversing the direction of the input source leads to a sign change of the output signal. However, the transfer function, which is the ratio of the output and input signal, is not changed. Since the load impedance has an orientation independent characteristic, it also does not have any

influence on the transfer function. On the other hand, reversal of one of the branches of the VCCS leads to a sign change, which can be accounted for by allowing for a positive and negative transconductance value. Finally, reversing both branches again leaves the transfer function unchanged. Thus, as far as the number of possibilities is concerned, the generating elements can be represented by labelled undirected branches (the graph symbols of Figure 3-8 without arrows). On the other hand, an (arbitrary) reference direction should be used during analysis, to define the element orientation for which the transfer function is derived.

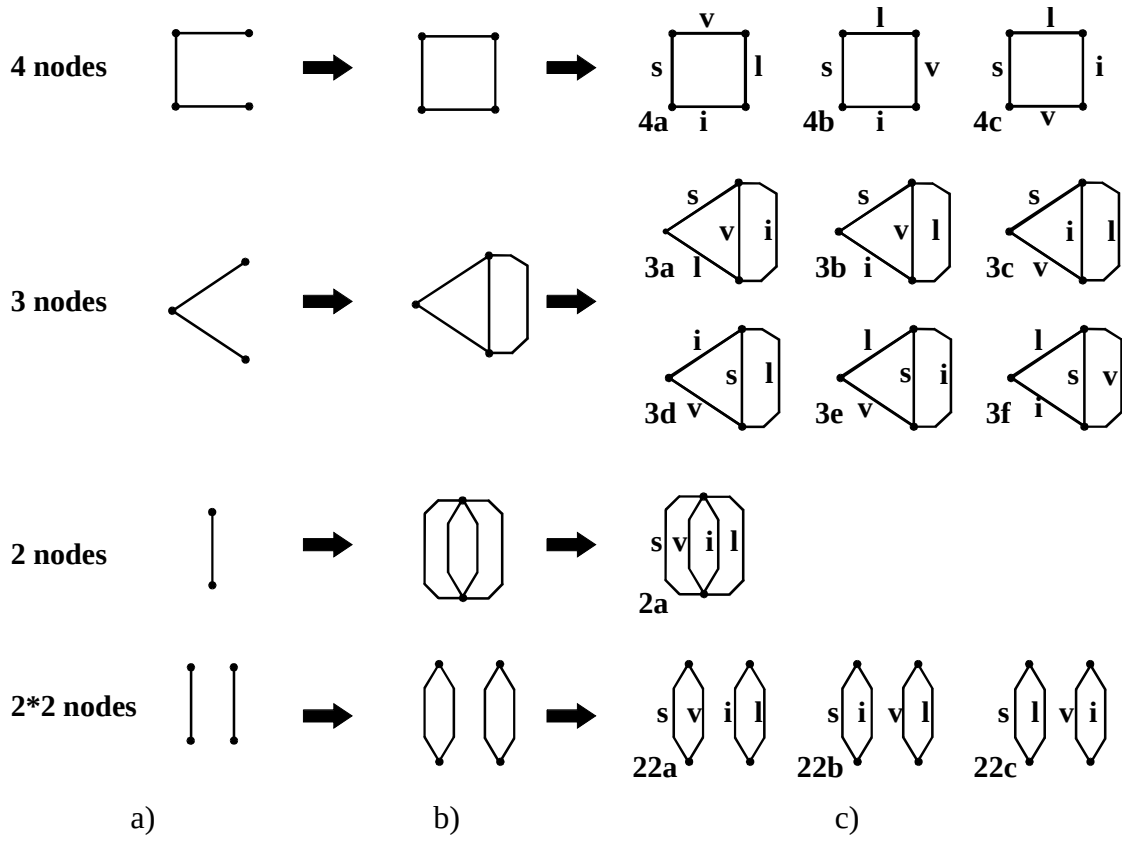


Figure 3-9: The generation of all different labelled graphs (column c) with one VCCS (v- en i-branch) and a source (s-branch) and load (l-branch) from tree graphs (column a) via unlabelled graphs (column b).

The task is now to find all different labelled graphs with the four branches mentioned. This will be done in two steps: first, the relevant unlabelled graphs are generated from tree graphs, and second, the different labelled versions of every of these unlabelled graphs are produced. From the considerations in the previous paragraphs, it follows that the relevant trees for the present problem are those for graphs with 2, 3 or 4 nodes, allowing for two subgraphs. These trees are shown in the a-column of Figure 3-9 [154]. Starting from them, links are added to form loops, up to the point where graphs with 4 branches result, in which all branches are connected in loops. These are shown in the b-column of Figure 3-9. Finally for every unlabelled graph, the different labelled graphs are generated, using the branch labels given in Figure 3-8. The results are shown in the c-column of Figure 3-9.

It should be noted that the graphs, consisting of two separated parts (the "2*2 nodes" graphs in Figure 3-9), may be redrawn with one node in common, without any effect on the operation of the corresponding circuit. This is because the Kirchhoff voltage equations are

not changed by joining the subgraphs at one node (no loops are added), nor are the current equations (no current can flow from one subgraph to the other without a return path).

From Figure 3-9c it appears that 13 different labelled graphs exist: 3 with 4 nodes, 6 with 3 nodes, 1 with 2 nodes and 3 with 2x2 nodes. For reference purposes, a unique name was given to each of them, indicating the number of nodes followed by a case identifier.

3.3.3 Systematic Analysis of the Transfer Function

The labelled graphs found in the previous section represent a circuit topology. By applying Kirchhoff's laws, the transfer properties of such circuits can be evaluated. This will now be done for graph "3f" (arbitrarily chosen), to illustrate the procedure. Since there are many graphs to be analysed, the analysis procedure is described in a systematic way, suitable for implementation in a software package with symbolic manipulation capabilities. The analysis is performed in 7 steps and aims at calculating the transactor properties, in terms of its transmission parameters.

1. *Draw a directed graph with node numbers.* The (arbitrary) directedness of the graph is needed, because reversal of the v-or i-branch can introduce sign changes in the transfer function. All resulting cases can be covered by allowing for both a positive and negative value of g. However, the directedness of the graphs is needed, to define the branch orientation for which the transfer function equations have been derived. The nodes are numbered 0, 1, 2 ...., N, and one of them is designated as the datum node (by convention node 0). The result is shown in Figure 3-10.

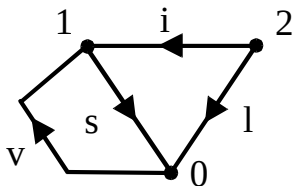


Figure 3-10: Directed graph with node numbering as used for the transfer property analysis for graph "3f" of Figure 3-9c.

2. *Write the node equations.* For a circuit with N nodes and B branches, N-1 independent KCL equations and (B-N+1) independent KVL equations exist [152]. Since the circuit contains a VCCS, which only has a admittance two-port representation and no impedance representation, KCL node equations are used (KVL loop equations would require substitutions for V_{branch} in terms of I_{branch} and Z_{branch} at step 3). These KCL equations for node 1 and 2 of Figure 3-10 are:

$$i_s - i_i - i_v = 0 \tag{3.13}$$

$$i_i + i_l = 0 \tag{3.14}$$

3. *Substitute the branch relations.* The branch currents can be expressed in terms of the branch voltages using admittance representations of the elements in the branches (Figure 3-8).

$$i_s = g_s \cdot (v_s - v_{sin}) \tag{3.15}$$

$$i_v = 0 \tag{3.16}$$

$$i_i = g \cdot v_v \tag{3.17}$$

$$i_l = g_l \cdot v_l \tag{3.18}$$

where v_{sin} is the open terminal independent source voltage, g_s is the source admittance, g is the VCCS transconductance and g_l is the load admittance.

4. *Express the branch voltages in terms of node voltages by means of KVL equations.* For the present example these equations are:

$$v_s = v_1 \tag{3.19}$$

$$v_v = -v_1 \tag{3.20}$$

$$v_i = v_2 - v_1 \tag{3.21}$$

$$v_l = v_2 \tag{3.22}$$

In fact steps 1-4 are easily possible by inspection from the graph, resulting in two equations in terms of the node-voltages:

$$g_s \cdot (v_1 - v_{sin}) - g \cdot -v_1 + 0 = 0 \tag{3.23}$$

$$g \cdot -v_1 + g_l \cdot v_2 = 0 \tag{3.24}$$

5. *Solve the set of equations for the node-voltages*. This is only possible if the determinant of the set of equation is non-zero. If it is zero, the circuit is non-functional. For the example the determinant evaluation leads to:

$$\det \begin{vmatrix} g_s + g & 0 \\ -g & g_l \end{vmatrix} = g_s \cdot g_l + g \cdot g_l \tag{3.25}$$

which is zero for g equal to:

$$g_{critical} = -g_s \tag{3.26}$$

Thus for a certain critical negative value of g, the set of equations has no solution. However, negative values for g are mainly used for specific applications e.g. for undamping in filter sections and oscillators, and their discussion is beyond the scope of this thesis. Such use of negative values of g requires a careful stability consideration. However, usually positive values for g are used, and a solution for the set of equation always exists in that case, given by:

$$v_1 = \frac{g_s}{g_s + g} \cdot v_{sin} \tag{3.27}$$

$$v_2 = \frac{g \cdot g_s}{(g_s + g) \cdot g_l} \cdot v_{sin} \tag{3.28}$$

6. *Calculate the transmission parameters of the transactor*. The four transmission parameters (see chapter 2), can be calculated by evaluating the limit of a ratio of source and load quantities, either for g_l approaching zero or infinity:

$$A = \left.\frac{v_{in}}{v_{out}}\right|_{i_{out}=0} = \lim_{g_l \to 0}\left(\frac{v_s}{v_l}\right) \tag{3.29}$$

$$B = \left.\frac{v_{in}}{i_{out}}\right|_{v_{out}=0} = \lim_{g_l \to \infty}\left(\frac{v_s}{g_l \cdot v_l}\right) \tag{3.30}$$

$$C = \left.\frac{i_{in}}{v_{out}}\right|_{i_{out}=0} = \lim_{g_l \to 0}\left(\frac{g_s \cdot (v_{sin} - v_s)}{v_l}\right) \tag{3.31}$$

$$D = \left.\frac{i_{in}}{i_{out}}\right|_{v_{out}=0} = \lim_{g_l \to \infty}\left(\frac{g_s \cdot (v_{sin} - v_s)}{g_l \cdot v_l}\right) \tag{3.32}$$

For the example under discussion the results are: A=0, B=1/g, C=0 and D=1. In obtaining these results, eqn. 3.19 and 3.22 are used to express the source and load voltage in terms of node voltages, and eqn. 3.15 and 3.18 to express the source and load current in terms of the branch voltages.

7. *Calculate the input and output conductance of the transactor*. As discussed in the previous chapter, the input and output impedance of the transactor can be expressed in terms of the transmission parameters. Because of the nature of the VCCS, an infinite input and output impedance often occur, while zero impedance situations don't. To avoid singularities in the calculations (division by zero), input and output conductance expressions will be used:

$$g_{in} = \frac{C \cdot Z_l + D}{A \cdot Z_l + B} \tag{3.33}$$

$$g_{out} = \frac{A + C \cdot Z_s}{B + D \cdot Z_s} \tag{3.34}$$

For the case of the example this results in $g_{in} = g$ and $g_{out} = 0$.

The last part of the above described analysis procedure has been automated using the mathematical software package MAPLE [160]. The node-equations for a topology are hand-written by inspection from the graphs. These serve as input for a MAPLE program, that solves the equations and calculates the transactor properties A, B, C, D, g_{in} and g_{out}. The results for circuits with one VCCS are described in the next paragraph.

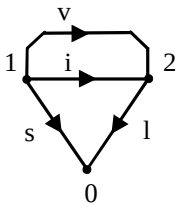
3.4 Discussion of the Results with one VCCS

The graphs of Figure 3-9c have been analysed, using the method described in the previous section. It appears that only 5 graphs result in potentially useful transactors: graph 3a, 2a, 22a, 3c and 3f. All other graphs will appear to be non-functional.

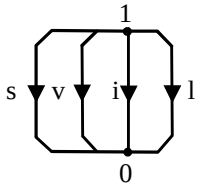
3.4.1 Potentially Useful Transactor Graphs

The directed graphs of potentially useful transactors are shown in Figure 3-11 and their transmission parameters are given in Table 3-8. The circuits corresponding to graph 3a and

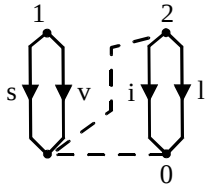
2a both configure the VCCS as a conductance element. For graph 3a it is connected in series with the source and load, while for graph 2a it is in parallel to them. A positive conductance is implemented by the graphs as drawn, the negative conductance results if either the direction of the v- or the i-branch of the VCCS is reversed.



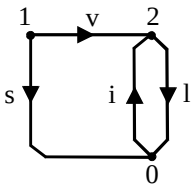
3a, "series conductance"



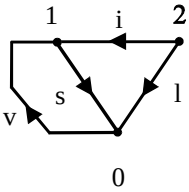
2a, "parallel conductance"



22a, transconductor e.g. CS-stage



3c,~voltage follower, e.g. CD-stage



3f, ~current follower, e.g. CG-stage

Figure 3-11: The graphs with one VCCS that correspond to useful transactors.

The other three graphs correspond to a transconductor, an approximate voltage follower and approximate current follower respectively. They can be implemented using familiar MOST amplifier stages: the Common Source (CS, graph 22a with lower terminals joined), Common Drain (CD, graph 3c) and Common Gate (CG, graph 3f) stages. These implementations will be discussed briefly.

Circuit graph	Functional description	A	B	C	D	g_{in}	g_{out}
3a	series conductance	1	$\frac{1}{g}$	0	1	$\frac{g}{1+g\cdot Z_l}$	$\frac{g}{1+g\cdot Z_s}$
2a	parallel conductance	1	0	g	1	$g+\frac{1}{Z_l}$	$g+\frac{1}{Z_s}$
22a	Transconductor e.g. CS-stage	0	$-\frac{1}{g}$	0	0	0	0
3c	Voltage follower, e.g. CD-stage	1	$\frac{1}{g}$	0	0	0	g
3f	Current follower, e.g. CG-stage	0	$\frac{1}{g}$	0	1	g	0

Table 3-8: Transmission parameters and input and output conductance of the useful transactor of Figure 3-11.

As shown in the Table 3-8, the CS stage has only a non-zero B parameter equal to -1/g. A CD stage additionally has A=1, resulting in a voltage gain equal to 1 according to eqn. 2.15, for $g\cdot Z_l >> 1$ (voltage follower). On the other hand, the CG stage has D=1, resulting in a current gain of 1 according to eqn. 2.18, for $g\cdot Z_s >> 1$ (current follower). Current or

voltage gains other than 1 and independent of Z_s and Z_l are not possible, because a ratio of two unequal transconductances is needed in that case, which requires at least two VCCSs.

Graph 22a is special in the sense that it consists of two subgraphs, that can be joined at an arbitrary node without changing the transfer function. Because of this, a transconductor with a floating input is possible, i.e. the voltage sense terminals are allowed to have an arbitrary common voltage. Ideally, this common-voltage should not affect the current of the transconductor.

The input and output conductances (also shown in Table 3-8) for case 3a and 2a are determined by g and the source and load impedances Z_s and Z_l. In contrast, the other cases have input and output conductances that are independent of the load and source impedance, respectively. The values are either equal to zero or to g.

3.4.2 Non-functional Graphs

Apart from the above discussed 5 useful cases, 8 non-functional graphs occur in Figure 3-9. The sets of equations for these graphs either have no solution or only have a zero solution. As this results in undefined transmission parameters, these graphs are non-functional. A closer look at these cases reveals three underlying reasons:

1. The i-branch is in series with a voltage sensing v-branch. Since no current can flow in the v-branch, and the voltage across the v-branch is undetermined, it is non-functional. This occurs for graph 4a, 4b, 4c, 3d and 22c.
2. The l-branch is in series with the (open) v-branch. Thus only a zero solution for the output voltage and current exists. This is true for graph 4a, 4b, 4c, 3e and 22b.
3. At one node only a s-branch and i-branch are connected. Since a current source can sustain an arbitrary voltage across its terminals without any influence on the current, the source voltage has no control over the circuit. If the source is a current source, two current sources are in series, without any control mechanism to equalise the currents. This problem occurs in the circuits of graph 4a, 4b, 3b and 22b.

These three above mentioned conditions should be avoided to find useful transactors. Formulated in a positive way, the following conditions should be satisfied:

1. The source should have control over the current of the VCCS.
2. The current of the VCCS should have an influence on a load quantity.

3.4.3 Omit v-Branches: KCL Graphs

In retrospect, it appears that many of the generated graphs are not useful, just because the v-branch does not conduct current. The question arises whether this cannot be made more visible in the graph generation phase. This is possible, by leaving the v-branch out of the graph. Since the current in that branch is zero, this *does not influence* the *KCL equations*. As the number of branches is reduced in this way, much less different graphs exist, and the graph generation becomes manageable. On the other hand, the absence of the v-branches *does* influence the KVL equations. Therefore, the v-branches must be added before

deriving KVL relations. Fortunately, this can be done in a systematic and automated way, as will be discussed in a moment. However, first we will reconsider the case with one VCCS to see how the method works. Repeating the graph generation, leaving out the v-branch, the graphs of Figure 3-12 and Figure 3-13 are found.

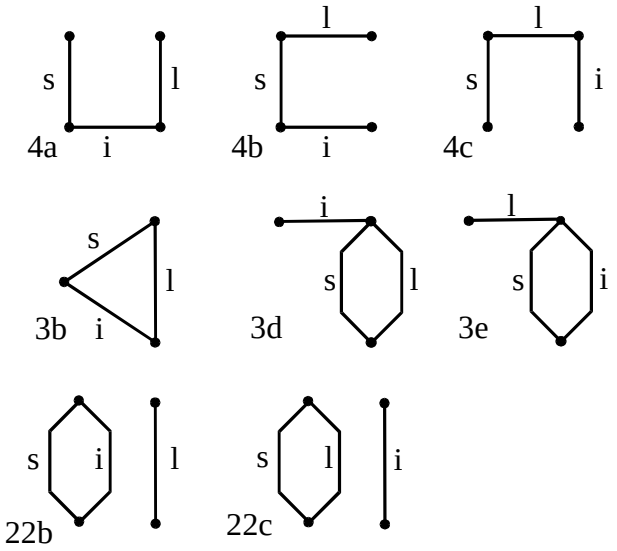


Figure 3-12: The 8 KCL graphs (without v-branch) corresponding to non-functional transactors. Apart from 3b all graphs have "dangling" i- or l-branches.

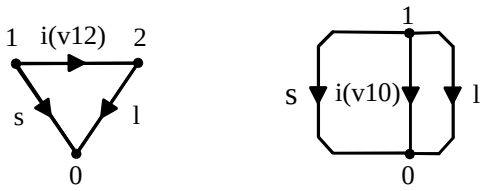
Figure 3-12 shows the graphs corresponding to non-functional transactors. From the 8 graphs, 7 have a "dangling" branch, either a i- or l-branch. Hence, the current in this branch is zero, which makes the branch non-functional. Figure 3-13 shows the graphs corresponding to potentially useful transactors. In this cases no dangling i- or l-branches occur. On the other hand, it appears that the s-branch is a dangling branch in some of the graphs, and can even be entirely separated from the i- and l-branch (graph 22a in Figure 3-13). This does not impede the realisation of useful transactors, since for instance transactors with voltage sensing only require a connection to VCCS voltage terminals.

Although it has no dangling branches, graph 3b in Figure 3-12 is also non-functional. This is because the source has no influence on the current. This is not directly recognisable from the graph, since additional information on the control voltage nodes is needed (which is not shown in the graph). However, in this case no solution for the set of Kirchhoff relations exists, which is discovered during the analysis of the transfer properties.

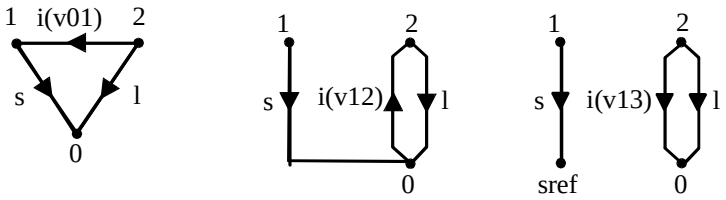
The main benefit of the v-branch deletion is the reduction of the number of graphs to be generated. This reduction is achieved for two reasons: first, there are less branches, resulting in less graphs. Second, a lot of graphs can be rejected because they have dangling i- or l-branches. For the graphs with one VCCS, in fact only three basically different KCL graphs without dangling i- and l-branches exist:

1. a triangular graph (case 3a, 3b and 3f)
2. a graph with 3 parallel branches (case 2a)
3. a graph with a parallel i- and l-branch and a separated or dangling s-branch (case 3c and 22a).

This is a significant reduction, compared to the original 13 graphs. Furthermore, this reduction will be even more significant if two VCCSs are considered.



3a, series conductance 2a, parallel conductance



3f, ~current follower 3c, ~voltage follower 22a, transconductor

Figure 3-13: The 5 KCL graphs corresponding to potentially useful transactors. The s-branch may be "dangling" or even separated.

3.4.4 Add v-branches Systematically

The information concerning the v-branch connection has to be added before considering the KVL equations. This however, can easily be done in an automatic way, by systematically allowing all possible node pairs of the KCL graph to control the voltage of the VCCS. Thus, in fact, different versions of the three basic KCL graphs exist for different control voltage definitions. The number of different versions is the number of combination of two different nodes out of all N nodes:

$$\binom{N}{2} = \frac{N!}{(N-2)! \cdot 2!} \tag{3.35}$$

For the triangular graph, for instance, the number of versions is 3!/(1!·2!)=3. The three cases correspond to a VCCS control voltage equal to v_{12} (graph 3a), v_{01} (graph 3f) or v_{20} (case 3b). The sign of the control voltage may be chosen arbitrarily, but should be recorded to establish a unique relation between the calculated expressions and the circuit implementation.

By deleting the v-branch from the graphs, it is no longer true that graphs consisting of two seperate subgraphs can arbitrarily be joined without changing the properties of the circuit. For the KCL relations this remains true. However, joining subgraphs at a node can change the KVL relations, that are not visible from the KCL graph. To find all graphs with two VCCSs, these cases are covered by subsequently connecting the source branch to every possible node of the rest of the circuit. It is sufficient so do this with one of the s-branch nodes, as the branch directions are arbitrary. This is done by introducing a special source node *"sref"* (see case 22a in Figure 3-13). During the automated graph generation and analysis procedure, the sref-node is connected to all other nodes in the graph, except for the other source node (a short-circuited s-branch render a non-functional circuit).

Furthermore, it is examined whether such graphs correspond to useful transactors with a floating input. To do so, the "sref" node is given an arbitrary voltage v_{sref}. A transactor is considered useful, if the transfer properties of the transactor are independent of the value of v_{sref} (ideal floating input).

Summarising, all circuit topologies with one VCCS, connected to a source and load, have been generated and evaluated using linear graphs. It appeared that most graphs that are non-functional, fail because the current in the voltage-sense branch is always zero. By removing the voltage-branch from the graphs, the KCL relations are not affected, while the number of (KCL) graphs to be considered is largely reduced. The v-branches can be added automatically and can be evaluated systematically by a MAPLE computer program, as we will see in the next section.

3.5 All Graphs of Transactors with Two VCCSs

In the previous section a method was developed to find all transactors with one VCCS, starting from KCL graphs. We will now apply the same method to find all transactor graphs with two VCCSs.

KCL Graph Generation

The KCL-graphs should satisfy the following conditions to avoid non-functionality:

- No self-loops are allowed (section 3.3.1).
- At least one loop should exist in which both an i-branch and an l-branch are present. This is because both VCCSs should affect at least one of the transmission parameters to avoid non-functionality (by definition). VCCSs can only do this by means of their current. If none of the VCCS currents flows through the load, none of the VCCSs has an effect on the output. Hence, ommission of a VCCS has no effect on any transmission parameters and the circuit would be non-functional.

With respect to the other branches the following observations can be made:

- The s-branch can be connected in one or more loops with other branches, but may also occur as a dangling or separate branch (see section 3.4.3 and 3.4.4).
- The second i-branch is in principle equivalent to the first one. It can also be connected in a loop with other branches, to affect the transmission parameters by means of the i-branch current. If the i-branch is not connected in any loop, its current is zero. Hence, it cannot influence any transmission parameter directly by means of its current (its contribution to all KCL equations is zero). To avoid non-functionality, transmission parameters should be affected by means of KVL equations. As the voltage across a current source is arbitrary, the contribution has to come from the v-branch of the VCCS. As the current is zero, the v-branch voltage is also zero, if a finite transconductance value is assumed. Consequently, both v=0 and i=0 for the v-branch, i.e. the equations for a nullator one-port. This nullator can impose a KVL relation that affects transmission parameters and is changed if the VCCS is omitted (i.e. non-functionality can be avoided). In a physical circuit realisation, a nullator with 2 element

equations (v=0 and i=0) should be combined with a norator with no element equations (arbitrary voltage and current) to form a nullor [14]. The i-branch of the VCCS can act as norator. In chapter 4 this will be discussed further when dealing with voltage and current follower circuits.

The two observations above do not lead to further restrictions: the second i-branch and the s-branch can be, but need not be connected to other branches. As far as the resulting KCL equations are concerned, the s- and i-branch are either fully connected (allowing for a non-zero branch current) or seperate branches (zero branch current). Hence, there are 4 different possibilities to construct KCL graphs:

a) One fully connected graph (all branches connected at both ends): branch set {s,i,i,l}.

b) Two fully connected separated subgraphs: {i,l}{s,i}.

c) One fully connected subgraph and one separated single branch: {s,i,l}{i} or {s}{i,i,l}.

d) One fully connected subgraph and two separated single branches {s}{i}{i,l}

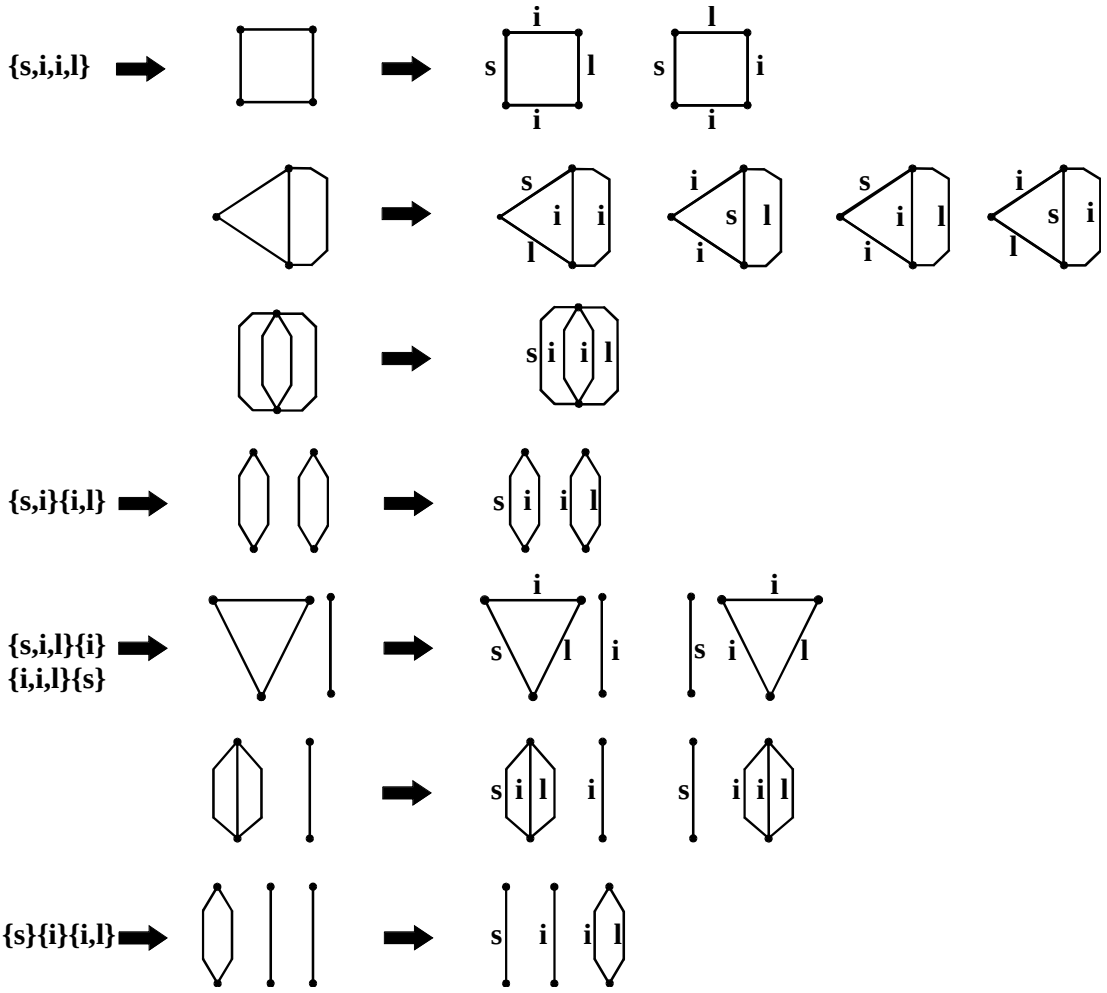


Figure 3-14: KCL graph generation for circuits with two VCCS.

Figure 3-14 depicts the KCL graph generation, resulting in 13 different graphs. It proceeds in a very similar way as in Figure 3-9. However, now there are two equivalent i-branches instead of a v- and i-branch, which reduces the number of labelled graphs derived from an unlabelled graph. Furthermore, now graphs with separate single branches exist.

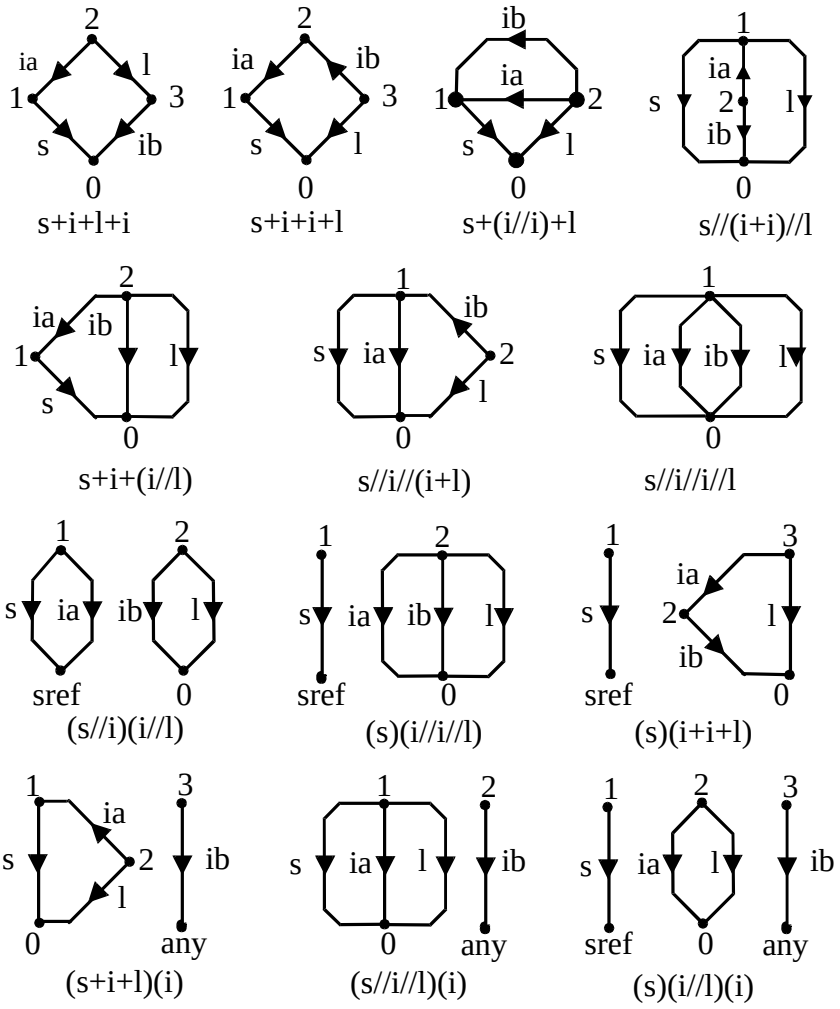


Figure 3-15: The 13 directed labelled KCL graphs for transactors with two VCCSs. For every graph $\binom{N}{2}^2$ ***versions exist, since*** v_a ***and*** v_b ***can be controlled by an arbitrary combination of nodes.***

The directed labelled versions of the 13 graphs are shown in Figure 3-15. These KCL graphs are drawn and assigned node names and labels, using the following conventions:

- The i-branches are equivalent, but are given different names i_a and i_b to establish an unambiguous relation between the terms in the derived transfer function expression and the branches in the graphs. The name assignment is arbitrary.
- The node-numbering is arbitrary, except for the s-branch. If the s-branch occurs in a KCL graph consisting of more than one seperated subgraphs, its lower node is labelled "sref" (source reference). As discussed at the end of section 3.4, the “sref” node is connected to all other nodes during the v-branch addition.

The lower node of a separated i-branch is given the label "any", since it can be connected to any node in the circuit, without affecting KCL or KVL equations. This is because the i-branch current is zero (open ended branch), while the voltage across the branch can take arbitrary values. Hence, the “any” node can be connected to an arbitrary node.

As shown in Figure 3-15, every KCL graph has been assigned a unique name, referring to the interconnection of its branches. The names list the branch names (e.g. s+(i//i)+l for the 3rd graph), starting with the source, then going clock-wise through a loop in the graph (two times an i-branch in this case), and ending with the branch connected to the other side of the s-branch (the l-branch). The symbols "+" and "//" are used to designate series and parallel connection respectively. Brackets are used to avoid ambiguity in the naming or indicate the existence of subgraphs. Thus s+(i//i)+l refers to a graph with 3 nodes, in which branch s is in series with a parallel connection of two i-branches, while branch l closes the loop to the source. An example of a name of a graph consisting of two subgraphs is (s//i)(i//l): one subgraph has a parallel s- and i-branch, the other a parallel i- and l-branch.

Complete Graphs by Adding v-branches

Having generated the different graphs, the control voltages v_a and v_b of the VCCSs need to be considered. Concretely, this means that node pairs must be assigned to the control voltages. To avoid that these voltages are zero, two different nodes should be assigned. Since there are two voltages to be assigned, the total number of combinations is equal to the square of the number in eqn. 3.35: $\binom{N}{2}^2$. Furthermore, the "sref"-node in the graphs with a separated s-branch is to be joined with each of the other nodes, except for node 1. Finally, the "sref" node is given an arbitrary voltage to check the functionality as transactor with a floating input.

For the 13 graphs of Figure 3-15 this leads to about 500 graphs. Because of the large number of possibilities, an automated analysis of the transfer function of the graphs as discussed in the previous section is indispensable. A MAPLE program was written for this purpose. MAPLE was chosen for this purpose, because of its powerful symbolic analysis capabilities. In the next paragraph the results of this analysis will be discussed.

If all cases are analysed in a straightforward manner, some cases are analysed two times. This is because of two reason:

- The two VCCSs are equivalent. If the two i-branches are in equivalent positions with respect to the s- and l-branch, the case with $v_a=v_{n1,n2}$ and $v_b=v_{n3,n4}$ results in the same transfer properties than for $v_a=v_{n3,n4}$ and $v_a=v_{n1,n2}$. This is easily recognised from Figure 3-14/ This occurs for graphs s+i+l+i, s+(i//i)+l, s//(i+i)//l, s//i//i//l, (s)(i//i//l) and (s)(i+i+l).
- Graphs with a separated s-branch, with sref connected to two different nodes are sometimes equivalent. This occurs for the graphs (s//i)(i//l), (s)(i//i//l) and (s)(i//l)(i).

The MAPLE program recognises these equivalencies, and analyses only one case.

3.6 Potentially Useful Transactors with two VCCSs

In the following two paragraphs the results of the transfer property analysis for the graphs with two VCCSs will be presented. First circuits with a non-floating input are discussed in section 3.6.1, and then the floating input cases in section 3.6.2. The main objective is to find out whether the 9 desired transactors defined in chapter 2 can be implemented.

3.6.1 Transactor with a Non-Floating Input

Transmission parameter expressions resulting from the analysis of graphs of circuits with a non-floating input are given in Appendix A. All non-listed cases either result in no solution or a zero solution, i.e. are non-functional. A look at the results in Appendix A shows 133 cases rendering a solution, i.e. at least one of the transmission parameters has a non-zero value. These cases are printed grouped on non-zero transmission parameters. It appears that groups of cases with very similar solutions exist, which means that a given set of transfer properties can be implemented with several different circuits. To find out which types of transactors can be implemented, Table 3-9 lists all different combinations of non-zero transfer parameters that are found in Appendix A. The table also shows the resulting input impedance and output impedance, together with some remarks on the usefulness of the case.

Non-zero transmission parameters				**Z_{in}**	**Z_{out}**	**Usefulness of the transfer function**
A (=1)				∞	0	Voltage Follower, A_v=1
	B			∞	∞	**Transconductor, Y_t=1/B**
			D (=1)	0	∞	Current Follower, A_i=1
A	**B**			∞	$\frac{\mathbf{B}}{\mathbf{A}}$	**Voltage input, adaptation to the load impedance => A_v, Y_t**
A (=1)			D (=1)	Z_l	Z_s	Impedance adaptation at both ports, however dependent on Z_s and Z_l
	B	C		$\frac{B}{C \cdot Z_l}$	$\frac{B}{C \cdot Z_S}$	Gyrator
	B		**D**	$\frac{\mathbf{B}}{\mathbf{D}}$	∞	**Adaptation to the source impedance, current output => Z_t, A_i**
A	B	C		$\frac{A \cdot Z_l + B}{C \cdot Z_l}$	$\frac{B}{A + C \cdot Z_s}$	Impedance adaptation at both ports, however dependent on Z_s and Z_l
A	B		D	$\frac{A \cdot Z_l + B}{D}$	$\frac{B + D \cdot Z_s}{A}$	Impedance adaptation at both ports, however dependent on Z_s and Z_l
A (=1)		C	D	$\frac{A \cdot Z_l}{C \cdot Z_l + D}$	$\frac{D \cdot Z_s}{A + C \cdot Z_s}$	Impedance adaptation at both ports, however dependent on Z_s and Z_l
	B	C	D	$\frac{B}{C \cdot Z_l + D}$	$\frac{B + D \cdot Z_s}{C \cdot Z_s}$	Impedance adaptation at both ports, however dependent on Z_s and Z_l
A	**B**	**C**	**D**	$\frac{\mathbf{A \cdot Z_l + B}}{\mathbf{C \cdot Z_l + D}}$	$\frac{\mathbf{B + D \cdot Z_s}}{\mathbf{A + C \cdot Z_s}}$	**Impedance adaptation at both ports independent of Z_s and Z_l if: $A \cdot D = B \cdot C$**

Table 3-9: The different combinations of non-zero transmission parameters that can be implemented with two VCCSs and the resulting transactor properties. The cases in bold correspond to useful transactors defined in chapter 2.

Comparison with the Requirements of Chapter 2

In chapter 2 it was found that 9 cases are especially useful: those with transmission parameter combinations: A, B, C, D, AC, BD, AB, CD and ABCD. From Table 3-9 and Appendix A it appears that four of these are directly available in a useful form: the parameter combinations B, AB, BD and ABCD, printed in bold. Case A and D are also covered, however only for A=1 (voltage follower) and D=1 (current follower), which is too restricted for general applicability. The useful cases printed in italics are all cases with either infinite or accurate port impedances. This result can easily be understood intuitively, since a VCCS has both a high input and output impedance, and can also be configured to implement an impedance. Apart from the mentioned 4 useful transmission parameter combinations, 8 other combinations are found in Table 3-9. They realise an input and output port impedance, that depends on the impedance at the other port. Thus the impedance connected to one port is reflected to the other, which is not generally acceptable. However, certain special cases of this impedance transformation can be useful, e.g. for case BC known in network theory as a Gyrator [152]. This network element can be useful in filter design, e.g. to emulate an inductor behaviour using a capacitor. However, a detailed discussion of filter design aspects is beyond the scope of this thesis.

Desired Z_{in}	Desired Z_{out}	Desired parameters	Realisable with case	Additional conditions
∞	0	A	AB	$B << A \cdot Z_l$
∞	∞	B	B	-
0	0	C	BC	$B << C \cdot Z_s \cdot Z_l$
0	∞	D	BD	$B << D \cdot Z_s$
∞	accurate	AB	AB	-
0	accurate	CD	BCD	$B << D \cdot Z_s$
accurate	0	AC	ABC	$B << A \cdot Z_l$
accurate	∞	BD	BD	-
accurate	accurate	ABCD	ABCD	$A \cdot D = B \cdot C$

Table 3-10: Overview of the implementation possibilities of the 9 desired transactors, and the additional conditions that have to be met.

Comparing the 4 implementation possibilities with the 9 required ones defined in the previous chapter, it appears that 5 cases are not yet covered. Those cases all require the realisation of a low port impedance. A closer look at Table 3-9 shows that the desired properties can be approximated for low values of B. Table 3-10 shows the exact conditions that have to be satisfied, to implement the 5 missing transactors. Together with the 4 unconditionally useful cases, which are also shown in the table, all 9 desired transactors can be implemented. The conditions listed in the table all require small values of B compared to the load and source impedances, which corresponds to large values of the transconductance compared to $1/Z_s$ or $1/Z_l$. For high source and load impedances this can usually be realised with single MOSTs, e.g. by using large aspect ratios and/or increasing the bias current. If this is not sufficient, one can resort to multi-stage transconductance amplifiers, e.g. consisting of a high voltage-gain stage followed by a transconductance.

Transmission Parameter Expressions

Apart from the type of transactors that can be implemented, the expressions found for transmission parameters are important, e.g. because they determine the tuning range. The number of cases is quite large. However, the following observations help to reduce the number of cases and help to acquire insight:

- Looking at the transmission parameter expressions found in Appendix A, many similar ones can be found. This can intuitively be understood, since they are all determined by only two transconductances g_a and g_b of the two VCCS elements $VCCS_a$ and $VCCS_b$.

- As expected from dimension considerations, the form of the expression of the transmission parameters A and D are ratios of transconductances g (or equal to 1), while B and C are of the form 1/g and g respectively.

Name	Definition	Comment
g_P	g_a or g_b	"Primary" VCCS transconductance
g_Σ	g_a+g_b	Sum
g_Δ	g_a-g_b	Difference
g_Π	$g_a \cdot g_b$	Product
$g_{\Pi/\Sigma}$	$g_a \cdot g_b/(g_a+g_b)$	Product/Sum
$g_{\Pi/\Delta}$	$g_a \cdot g_b/(g_a-g_b)$	Product/Difference
$g_{\Sigma\Delta}$	g_Σ or g_Δ	Sum or Difference
$[]_{1,2}$	index 1 or 2	To distinguish multiple occurrences

Table 3-11: Different short hand notations used to simplify the transmission parameter expressions in terms of transconductances g_a and g_b.

- In order to simplify the expressions and to combine cases, the short hand notations listed in Table 3-11 will be used. The actual transconductance expressions that occur can be divided in two categories: "primary" and "secondary" ones. The actual VCCS transconductances g_a or g_b will be called primary transconductances, that will be indicated as g_P. The secondary transconductance expressions are combinations of g_a and g_b, resulting from parallel or series connections of VCCSs. For a parallel and anti-parallel connection, the sum g_Σ and difference g_Δ are found. For a series and anti-series connection, the product of g_a and g_b, divided by their sum or difference occurs, indicated as $g_{\Pi/\Sigma}$ and $g_{\Pi/\Delta}$. In order to distinguish between different occurrences of the same expression, the indices 1 and 2 are used.

- The direction assignment for the v- and i-branch in the graphs of Figure 3-15 is arbitrary. Reversal of one of these has the same effect as changing the sign of the corresponding transconductance, while reversal of both has no net effect. Furthermore, the assignment of the names g_a and g_b is also arbitrary, so that these may also be interchanged. Table 3-12 shows the effect of the above mentioned actions on the transconductance expressions. If, for instance, the names g_a and g_b are interchanged in a graph, a "g_Δ"-term in an expression becomes a "$-g_\Delta$"-term (exchanging a and b in $g_\Delta=g_a-g_b$, results in g_b-g_a, which is, according to definition in Table 3-11, equal to $-g_\Delta$). For the present discussion on the types of different transactors, these differences in sign and labelling are of minor

importance, so that many cases are discussed in one run. In later chapters these differences will be examined in more detail.

Original expression	g_a <=> g_b (exchange)	g_a => $-g_a$ (sign change)	g_b => $-g_b$ (sign change)
g_a	g_b	$-g_a$	g_a
g_b	g_a	g_b	$-g_b$
g_Σ	g_Σ	$-g_\Delta$	g_Δ
g_Δ	$-g_\Delta$	$-g_\Sigma$	g_Σ
g_Π	g_Π	$-g_\Pi$	$-g_\Pi$
$g_{\Pi/\Sigma}$	$g_{\Pi/\Sigma}$	$g_{\Pi/\Delta}$	$-g_{\Pi/\Delta}$
$g_{\Pi/\Delta}$	$-g_{\Pi/\Delta}$	$g_{\Pi/\Sigma}$	$-g_{\Pi/\Sigma}$

Table 3-12: Transformations of the g-term expressions in the transmission parameter expressions, due to changes in the (arbitrary) name or sign assignment.

Possible Combinations of Transmission Parameter Expressions

Using the notation defined in Table 3-11, the transmission parameter expressions for the graphs with two VCCSs are shown in Table 3-13 (one or two non-zero transmission parameters) and Table 3-14 (3 or 4 non-zero transmission parameters).

ABCD combination	|A|	|B|	|C|	|D|	Number of graphs
A	1	0	0	0	3
B	0	$1/g_\Sigma$	0	0	1
	0	$1/g_{\Pi/\Sigma}$	0	0	4
	0	$1/g_P$	0	0	23
D	0	0	0	1	3
AB	g_{P1}/g_{P2}	$1/g_{P2}$	0	0	1
	g_P/g_Σ	$1/g_\Sigma$	0	0	1
	g_Σ/g_P	$1/g_P$	0	0	1
	1	$1/g_\Sigma$	0	0	1
	1	$1/g_{\Pi/\Sigma}$	0	0	4
	1	$1/g_P$	0	0	15
AD	1	0	0	1	6
BC	0	$1/g_{P1}$	g_{P2}	0	1
BD	0	$1/g_{\Pi/\Sigma}$	0	1	4
	0	$1/g_\Sigma$	0	1	1
	0	$1/g_\Sigma$	0	g_P/g_Σ	1
	0	$1/g_P$	0	g_Σ/g_P	1
	0	$1/g_{P1}$	0	g_{P2}/g_{P1}	1
	0	$1/g_P$	0	1	15

Table 3-13: Possible combinations of one or two non-zero transmission parameters occurring in Appendix A (see also Table 3-11, Table 3-12).

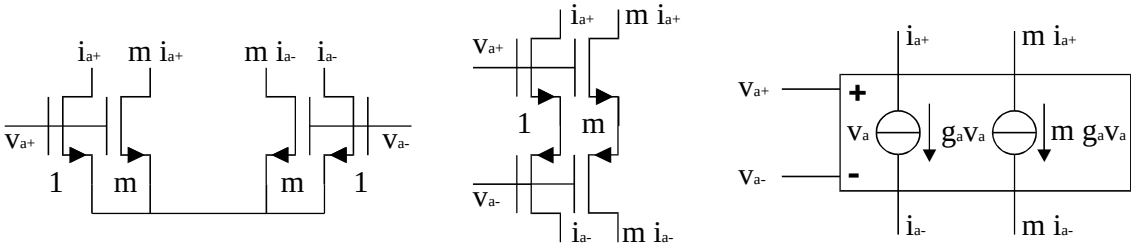
Absolute values of A, B, C and D are given in the table. The exact sign to graph correspondence can be found in Appendix A. The number of graphs with the same transmission parameter expressions is also listed. It appears that some parameter combinations are only realised by one circuit topology, while others can be realised in many ways. The question might rise, whether these different implementations are fully equivalent since they have the same transmission parameters. This is true as far as the small signal transfer characteristics are concerned, assuming ideal VCCSs. However, in general this will not be true for other properties, taking into account second order effects. These aspects will be touched on in later chapters.

ABCD combination	|A|	|B|	|C|	|D|	Number of graphs
ABC	g_{P1}/g_{P2}	$1/g_{P2}$	g_{P1}	0	1
	g_{Σ}/g_{P1}	$1/g_{P1}$	g_{P2}	0	1
	1	$1/g_{P1}$	g_{P2}	0	1
ABD	-1	$1/g_{\Pi/\Sigma}$	0	1	2
	1	$1/g_{\Pi/\Sigma}$	0	1	4
	g_{P1}/g_{P2}	$1/g_{P2}$	0	1	1
	g_P/g_{Σ}	$1/g_{\Sigma}$	0	1	1
	g_{Σ}/g_P	$1/g_P$	0	1	1
	1	$1/g_{\Sigma}$	0	1	1
	1	$1/g_{\Sigma}$	0	g_P/g_{Σ}	1
	1	$1/g_P$	0	g_{Σ}/g_P	1
	1	$1/g_{P1}$	0	g_{P2}/g_{P1}	1
	1	$1/g_P$	0	1	11
ACD	1	0	$g_{\Pi/\Sigma}$	1	2
	1	0	g_{Σ}	1	1
	1	0	g_P	1	6
BCD	0	$1/g_{P1}$	g_{P2}	1	1
	0	$1/g_{P1}$	g_{P2}	g_{Σ}/g_{P1}	1
	0	$1/g_{P1}$	g_{P2}	g_{P2}/g_{P1}	1
ABCD	g_{P1}/g_{P2}	$1/g_{P2}$	g_{P1}	1	1
	g_{P1}/g_{Σ}	$1/g_{\Sigma}$	$g_{\Pi/\Delta}$	g_{P2}/g_{Σ}	1
	g_{P1}/g_{Σ}	$1/g_{\Sigma}$	$g_{\Pi/\Sigma}$	g_{P1}/g_{Σ}	1
	g_{Σ}/g_{P1}	$1/g_{P1}$	g_{P2}	1	1
	1	$1/g_{P1}$	g_{P2}	g_{Σ}/g_{P1}	1
	1	$1/g_{P1}$	g_{P2}	1	1
	1	$1/g_{P1}$	g_{P2}	g_{P2}/g_{P1}	1

Table 3-14: Possible combinations of 3 or 4 non-zero transmission parameters occurring in Appendix A (see also Table 3-11, Table 3-12).

Although sometimes 3 or 4 expressions are encountered in Table 3-14, there are only two degrees of freedom to choose the transmission parameters (g_a and g_b). Thus it is not possible to choose more than two transmission parameters independently. Except for the

ABCD case, this is no problem, since two degrees of freedom are sufficient to choose either a transactance value (e.g. voltage gain A_v), or a transactance value and a port impedance. In order to be able to choose two port impedances and a transactance value independently for the ABCD case, 3 degrees of freedom are needed. Furthermore, in that case the condition $A \cdot D = B \cdot C$ is desired so that the transactor port impedances are independent of Z_s and Z_l. Fortunately, Table 3-14 shows that 3 of the ABCD cases satisfy this condition. The desired third degree of freedom can be implemented by multiplying all transmission parameters with an equal scale factor. This results in a transactance change with that factor, while the transactor port impedances do not change, since these are ratios of transmission parameters. Such multiplication of transmission parameters can be established by providing the VCCS with an extra, m times larger output current as shown in Figure 3-16.



a) b) c)

Figure 3-16: An extra, m-times larger, copy of a VCCS output current can be obtained by duplicating the VCCS output transistors in a ratio 1:m. a) Anti-series NMOST implementation; b) Series complementary implementation; c) The symbol used for the VCCS with two output currents.

Using this building block, an extra degree of design freedom is added, which can be used to fix port impedances and the transactance independently. Figure 3-17 shows an example of how this can be done.

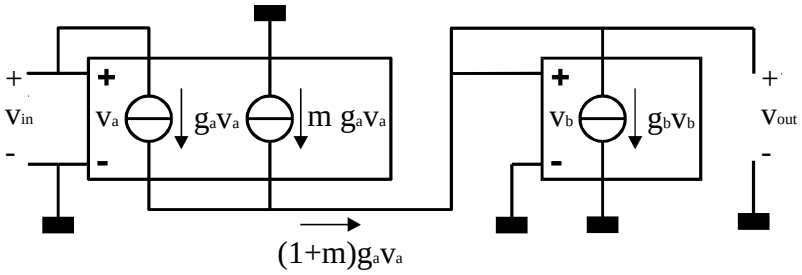


Figure 3-17: Example of a transactor with three degrees of freedom in choosing parameter A,B,C and D.

The resulting transmission parameters are easily calculated by inspection from the circuit:

$$A = \frac{g_b}{g_a(1+m)} \quad B = \frac{1}{g_a(1+m)} \qquad C = \frac{g_b}{(1+m)} \qquad D = \frac{1}{(1+m)} \tag{3.36}$$

Thus all parameters are divided by (1+m), resulting in: $Z_{in}=1/g_a$ and $Z_{out}=1/g_b$, while the voltage gain is given by:

$$A_v = \frac{Z_l\,(1+m)}{\frac{g_a}{g_b}Z_l + \frac{1}{g_a} + g_b Z_s Z_l + Z_s} \overset{\substack{Z_{in}=Z_s \\ Z_{out}=Z_l}}{=} \frac{1}{4}\frac{Z_l}{Z_s}(1+m) \tag{3.37}$$

Thus g_a is used to make Z_{in} equal to Z_s, g_b to fix $Z_{out} = Z_l$, while m can be used to give A_v a suitable value.

3.6.2 Transactors with a Floating Input

In many applications the signal of interest is the difference between two voltages, while there is a desire to choose the common voltage freely. Furthermore, such voltages are sometimes subject to large common mode interference. Circuits with a floating input, with transfer properties that are independent of the common-mode voltage are useful in such cases: ideally they completely reject the common voltage and transfer the differential part. Such transactors can be implemented with VCCS graphs with a separate source branch. The "sref" node of the graphs in Figure 3-15 is given an arbitrary voltage v_N, where N is the highest node number in the graph. Figure 3-18 shows the involved graphs with the node number assignment.

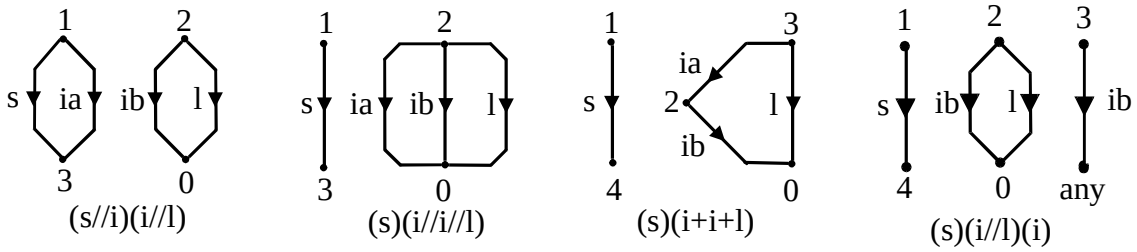


Figure 3-18: The 4 KCL graphs with two VCCSs and a floating source.

A transactor with a truly floating input, should have transfer properties that are independent of the value of v_N. The graphs satisfying this condition are listed at the end of Appendix A and in Table 3-15. It appears that transactors with high and accurate port impedances can be implemented: the B, AB and BD cases. Furthermore combination BC implements a gyrator with floating input and output ports.

ABCD combination	|A|	|B|	|C|	|D|	Number of Graphs
B	0	$1/g_P$	0	0	7
	0	$1/g_\Sigma$	0	0	1
	0	$1/g_{\Pi/\Sigma}$	0	0	1
AB	g_{P1}/g_{P2}	$1/g_{P2}$	0	0	1
BC	0	$1/g_{P1}$	g_{P2}	0	1
BD	0	$1/g_{P1}$	0	g_{P2}/g_{P1}	1

Table 3-15: Different combinations of the transmission parameter expressions found for circuits with two VCCSs and a floating input.

3.6.3 Value and Tuning Range of Transmission Parameters

The expressions for the transmission parameters will now be examined with respect to the range of practically implementable values. We will concentrate on simple MOST implementations of the VCCSs. Basically, there are two ways to change the transconductance of a MOST: firstly by changing its gate geometry and secondly by changing its biasing. In section 3.2.4 typical values for the transconductance of different types of VCCSs can be found. For an NMOST operating in strong inversion and saturation, a maximum transconductance of about 100μS times W/L is found for V_{GT} = 1 V and I_D = 50 μA. Thus for W/L=1, the impedance level is in the order of 10 Kohm. This transconductance can be enlarged by a factor W/L, however at the cost of an increase in current consumption with the same factor (assuming constant bias voltages). Thus a 50 ohm impedance level (g_m = 20 mS) is roughly achievable at W/L=200, e.g. with a saturated NMOST operating at I_D = 10 mA and V_{GT} = 1 Volt. On the other hand, small transconductance values of less than 1μS are possible for W<<L. Much lower values, can be achieved in weak inversion, down to the nS range. Thus the realisable range of transconductance values allows transmission parameter values 1/B and C to be chosen over several decades from roughly 10^{-1}S to below 10^{-9}S, which is appropriate for most applications. Furthermore, since both a large and a small ratio between transconductances can be realised, transmission parameter A and D can be chosen in an range around 1. If an accurate ratio is desired, it is usually implemented using different numbers of matched devices. Typically, ratios between 1:100 and 100:1 are used.

Electronic Controllability

Apart from the nominal value of the transmission parameters that can be realized, the control range of the parameters is of great interest for applications requiring electronic control. To get insight in the controllability of the parameters, it is useful to define a nominal transconductance value g_0, and a transconductance control parameter a_c. A convenient definition for the control parameter a_c is the ratio between the maximum transconductance and its nominal value. If the nominal transconductance g_0 is defined as the geometric mean of the maximum and minimum value of the transconductance:

$$g_0 = \sqrt{g_{min} \cdot g_{max}} \tag{3.38}$$

then: $$a_c = \frac{g_{max}}{g_0} = \frac{g_0}{g_{min}} \tag{3.39}$$

Thus the transconductance is controllable from g_0/a_c to $a_c \cdot g_0$. With reference to Table 3-7, a_c is typically found to be $\sqrt{10}$ for a SVCCS with saturated NMOSTs, 10 for a LVCCS with a triode NMOSTs and $10\sqrt{10}$ for a EVCCS based on weak inversion NMOSTs.

Using the g_0 and a_c definitions for g_a and g_b of the two VCCSs, the control range of the secondary transconductance expressions from Table 3-11 can be calculated. The results are shown in Table 3-16, where it is assumed that g_a and g_b have equal nominal values g_0. This does not restrict the value of the results, since g_0 cancels in the calculation of the final control range, which is the ratio of the maximum and minimum value of the transmission parameter. The left half of the table shows the control ranges for 1/B and C terms, which

both have the dimension of a transconductance. All parameters have a control ratio a_c^2, except for the expressions with g_Δ. For this case, it is possible to change the sign of the transconductance, since g_a can both be larger and smaller than g_b. Although electronic change of the sign might be useful in some applications, usually only the magnitude of the transmission parameter needs to be electronically variable. Since the absolute transconductance value is relevant in that case, $|g_\Delta|$ is listed in the table. As the difference between g_a and g_b can be made arbitrarily small, this leads to an infinite control range. In practice this range is limited e.g. by accuracy and Signal-to-Noise ratio considerations (g_a and g_b have a finite accuracy, which leads to large inaccuracies for small values of $|g_\Delta|$. The SNR is adversely affected, because the output currents of two VCCSs are subtracted, while their noise contributions add up).

The right half of the table shows the control ranges for the A and D terms, which are transconductance ratios. Again the terms with $|g_\Delta|$ have an infinite control range. The terms with g_Σ have a control ratio a_c^2, and the ratio of primary VCCS transconductances even has a control ratio a_c^4. This is because both the numerator and denominator term is tuneable.

1/B or C				A or D			
g-term	**minimum value**	**maximum value**	**ratio**	**g-term**	**minimum value**	**maximum value**	**ratio**
g_P	$\frac{g_0}{a_c}$	$a_c \cdot g_0$	a_c^2	$\frac{g_{P1}}{g_{P2}}$	$\frac{1}{a_c^2}$	a_c^2	a_c^4
g_Σ	$\frac{2 \cdot g_0}{a_c}$	$2 \cdot a_c \cdot g_0$	a_c^2	$\frac{g_\Sigma}{g_P}$	$1+\frac{1}{a_c^2}$	$1+a_c^2$	a_c^2
$\lvert g_\Delta \rvert$	0	$\frac{a_c-1}{a_c} \cdot g_0$	∞	$\frac{\lvert g_\Delta \rvert}{g_P}$	0	$1-\frac{1}{a_c^2}$	∞
$\frac{g_\Pi}{g_\Sigma}$	$\frac{g_0}{2 \cdot a_c}$	$\frac{a_c \cdot g_0}{2}$	a_c^2	$\frac{g_P}{g_\Sigma}$	$\frac{1}{1+a_c^2}$	$\frac{a_c^2}{1+a_c^2}$	a_c^2
$\frac{g_\Pi}{\lvert g_\Delta \rvert}$	$\frac{g_0 \cdot a_c}{a_c^2-1}$	∞	∞	$\frac{g_P}{\lvert g_\Delta \rvert}$	$\frac{a_c^2}{a_c^2-1}$	∞	∞

Table 3-16: The electronic control range (maximum/minimum) of transconductance expressions occurring in Table 3-13 and Table 3-14.

3.7 Summary and Conclusions

In this chapter the possibilities to implement transactors based on the transconductance of MOS transistors have been examined. For this purpose *all graphs of transactor two-ports with one or two VCCSs* have been generated and analysed. The main results that were achieved are summarised below.

The MOST as a Voltage Controlled Current Source

- A MOST biased at a sufficiently high drain-source voltage, shows saturation of the drain current, and can be idealised as a VCCS, both in weak and strong inversion. Furthermore several simple MOST circuits behave like a VCCS.
- Depending on the operating region of the MOS transistor, three types of Generalised VCCS characteristics can be approximated:
    1. Linear VCCS (e.g. triode MOST with cascode circuit)
    2. Square-law VCCS (e.g. saturated strong inversion MOST)
    3. Exponential VCCS (e.g. weak inversion MOST)
- The single MOST VCCSs are common-terminal two-ports: they have a connection between a voltage and a current terminal. For VCCS circuit synthesis, a more flexible VCCS with separate voltage and current terminals is used. It can be implemented by a series or anti-series connection of two common-terminal VCCSs.

Generation and Evaluation of Transactor Graphs

All graphs of circuits with a source, load and one or two VCCSs were generated and analysed systematically. The most important aspects of the method used are:

- Directed labelled graphs are used to represent the circuit topology with branches labelled s-branch (source), l-branch (load) and v- and i-branch (VCCS). To avoid non-functional graphs (section 3.3.1), all branches should be connected in loops and no self-loops are allowed. Such graphs are generated from trees by adding links.
- Since branch reversal either has no effect (s- or l-branch), or only affects the sign of terms in transfer function expressions (v- or i-branch), only one arbitrary directed version of every labelled graph needs to be found and analysed. All other cases can be derived by allowing for positive and negative transconductance values.
- The number of graphs to be considered is largely reduced by postponing the addition of v-branches. This is possible since ideal VCCSs have zero v-branch current, so that KCL graphs can be constructed without taking into account the v-branches.
- The v-branches are added in a later stage in a systematic automatic way by means of a MAPLE program. All possible transactors with two VCCSs are generated in this way. The transmission parameters of the resulting transactors have been evaluated systematically, and are presented in Appendix A.

Transactors with One VCCS

- Five transactors with a non-floating source are possible: a series and parallel conductance, a transconductor, and approximations of a current follower and voltage follower. The latter three circuits can be implemented with the three familiar single-device amplifier configurations CS, CG and CD.
- The transmission parameters of the transactors can assume a very restricted number of non-zero values: ±1/g for parameter B, ±g for parameter C, and 1 for parameter A and D. A second VCCS is needed to implement other voltage or current transfer ratios.

Transactors with Two VCCSs

- All desired 9 transactors with a non-floating input can readily be implemented.
- The cases with low port impedances can be approximated by using large transconductance values.
- A restricted number of transactors with a floating input is possible: the transactors with either infinite or accurate port impedances.
- The resulting transmission parameters are either determined by a transconductance (in case of 1/B and C) or by a ratio of transconductances (in case of A and D). The transconductance terms that occur are either the primary VCCS transconductance g_P (g_a or g_b), or combinations of them: the sum g_Σ or difference g_Δ (parallel or anti-parallel VCCS connection), or the product g_Π divided by g_Σ or g_Δ (series or anti-series VCCS connection).

Value and Control Range of Transmission Parameters

- The value of 1/B and C is determined by practical realisable MOST-VCCS transconductance values, and can typically be chosen in the range from 10^{-9} S to 10^{-1} S. Transmission parameters A and D are typically chosen between 1:100 and 100:1.
- The control ranges of the transmission parameter 1/B and C are equal for g_P and g_Σ, but much larger for g_Δ. Since the difference can be made arbitrarily small, this renders a theoretically infinite control range.
- The control range of the A and D transmission parameters (inverse of voltage gain and current gain) is again maximal for the terms with g_Δ. Furthermore the control range of a ratio of two primary VCCS transconductances is larger than for cases involving g_Σ.

4

Application Examples I

4.1 Introduction

The previous chapters have dealt with the requirements for linear transactors and the possibilities to implement these using VCCSs. This chapter tries to demonstrate the usefulness of the results of chapter 2 and 3, by some application examples.

In section 4.2, the relation between VCCS graphs and transistor level circuit implementations is considered. Next, examples of implementations of often used transactors like the transconductor, current amplifier, transresistance amplifier and voltage amplifier are discussed in the sections 4.3 through 4.3.4. It will be shown how different transistor level implementations of a transactor with certain specified transmission parameters can be found in a systematic way.

Thereafter, a more complex design example will be presented in section 4.4: a variable gain amplifier stage with an well-defined input impedance. It shows a design procedure from specification to possible circuit implementations, and compares the performance of the resulting possibilities.

4.2 Transistor Level Implementations of VCCS Graphs

We will now look at transistor level implementations of VCCS transactor graphs. The interconnection and orientation of the v- and i- branch of a VCCS play an important role in this matter. Figure 4-1 illustrates this point. From the figure we see that in cases without any connection between the v- and i-branch, a VCCS with a separate floating input and output ports is necessary. This can be implemented by common source MOST pairs, either of the same or of different type. If one connection exists between the v- and i-branch, and the branches have the same orientation (both arrows pointing to or from the common node), a single MOST can be used (a PMOST or NMOST depending on the branch orientation). Alternatively, common source MOST pairs can be used. If the branches are connected at both ends, and also have the same orientation, then a simple resistor can be used, apart from single MOSTs or common source MOST pairs.

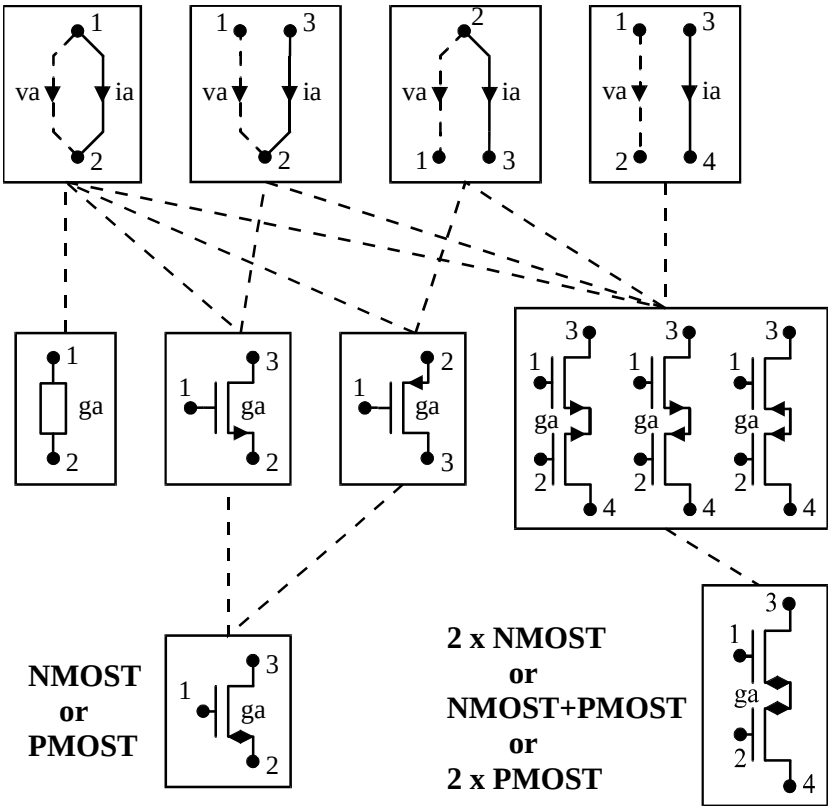


Figure 4-1: The relation between VCCS graphs and implementation options using MOS transistors and resistors. The interconnections between the v- and i-branches, and their relative orientation determine the possibilities. The lower MOST symbols with double arrows are used to indicate that there are multiple implementation possibilities (either NMOST or PMOST).

Because of its impact on the implementation possibilities, the direction of the branches will now be examined in more detail. In the previous chapter we introduced branch directions to link transmission parameter expressions in an unambiguous way to a (arbitrarily chosen) directed graph. The effect of v- or i-branch reversal on the transmission parameters is as follows (see also Table 3.12):

- Change the direction of the v- *or* i-branch: sign change of corresponding g-term.
- Change both the direction of the v- *and* i-branch of the same VCCS: no effect. This transformation changes an NMOST into a PMOST and vice versa.
- Change of the s- or l-branch orientation: no effect.

As a PMOST implementation can always be replaced by an NMOST by changing both the v- and i- orientation without changing the transmission parameter equations, it is useful to have a symbol available which represents *either a NMOST or a PMOST*. The symbol that will be used in this thesis for this purpose is a MOST symbol with double arrow, as shown at the bottom of Figure 4-1. As an example, Figure 4-2 shows the effect of several branch orientation changes on a certain transconductor graph found in Appendix A[1]. In graphs

[1] The circuits shown only comprise of the components relevant for the signal flow, while biasing sources are omitted. In chapter 6 we will consider biasing and large signal aspects.

Figure 4-2a the orientation of the v- and i-branches are different for VCCSa as well as VCCSb. Therefore common source pairs have to be used for both g_a and g_b.

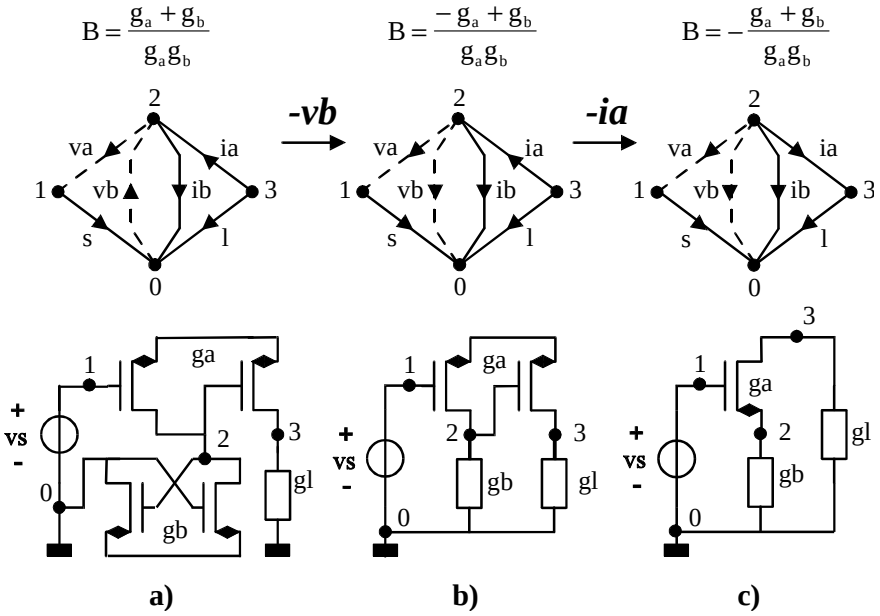


Figure 4-2: The effect of v_a and v_b sign changes on the transmission parameter expressions and the complexity of some possible circuit implementations (biasing not shown; some of these graphs may have stability problems).

By changing the direction of the v_b branch, v_b and i_b get the same orientation (Figure 4-2b). Since they are also in parallel, a simple resistor can be used. Alternatively, a diode-connected NMOST or PMOST can be used. If the direction of i_a is also changed (Figure 4-2c), VCCSa can be implemented by a single PMOST, and a familiar source degenerated MOST circuit results. Because of these direction changes, transmission parameter B changes, as indicated above the graphs in Figure 4-2. Note that changing the direction of v_b or i_a results in a sign change of respectively g_b and g_a in B.

In this place, a note on stability is appropriate. Although the graph analysis in Appendix A renders solutions for the node voltages, it is not guaranteed that the solutions are stable. It only means that there exists a set of node voltages for which all Kirchhoff and element relations are satisfied. However, many of the possible branch orientations render negative impedances, because of positive feedback loops. Therefore a careful stability consideration is important. By inspection of the graphs, the occurrence of a negative impedance can easily be recognised by qualitative reasoning. This can be done as follows: select a v-branch of a VCCS, and suppose for instance that only the voltage at the v+ node increases. This results in an increase of the current in the i-branch of the same VCCS. If this results in a current flow directed to the v+ node, a negative impedance exists. For the v- node similar reasoning holds. Applying this method to Figure 4-2a, shows that both VCCSa and VCCSb introduce a negative impedance, while in Figure 4-2b only VCCSa does so. Case Figure 4-2c has positive node impedances.

4.3 Implementations of Frequently Used Transactors

We will now look at implementation examples of frequently used transactors: the transconductor, current amplifier, transresistance amplifier and voltage amplifier. The considerations from the previous section will be taken into account during the selection of graphs from Appendix A in the rest of this chapter. Unless otherwise stated, *the branch orientations will be chosen such that only positive node impedances occur*. Furthermore, the *simplest possible implementations will be shown*.

4.3.1 Transconductors

As the generating elements used to implement transactors are VCCSs, it is no big surprise that transconductors can be implemented. From Appendix A we see that there are 9 floating input graphs and 28 non-floating input graphs with non-zero B. However, for 30 of them only one of the transconductances g_a or g_b occurs in the expression for B, although two VCCSs are present in the graph. A closer view at these cases shows that the VCCS corresponding to the "disappeared" transconductance, often have an "auxiliary" function, e.g. as a current-follower (cascode), or as a unity gain voltage buffer. This can be useful, e.g. to increase the output impedance or bandwidth of an actual transconductor transistor circuit. However, from a functional point of view assuming idealised VCCSs, these transactors are equivalent to a single VCCS. On the other hand, transconductors with both g_a and g_b in the B-expressions behave different from a single VCCS. Their transconductance control-range can for instance be significantly larger by current subtraction or their linearity can be improved (to be discussed in chapter 6). Since these cases are especially attractive from an application point of view, we will now investigate them further. From Appendix A we find that there are 2 floating input graphs with both g_a and g_b in the B-expression, as depicted in Figure 4-3.

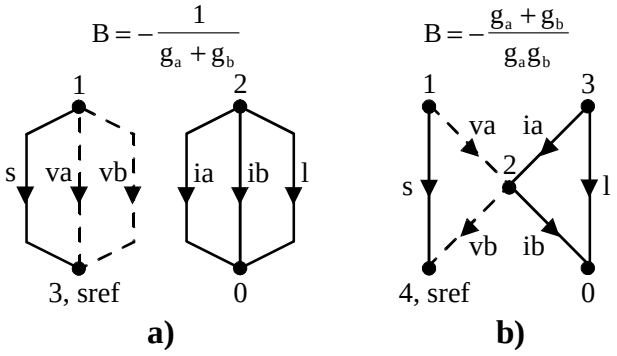


Figure 4-3: The 2 graphs of transconductors with a floating input and B depending on both g_a and g_b.

Looking at these graphs we see that they can be interpreted as a parallel-parallel connection of two VCCS input (v) and output (i) ports (Figure 4-3a) and a series-series connection (Figure 4-3b). The corresponding B-expressions are given above the graphs, and are independent of the common voltage of the source.

Figure 4-4 shows the graphs of transconductors without a floating input. Now there are 4 series-series connected VCCS graphs (a-d) and one with a parallel-parallel arrangement (e).

In fact these graphs have the same subgraphs as Figure 4-3, but they are joined at different nodes or have an extra joined node.

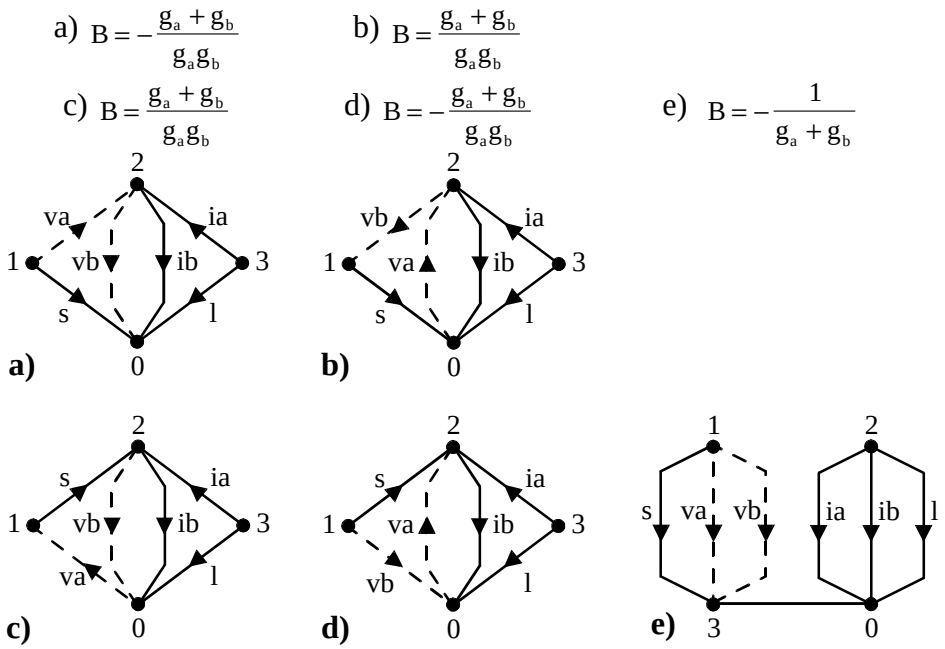


Figure 4-4: The 5 different graphs of transconductors with a non-floating input for which B depends on both g_a and g_b.

Looking at the parallel-parallel connected VCCSs of Figure 4-3a, we see that no common v- and i-branch nodes exist. Therefore common source pairs must be used, for example as shown in Figure 4-5a.

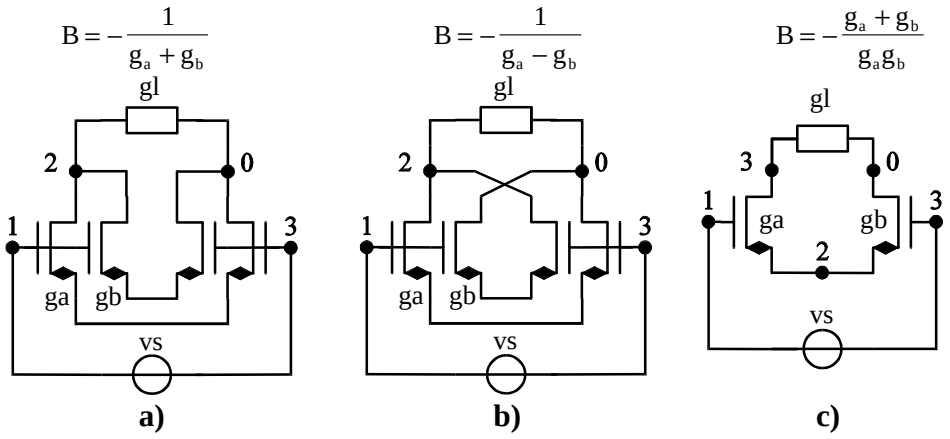


Figure 4-5: Examples of circuit implementations of the floating input graphs of Figure 4-3: a) and b) correspond to Figure 4-3a and c) to Figure 4-3b.

These transistor arrangements are well known from literature as simple differential pairs often implemented using one type of transistors. In a complementary MOST pair implementation they are used in Opamps as a class AB stage [e.g. 155] and in the transconductors of Park et al [47] and Seevinck et al [50], with different ways of implementing the required biasing (see also chapter 6 and 8). Note that the differential pairs are in parallel, so that their transconductances add up. This is not true for a cross-coupled version shown in Figure 4-5b, in which the difference of the transconductance g_a

and g_b determines the transconductance (this configuration results from changing the orientation of branch i_b, which can be done without introducing a negative impedance). This arrangement is well-known as a multiplier [139], and is also used for AGC applications [122]. Figure 4-5c, shows the series-series combination of two VCCSs in its simplest form: the differential pair.

In contrast to the cases discussed above, the non-floating input graphs have a source branch which is connected to the rest of the graph. Although this limits the application possibilities to some (often acceptable) extend, it simplifies the circuit implementation, because of the extra connection. Figure 4-6 shows examples of simple implementations of the 5 graphs of Figure 4-4 (the captions a-e correspond to those of Figure 4-4). One of the source-nodes is arbitrarily grounded. Except for case c, all VCCSs can be implemented by a single MOST or even a resistor. Again, some of these structures are well-known from literature. Figure 4-6a is well-known as a source-degenerated MOST which is sometimes used as a single ended V-I converter.

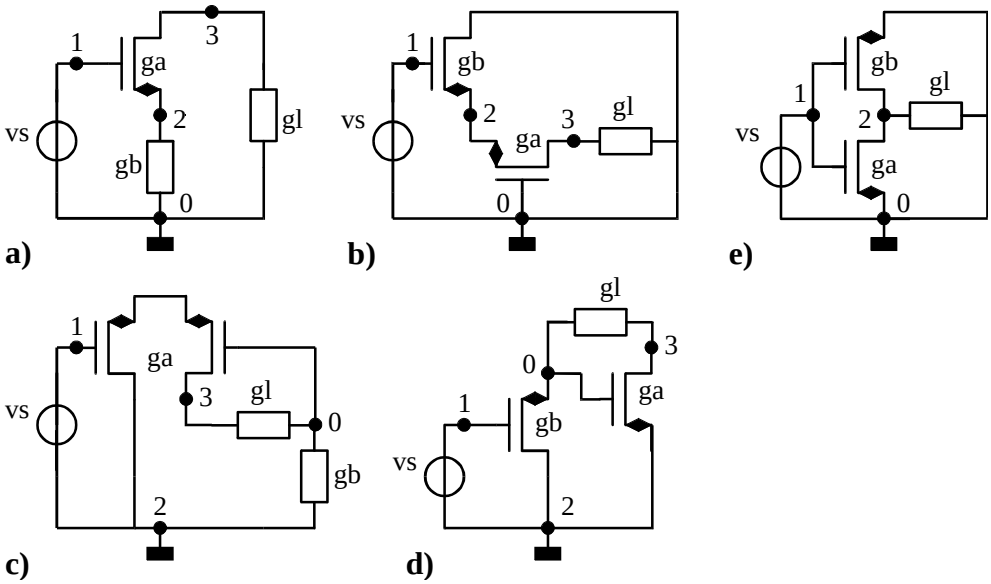


Figure 4-6: Examples of circuit implementations of the 5 graphs of Figure 4-4 (captions a-e correspond with those of Figure 4-4).

The source-follower and common-gate combination of Figure 4-6b is useful in feedback amplifiers [21]. The circuit of Figure 4-6e is well-known as an inverter and has been used as a V-I converter in VHF G_m-C filters [56]. On the other hand, the circuits of Figure 4-6c and Figure 4-6d were not previously encountered by the author. They are peculiar in the sense that they have a non-grounded load g_l, which has a well-defined voltage at node 0, because of its connection to VCCSb. For $g_a = g_b$, half of the source signal is present at this node. Furthermore, for ideal transconductors, the impedance seen looking from node 0 into the g_a and g_b current branch is equal for $g_a = g_b$, regardless of g_l. These circuits might be useful as transconductor stages that have to process signals outside the supply rails.

4.3.2 Current Amplifiers

Current mirrors are often used in integrated circuits, and can be considered as current amplifiers with a fixed gain, defined by a geometric ratio. On the other hand, in some cases current amplifiers with an electronically variable gain can be useful. We will now examine the possibilities to implement such circuits using VCCSs.

An ideal current amplifier should have non-zero current gain, zero input impedance and infinite output impedance. In terms of transmission parameters, D should be non-zero, and A, B and C zero. From Appendix A we see that there are only cases with D=1, that satisfy these conditions. These current followers will be discussed in the next sub-section. If we want to implement gains other than 1, we can resort to the approximations given in Table 3.7. The desired behaviour can be approximated for $B \ll D \cdot Z_s$ (large transconductance values for the VCCS) with the BD case. In practice, this condition is often satisfied, since a current mirror or amplifier is often driven by circuits with a high output impedance. Furthermore, a close look at Table 3.9 shows that there are two other possibilities: case AD and ABD. In both cases the limit for the output resistance for $Z_s \to \infty$ is infinity. Unfortunately, all AD cases have both A and D equal to 1, so that this will not be examined further.

Graph	va	vb	A	B	D ≈1/Ai for Zs→∞	Zin (A·Zl + B)/D
(s//i)(i//l)(fl. source) Figure 4-7	v_{13}	v_{13}	0	$-\frac{1}{g_b}$	$-\frac{g_a}{g_b}$	$\frac{1}{g_a}$
s+i+(i//l) Figure 4-8a	v_{10}	v_{10}	0	$\frac{1}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$\frac{1}{g_a}$
s//i//(i+l) Figure 4-8b	v_{10}	v_{01}	0	$\frac{1}{g_b}$	$\frac{g_a+g_b}{g_b}$	$\frac{1}{g_a+g_b}$
(s//i)(i//l) v_{sref}= 0 Figure 4-8c	v_{10}	v_{10}	0	$-\frac{1}{g_b}$	$-\frac{g_a}{g_b}$	$\frac{1}{g_a}$
s+i+(i//l) Figure 4-9a	v_{21}	v_{21}	1	$\frac{1}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$\frac{1}{g_a}\left((g_a+g_b)Z_l+1\right)$
s//i//(i+l) Figure 4-9b	v_{12}	v_{21}	1	$\frac{1}{g_b}$	$\frac{g_a+g_b}{g_b}$	$\frac{1}{g_a+g_b}\left(g_bZ_l+1\right)$
(s//i)(i//l) v_{sref}=0 Figure 4-9c	v_{12}	v_{21}	1	$\frac{1}{g_b}$	$\frac{g_a}{g_b}$	$\frac{1}{g_a}\left(g_bZ_l+1\right)$

Table 4-1: The 4 BD graphs and 3 ABD graphs, suitable for current amplifiers ($Z_{out} \to \infty$ for $Z_s \to \infty$).

Now we will take a closer look at the BD and ABD graphs, starting with the first. From Appendix A we find that 1 floating input BD graph and 23 non-floating input graphs exist. From the 24 cases, 15 have only 1 degree of freedom, with a non-inverting current gain of 1. For gains other than 1, we need the cases for which D is determined by a ratio of transconductance values. The 4 BD cases satisfying this condition are shown in Table 4-1, together with their input impedance expression. For the ABD case we find 3 non-floating input graphs satisfying the mentioned conditions. These are added at the end of table. From

the table we see that both gains larger and smaller than 1 are possible, inverting and non-inverting. The BD circuits have an input impedance that depends only on transconductance values, whereas it also depends on Z_l in the ABD cases. If Z_l is larger than $1/g_a$ and/or $1/g_b$ this contribution becomes significant.

The floating input BD graph implementation is shown in Figure 4-7. The implementation with one type of MOSTs is useful for implementing electronically variable current gain as in the current gain cell proposed in [61]. The circuit implementation with complementary MOST pairs is useful if a floating current source is needed, e.g. to bias a PMOS mirror connected to VDD and an NMOST mirror, connected to VSS, with the same current. Additionally this allows for electronic control of g_a and g_b, and thus of the gain.

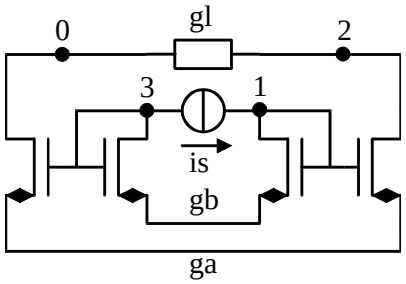


Figure 4-7: Floating input BD graph implementations suitable as current amplifiers.

The implementations of the non-floating input current amplifiers are shown in Figure 4-8.

B	$\frac{1}{g_a + g_b}$	$\frac{1}{g_b}$	$-\frac{1}{g_b}$
D	$\frac{g_a}{g_a + g_b}$	$\frac{g_a + g_b}{g_b}$	$-\frac{g_a}{g_b}$

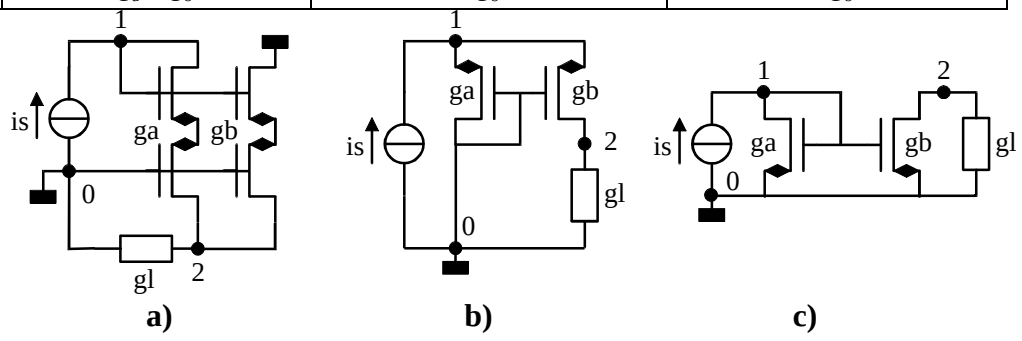


Figure 4-8: Non-floating input graph implementations of current amplifiers with a gain that is larger than 1 (a), smaller than 1 (b), or arbitrary (c).

Figure 4-8a is a non-inverting amplifier, with a minimum gain of 1. Figure 4-8b is also non-inverting, but has a gain lower than 1. It is sometimes used in circuits as a current splitter. Finally Figure 4-8c is recognised as the simple Widlar current mirror. It has an "arbitrary" gain in the sense that it can both be smaller and larger than 1.

Implementations for the ABD current amplifier graphs (all with a non-floating input) are shown in Figure 4-9. In all cases the voltage changes across the load are directly reflected to the input, because A=1. Again a non-inverting current amplifier with a minimum gain of 1 is found (Figure 4-9a) and a current splitter (Figure 4-9b) and arbitrary gain amplifier (Figure 4-9c).

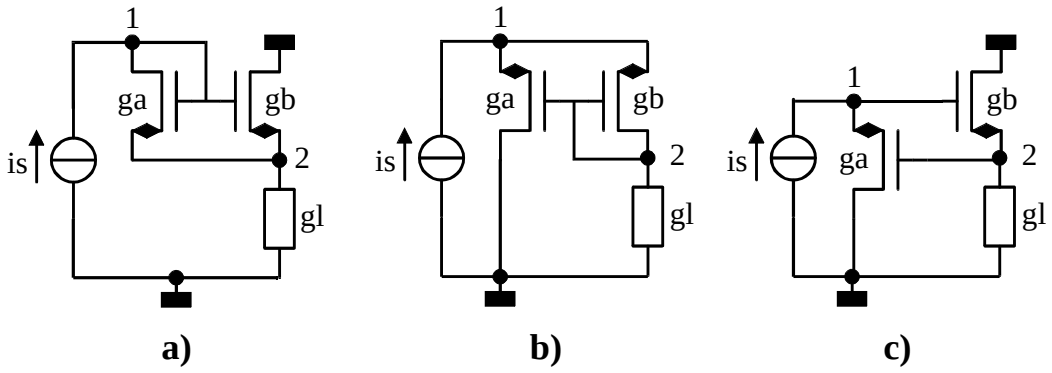


Figure 4-9: ABD graph current amplifier with a gain which is either larger than 1 (a), smaller than 1, or arbitrary.

In the above discussed example, we find a useful approximation of the desired behaviour (only a non-zero D) if certain additional conditions are satisfied (e.g. Z_s sufficiently high). However, even more approximation possibilities exist, e.g. case BCD and ABCD. In principle these can all be useful, depending on the specific boundary conditions of the design problem (Z_s, Z_l and the required transactance value). Since we already found quite some implementation possibilities for current amplifiers we will not discuss this further for this case, but we will in the section 4.3.3.

Current Followers (D=1)

It was already mentioned that it is possible to implement a current follower with current-gain equal to 1, by means of D graphs. In Appendix A we see that these possibilities all relate to graph (s+i+l)(i). These cases have in common that the i_b branch is an open branch, with zero current. As a result v_b must be zero, since g_b has a finite value. In fact, VCCSb implements a nullor: a combination of a nullator with zero voltage and current, and a norator, which enforces this condition. Figure 4-10a shows the different cases in one combined graph (nodes $i_{b,ref}$ and $v_{a,ref}$ can be connected to an arbitrary node). Figure 4-10b shows the corresponding nullor circuit representation: the nullator is connected between node 1 and 0, while the norator is connected between node 3 and $i_{b,ref}$ The norator controls v_a in such a way that the input voltage $v_{10}=v_b$ of the current follower remains zero. Since the current in branch v_b is also zero, the complete source current is transferred to the load, by means of VCCSa.

There are quite some different possibilities to implement the current follower, since both node $v_{a,ref}$ and $i_{b,ref}$ can be connected to any of the nodes 0,1 or 2, without changing the transmission parameters (see Appendix A). Table 4-2 lists the 9 different combinations possibilities, while Figure 4-11 shows the simplest circuit implementations (the number between brackets indicate the node number for $v_{a,ref}$ and $i_{b,ref}$). The implementations are such, that overall a negative feedback loop exists around the nullor, VCCSb. The latter two columns in Table 4-2 indicate whether the v- and i-branch of VCCSa and VCCSb share a node and whether the branch orientations are equal. If the branch orientations are such, that a single MOST implementation is possible, this is indicated with a ++. This occurs, for example for both VCCSs, in case (1,0). Hence, the circuit can be implemented using 2 single MOSTs. It is well-known as an active cascode stage and used for gain boosting [36,65,74].

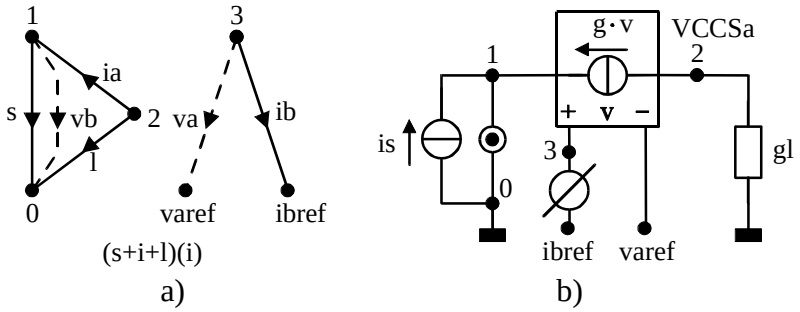


Figure 4-10: a) Combined (s+i+l)(i) graph of current followers. b) The corresponding equivalent circuit. VCCSb acts as a nullor, that enforces zero input voltage, while VCCSa transfers the source current to the load.

If a branch reversal is needed to create a implementation option with a single MOST, this is indicated with a +. Such a branch reversal requires a simultaneous reversal of one branch of the other VCCS, to maintain negative feedback. As a result, in some cases two implementations exist: one with VCCSa implemented with a single MOST and VCCSb with a common source pair, and vice versa. Case (1,1) is an example of such a case.

$v_{a,ref}$ node	$i_{b,ref}$ node	common node v_a and i_a?	common node v_b and i_b?
0	0	-	++
0	1	-	+
0	2	-	-
1	0	++	++
1	1	++	+
1	2	++	-
2	0	+	++
2	1	+	+
2	2	+	-

Table 4-2: The 9 different combinations of nodes to which $v_{a,ref}$ and $i_{b,ref}$ can be connected in the graphs of Figure 4-10. The two rightmost columns indicate whether the VCCSs have a common v- and i-branch node and equal branch orientation: - (no), ++ (yes), + (yes, after branch reversal).

From a transmission parameter point of view, all the current followers in Figure 4-11 are equivalent. However, note that the graphs only reflect ideal VCCSs, with infinite input and output impedance. For low frequencies this condition can usually be approximated quite well, and the current of VCCSb can be neglected. However, for higher frequencies, inevitable parasitic capacitances constitute additional current paths, changing the KCL relations. Since these paths differ from circuit to circuit, different configurations result in different transmission properties. Similar observations can be made for other performance aspects. As a last example we mention the influence of tolerances in DC-biasing sources. If node $i_{b,ref}$ is connected to node 1 or 2 (cases (...,1) and (...,2)), such tolerances in the current through VCCSb directly influence the load current. This disadvantage does not occur if i_b is connected to ground. Which of the topologies is most fitted for an actual design, depends

on the combination of specifications. The topologies generated in this thesis can serve as a design database of possible implementation options.

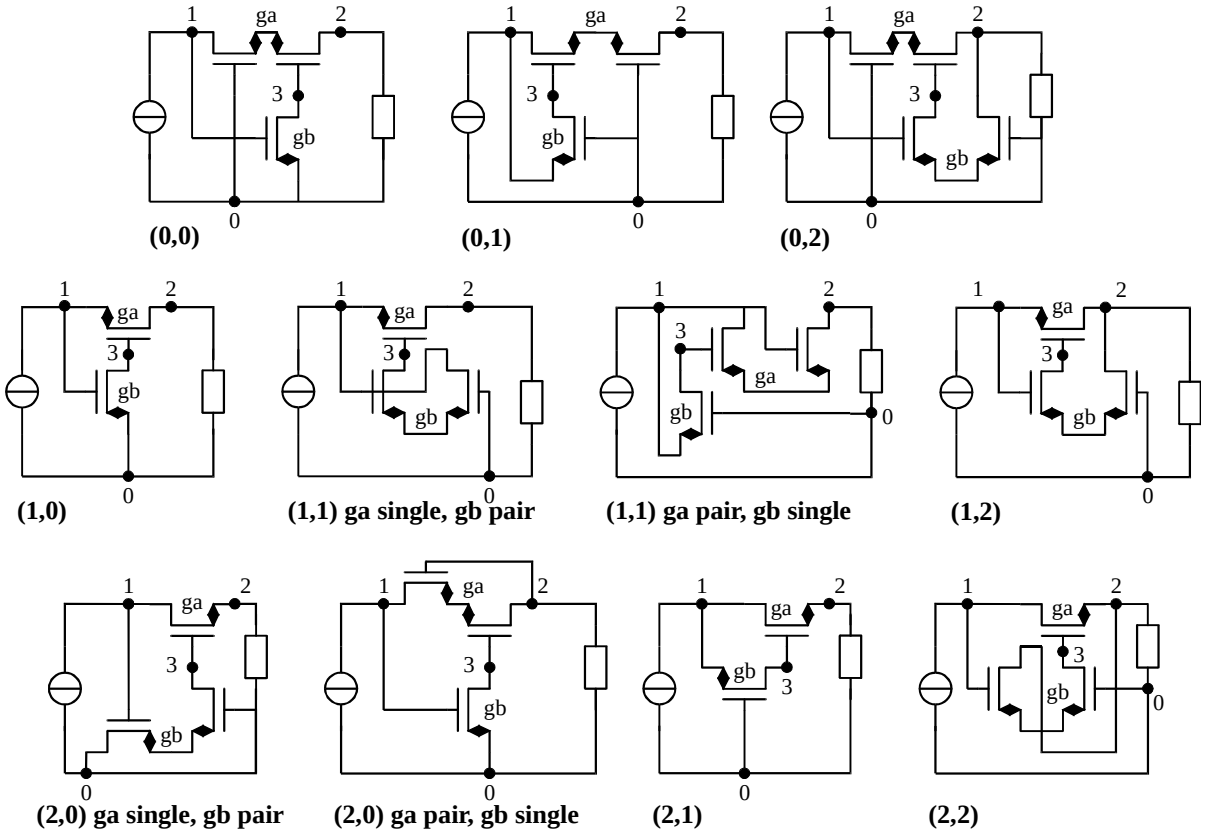


Figure 4-11: Current follower circuits implementing the (s+i+l)(i) graph of Figure 4-10. The numbers between brackets indicate the nodes of $v_{a,ref}$ and $i_{b,ref}$.

4.3.3 Transresistance Amplifiers

An ideal transresistance amplifier should have zero input and output impedance, i.e. only a non-zero C transmission parameter. A look at Appendix A and Table 3.9 and 3.10 shows that a direct implementation is not available, but that case BC can approximate the desired behaviour. The input impedance, output impedance and transimpedance become:

$$Z_{in} = \frac{B}{C \cdot Z_l} \quad (4.1a) \qquad Z_{out} = \frac{B}{C \cdot Z_s} \quad (4.1b) \qquad Z_t = \frac{1}{C + B/(Z_s Z_l)} \quad (4.1c)$$

For $B << C \cdot Z_s \cdot Z_l$, the equations in (4.1) get their ideal values 0, 0 and 1/C. Table 4-3 lists the BC graphs found in Appendix A: one floating VCCS graph and one non-floating one. Transmission parameter C is fixed by transconductance g_a, and made equal to $1/Z_t$. Parameter B is equal to g_b, and can be used to make Z_{in} and Z_{out} sufficiently small for the application. The simplest circuit implementations corresponding to the BC graphs from Table 4-3 are depicted in Figure 4-12. If these transresistance amplifiers don't satisfy the requirements, we would like to look at alternatives. Apart from case BC, there are other possibilities with non-zero C that can sometimes be used as a transresistance amplifier: cases ABC, ACD, BCD and ABCD. In Appendix A further data on these graphs can be found.

Graph	v_a	v_b	A	B	C	D
(s//i)(i//l) (floating input) Figure 4-3a	v_{20}	v_{31}	0	$\frac{1}{g_b}$	g_a	0
(s//i)(i//l) Figure 4-3b, c	v_{20}	v_{01}	0	$\frac{1}{g_b}$	g_a	0

Table 4-3: BC graphs implementing a transresistance amplifier for $B<<C\cdot Z_s\cdot Z_l$.

We will not discuss all these cases in detail, but restrict ourselves to some remarks on additional conditions that have to be met to approximate a transresistance amplifier. For cases with non-zero A, Z_t and Z_{out} get their desired values for $A<<C\cdot Z_s$. For high source resistance values this is easily obtained. The influence of A on Z_{in}, also depends on Z_l, but has a limit $Z_{in} = A/C$ for high values of Z_l. For cases with non-zero D, Z_t and Z_{in} get their desired values for $D<<C\cdot Z_l$. Now, the influence of D on Z_{out} depends on Z_s, but has a limit $Z_{out} = A/C$ for high values of Z_s.

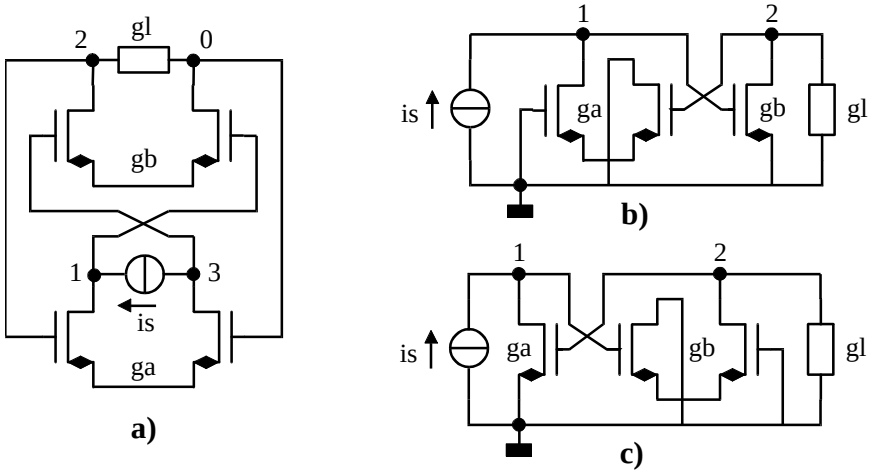


Figure 4-12: Transresistance amplifiers implementing the BC graphs of Table 4-3.

4.3.4 Voltage Amplifiers

An ideal voltage amplifier should have an infinite input impedance and zero output impedance, i.e. only non-zero A. Voltage gain 1/A should either have a well-determined value or be electronically variable. From Appendix A we find that only cases with A=1 occur. These voltage followers will be treated separately in the next subsection. Case AB approximates a voltage amplifier for $B<<A\cdot Z_l$. If we restrict ourselves to cases with a gain that can be chosen unequal to 1, one floating input graph and 3 non-floating input graphs are found, as shown in Table 4-4.

Figure 4-13 shows simple implementations of the 4 cases in Table 4-4. Again other approximation are possible, as discussed at the end of section 4.3.3, but these will not be discussed here for compactness.

Graph	v_a	v_b	A ($\approx 1/A_v$ for $B \ll A \cdot Z_l$)	B	$Z_{out} = B/A$
(s)(i//i//l) (floating input) Figure 4-13a	v_{20}	v_{31}	$\frac{g_a}{g_b}$	$\frac{1}{g_b}$	$\frac{1}{g_a}$
(s)(i//i//l) Figure 4-13b	v_{10}	v_{20}	$-\frac{g_b}{g_a}$	$-\frac{1}{g_a}$	$\frac{1}{g_b}$
(s)(i//i//l) Figure 4-13c	v_{01}	v_{21}	$\frac{g_b}{g_a + g_b}$	$\frac{1}{g_a + g_b}$	$\frac{1}{g_b}$
(s)(i//i//l) Figure 4-13d	v_{20}	v_{21}	$\frac{g_a + g_b}{g_b}$	$\frac{1}{g_b}$	$\frac{1}{g_a + g_b}$

Table 4-4: The AB graphs approximating an ideal voltage amplifier for $B \ll A \cdot Z_l$ with a gain that can be different from 1.

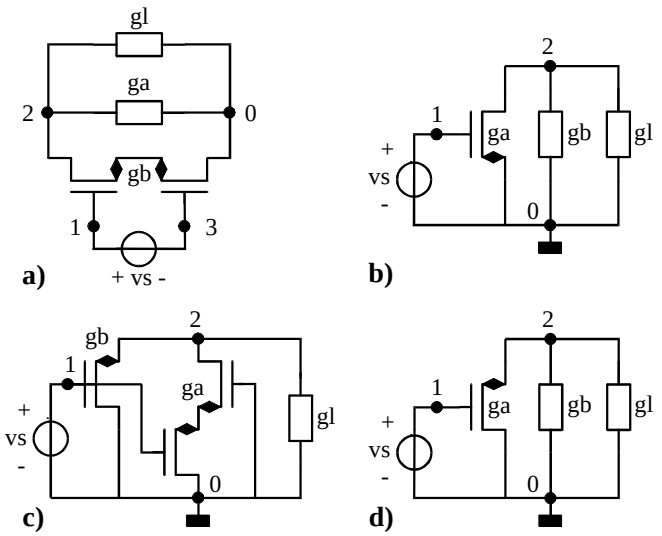


Figure 4-13: Simplest implementations of the voltage amplifiers listed in Table 4-4.

Voltage Followers (A=1)

In the previous section we already mentioned the possibility to implement a voltage follower with a gain equal to 1, by means of A graphs. In Appendix A we see that these possibilities all relate to graph (s)(i//l)(i). As for the current follower graphs, these cases have in common that the i_b-branch has zero current, so that v_b is also zero. Figure 4-14 shows a combined graph and the corresponding nullor circuit representation: now the nullator is connected directly between the input node 1 and the output node 2. The norator, connected between node 3 and $i_{b,ref}$, changes the load voltage such that $v_{12} = v_b$ becomes zero, i.e. the load voltage becomes equal to the source voltage. As for the current follower, there are quite some different possibilities to implement voltage followers, since both node $v_{a,ref}$ and $i_{b,ref}$ can be connected to any of the nodes 0,1 or 2, without changing the transmission parameters (see Appendix A).

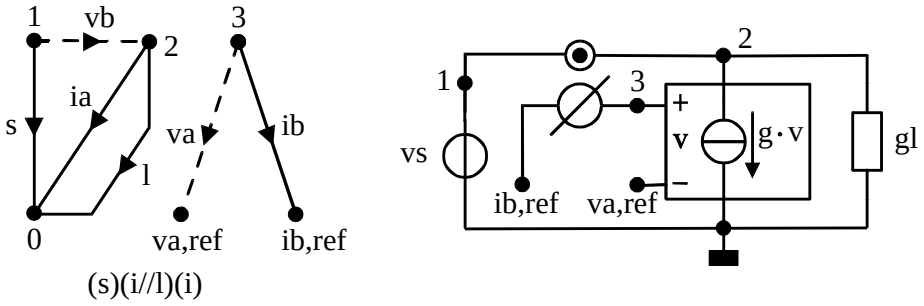


Figure 4-14: The voltage follower graph (s)(i//l)(i) in which VCCSb acts as a nullor, that forces the load voltage equal to the source voltage.

Table 4-5 lists the 9 different combinations possibilities, while Figure 4-15 shows the 11 most simple circuit implementations (the number between brackets indicate the node number for $v_{a,ref}$ and $i_{b,ref}$). The implementations are such, that overall a negative feedback loop exists around the nullor, VCCSb. Since the generation of circuits proceeds along the same lines as for the current follower, they will not be discussed in more detail.

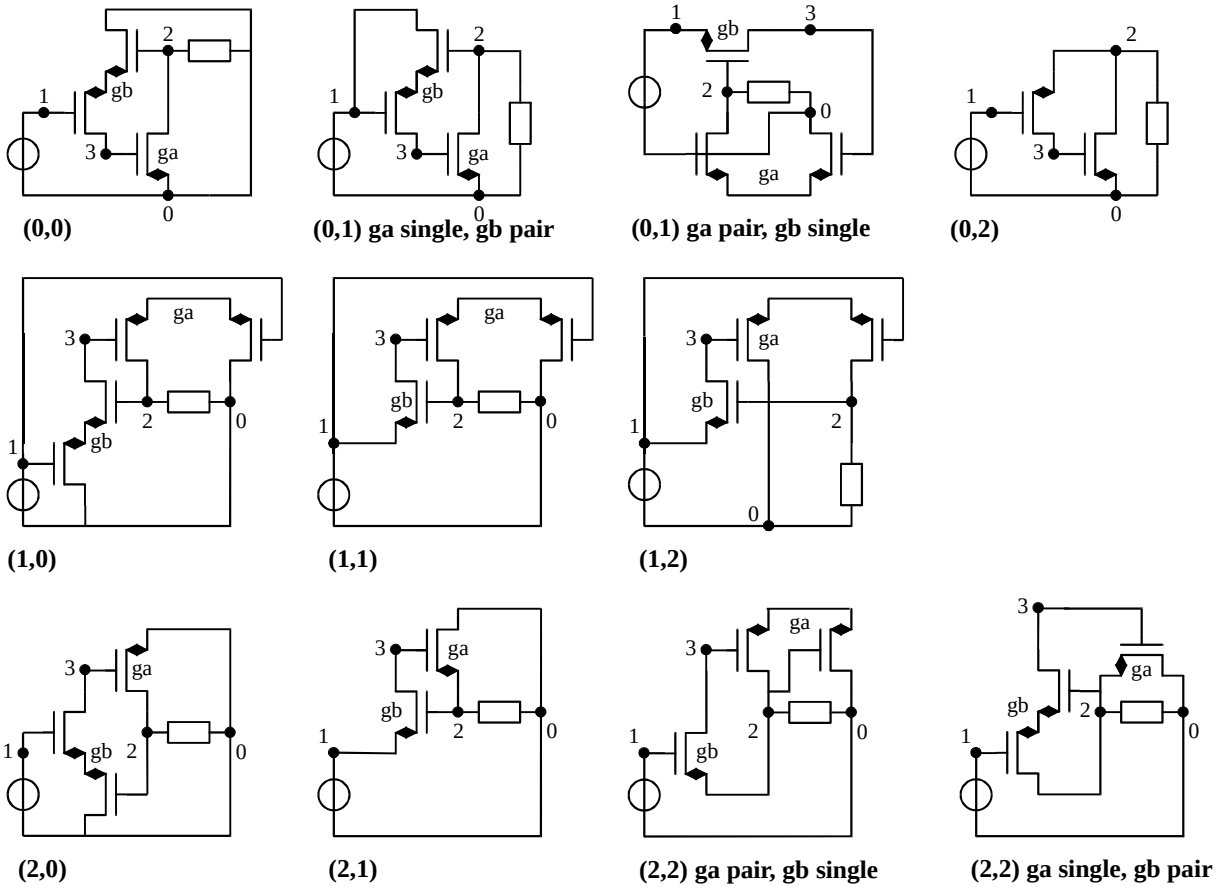


Figure 4-15: 11 Different voltage follower circuits implementing the (s)(i//l)(i) graph of Figure 4-14. The node pairs between bracket indicate the nodes to $v_{a,ref}$ and $i_{b,ref}$ are connected.

$v_{a,ref}$ node	$i_{b,ref}$ node	common node v_a and i_a?	common node v_b and i_b?
0	0	++	-
0	1	++	+
0	2	++	++
1	0	-	-
1	1	-	+
1	2	-	++
2	0	+	-
2	1	+	+
2	2	+	++

Table 4-5: The 9 different combinations of nodes to which $v_{a,ref}$ and $i_{b,ref}$ can be connected in the graphs of Figure 4-14. The two rightmost columns indicate whether the VCCSs have a common v- and i-branch node and equal branch orientation: - (no), ++ (yes), + (yes, after branch reversal).

4.4 Design Case Study: AGC-Stage: Part I

In the previous section we generated different transistor level circuit implementations of commonly used transactors. The discussion was confined to their first order functional behaviour. We will now go into more detail for a specific application example, and also consider DC-biasing aspects, and performance criteria. An AGC amplifier for a television receiver set will be used as an example.

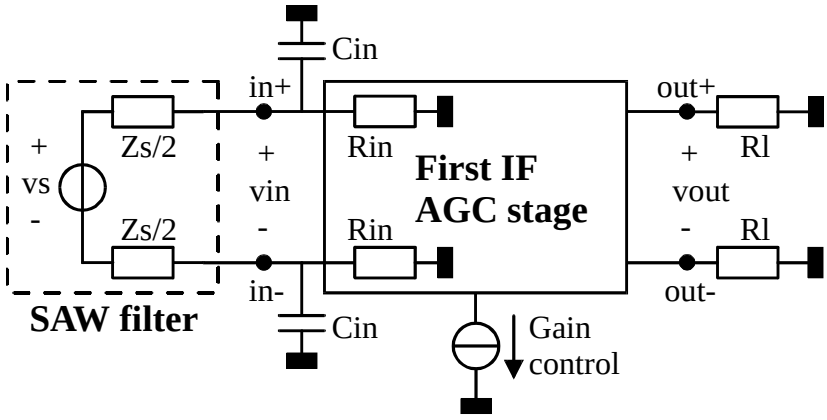


Figure 4-16: The AGC stage to be designed and its source, the SAW filter, and load.

In a broadcasting television receiver, much of the amplification and filtering is performed in an intermediate frequency (IF) band around 38.9 MHz. The IF-filter is commonly implemented using a Surface Acoustic Wave filter (SAW-filter). The subsequent IF-amplifier has to amplify the bandfiltered IF-signal, with a gain that depends on the amplitude of the received antenna signal. The SAW-filter has a transfer function that is specified for a certain load impedance, which is determined by the input impedance of the AGC amplifier, as shown in Figure 4-16. Therefore, this impedance should have a well-defined value, consisting of a resistance and a capacitance in parallel, with values specified in the SAW filter datasheet. For an optimal transfer function the two SAW filter outputs

should "see" equal impedances to ground "looking into" node in+ and in-. Typical values for the required input resistance R_{in} and capacitance C_{in} are 1 Kohm and 5 pF respectively. The capacitive part is determined by two capacitors and printed circuit board interconnection capacitances.

Specification	Value	Description
Z_s	2 Kohm // 2 pF	Output Impedance of the SAW filter
R_{in}	1 Kohm	Input Resistance
C_{in}	< 5 pF	Total Input Capacitance
A_0	0-66dB (1 - 2000)	Total AGC Gain-Range
v_s	200 mV_{rms}/A_0	Open Output Amplitude of the SAW filter
BW	>40 MHz	Bandwidth
$v_{n,eq}$	<6 $nV/\sqrt{Hz}$	Equivalent Input Noise
HD3	<-60 dB	Third Order Harmonic Distortion

Table 4-6: Specifications of a typical IF AGC-amplifier for television.

The object of the design procedure that follows now is to design an AGC amplifier stage that has an electronically variable gain and a well-defined resistive input impedance. The specifications in Table 4-6 will be used as a design goal. The design procedure consists of the following subsequent actions:

1. Analyse the design requirements to determine which transactors can potentially fulfil the requirements in terms of Z_{in}, Z_{out} and A_t (see Table 2.1 of chapter 2).
2. Use chapter 3, Table 3.9 and 3.10 to find out which combination(s) of transmission parameters satisfy the requirements.
3. Use Appendix A, to find VCCS graphs that implement these parameters.
4. Calculate the required transmission parameter values and the resulting transconductance values needed to meet the circuit specifications.
5. Select candidates for the VCCS implementation based on the need for floating VCCS ports and the achievable transconductance values of Table 3.7.
6. Size and bias the VCCS circuits to implement the required transconductances.
7. Evaluate the performance of the resulting VCCS circuits and select the circuits most fitted for the particular application.

The above mentioned design steps will be discussed in the following paragraphs.

4.4.1 Design Requirements

An important requirement for the AGC stage is its input impedance. From the specification of the SAW filter, a grounded input impedance is required. This means that circuits with a non-floating input can be used, which can be implemented easier. In order to create two equal impedances to ground as required, two of these transactors are needed.

As mentioned in the previous paragraph, a capacitor at the input can easily fix the capacitive part of the impedance. This requires that the transactor has less input

capacitance than typically 2pF, which is usually no problem. To implement the resistive part R_{in}, a passive resistor across the input can be used. Alternatively, this can be established by means of a VCCS with feedback. The latter solution allows for electronic adjustment of the impedance matching. If the demand on the impedance matching accuracy is more stringent than the fabrication tolerance of the resistors, this may be necessary. For SAW filters this is usually not the case. However, the active input impedance implementations will be examined because of their potentially lower noise [21].

Apart from impedance matching, the AGC amplifier stage should have electronically variable gain. This is possible by varying the transconductance of the VCCSs in the transactor. The output impedance of the transactor can be high, low or well-defined, depending on the stage following the impedance matching stage, which is still free to choose. To compare these different possibilities, a load resistor will be assumed at the output, so that a voltage transfer function exists for all transactors.

4.4.2 Suitable Transmission Parameter Combinations

If the input resistance is fixed by a separate resistor, the input impedance of the subsequent transactor should be very high. Case A, B and AB satisfy these conditions. Alternatively, with reference to Table 3.9, we find 8 cases with possibilities to fix the input impedance.

Non-zero parameters				Zin	Condition to keep Zin constant
A			D	$\frac{A}{D}\cdot Z_l$	$A \propto D$
	B	C		$\frac{B}{C\cdot Z_l}$	$B \propto C\,Z_l$
	B		D	$\frac{B}{D}$	$B \propto D$
A	B	C		$\frac{A\cdot Z_l + B}{C\cdot Z_l}$	$(A\cdot Z_l + B) \propto C\cdot Z_l$
A	B		D	$\frac{A\cdot Z_l + B}{D}$	$(A\cdot Z_l + B) \propto D$
A		C	D	$\frac{A\cdot Z_l}{C\cdot Z_l + D}$	$A\cdot Z_l \propto (C\cdot Z_l + D)$
	B	C	D	$\frac{B}{C\cdot Z_l + D}$	$B \propto (C\cdot Z_l + D)$
A	B	C	D	$\frac{A\cdot Z_l + B}{C\cdot Z_l + D}$	$(A\cdot Z_l + B) \propto (C\cdot Z_l + D)$ *e.g.* $A\cdot D = B\cdot C$

Table 4-7: The different possibilities to implement a well-determined input impedance and the additional required conditions to keep the impedance constant. The cases in italics are selected for further examinations.

These cases are shown in Table 4-7. In order to vary the gain of the AGC stage, at least one of the transmission parameters must be varied. As seen in Table 4-7 this also affects the

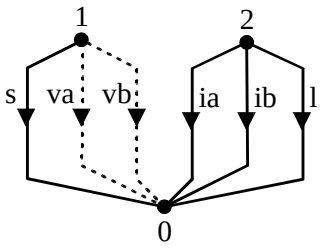
input impedance. To keep this impedance constant as required, the other transmission parameters should vary in accordance with the condition in the last column of Table 4-7. The transmission parameters of transconductance based transactors are determined by transconductances ($B \propto 1/g$, $C \propto g$) or ratios of them (A or D). As a result, the conditions $A \propto D$, $B \propto C \cdot Z_l$, $B \propto D$ and $A \cdot D = B \cdot C$ can be implemented fairly easy, by simultaneous proportional or inverse proportional tuning of two transconductance values. The other 4 conditions also depend on Z_l, and it is not obvious how to implement them. Therefore we will only consider the case AD, BD, BC and ABCD.

4.4.3 Suitable VCCS Graphs

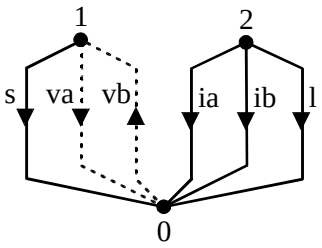
Our next step is to look for VCCS graphs that render the desired non-zero transmission parameter combinations selected in the previous paragraph. In Appendix A, the graphs and corresponding formulas can be found (Table 3.13 gives an overview). However, an additional constraint can be used to restricts the number of possibilities: according to the specification in Table 4-6 the gain should be variable and larger than 1. Looking at the voltage-gain expression eqn. 2.15, it is easily verified that this can only be true if $A<1$, $B<Z_l$, $C<1/Z_s$ and $D<Z_l/Z_s$ are satisfied. As a result, the cases A and AD are not suitable ($A=1$ and $D=1$). Furthermore several other graphs can be rejected on this basis.

Figure 4-17 and Table 4-8 list the cases that remain. The first 8 rows in the table relate to passive resistor impedance matching. In the 6 other cases, the VCCSs implement the impedance. Looking at the conditions for a constant input impedance, it appears that the BC case requires a constant product $g_a g_a Z_l$. This is possible by choosing R_l equal to $1/g_a$ (use a self-connected VCCS as load), which is done.

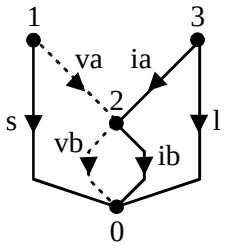
The branch orientations in the graphs have been chosen in such a way that negative feedback loops occur. In principle, it is also possible to use configurations with (limited) positive feedback, provided that the total impedance at every node remains positive (stability condition). Since this complicates the design, and in order to limit the number of possibilities in this example, this option is not considered further here. Another aspect that is not considered, is the difference in performance between transconductors with one degree of freedom in the B equation: $B=1/g_a$ or $B=1/g_b$. Since all these cases have the same transmission parameter expression, their behaviour is equal in first order approximation. Therefore it is sufficient to consider only one of them in an early phase of the design process. The first case in Table 4-8 covers them (g_a and g_b are in parallel and can be combined to one single VCCS, provided that they are implemented with the same type of VCCS, at equal biasing conditions).



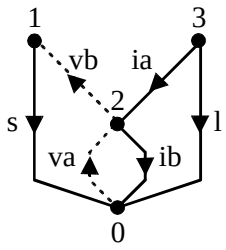
a) (s)(i//i//l) [v10,v10]



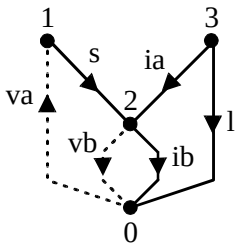
b) (s)(i//i//l) [v10,v01]



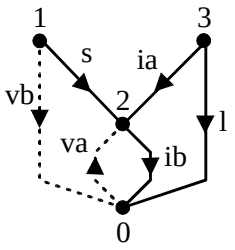
c) (s)(i+i+l) [v12,v20]



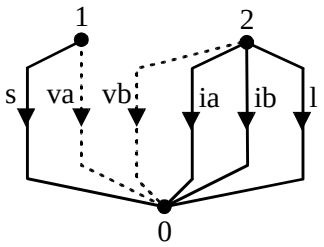
d) (s)(i+i+l) [v02,v21]



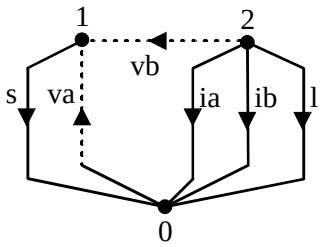
e) (s)(i+i+l) [v01,v20,v2]



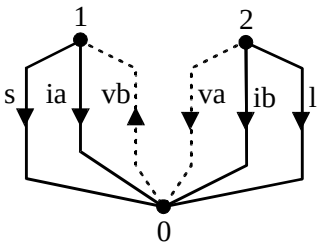
f) (s)(i+i+l) [v02,v10,v2]



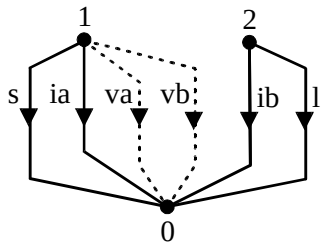
g) (s)(i//i//l) [v10,v20]



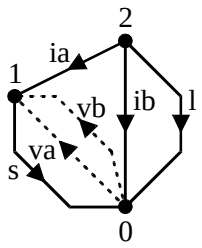
h) (s)(i//i//l) [v01,v21]



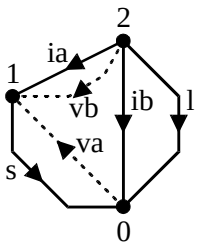
i) (s//i)(i//l) [v20,v01]



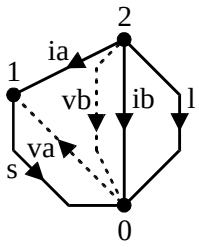
j) (s//i)(i//l) [v10,v10]



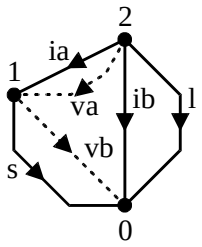
k) s+i+(i//l) [v01,v01]



l) s+i+(i//l) [v01,v21]



m) s+i+(i//l) [v01,v20]



n) s+i+(i//l) [v21,v10]

Figure 4-17: The different graphs of VCCS circuits that are potentially suitable for the AGC amplifier (the voltages between brackets indicate v_a, v_b and v_{sref}).

	Graph	A	B	C	D	A_v	Z_{in}
a	(s)(i//i//l) $[v_{10},v_{10}]$	0	$-\frac{1}{g_a+g_b}$	0	0	$-\frac{1}{2}(g_a+g_b)R_l$	$R_{in}=R_s$ (added)
b	(s)(i//i//l) $[v_{10},v_{01}]$	0	$-\frac{1}{g_a-g_b}$	0	0	$-\frac{1}{2}(g_a-g_b)R_l$	$R_{in}=R_s$ (added)
c	(s)(i+i+l) $[v_{12},v_{20}]$	0	$-\frac{g_a+g_b}{g_ag_b}$	0	0	$-\frac{1}{2}\frac{g_ag_b}{g_a+g_b}R_l$	R_{in} (added)
d	(s)(i+i+l) $[v_{02},v_{21}]$	0	$\frac{g_a+g_b}{g_ag_b}$	0	0	$\frac{1}{2}\frac{g_ag_b}{g_a+g_b}R_l$	R_{in} (added)
e	(s)(i+i+l) $[v_{01},v_{20},v_2]$	0	$\frac{g_a+g_b}{g_ag_b}$	0	0	$\frac{1}{2}\frac{g_ag_b}{g_a+g_b}R_l$	R_{in} (added)
f	(s)(i+i+l) $[v_{02},v_{10},v_2]$	0	$-\frac{g_a+g_b}{g_ag_b}$	0	0	$-\frac{1}{2}\frac{g_ag_b}{g_a+g_b}R_l$	R_{in} (added)
g	(s)(i//i//l) $[v_{10},v_{20}]$	$-\frac{g_b}{g_a}$	$-\frac{1}{g_a}$	0	0	$-\frac{1}{2}\frac{g_a}{g_b}$	R_{in} (added)
h	(s)(i//i//l) $[v_{01},v_{21}]$	$\frac{g_b}{g_a+g_b}$	$\frac{1}{g_a+g_b}$	0	0	$\frac{1}{2}\frac{g_a+g_b}{g_b}$	R_{in} (added)
i	(s//i)(i//l) $[v_{20},v_{01}]$	0	$\frac{1}{g_b}$	g_a	0	$\frac{1}{2}\frac{g_b}{g_a}$	$\frac{1}{g_bg_aR_l}$ $(R_l=1/g_a)$
j	(s//i)(i//l) $[v_{10},v_{10}]$	0	$-\frac{1}{g_b}$	0	$-\frac{g_a}{g_b}$	$-\frac{1}{2}g_bR_l$	$\frac{1}{g_a}$
k	s+i+(i//l) $[v_{01},v_{01}]$	0	$\frac{1}{g_a+g_b}$	0	$\frac{g_a}{g_a+g_b}$	$\frac{1}{2}(g_a+g_b)R_l$	$\frac{1}{g_a}$
l	s+i+(i//l) $[v_{01},v_{21}]$	$\frac{g_b}{g_a+g_b}$	$\frac{1}{g_a+g_b}$	$\frac{g_ag_b}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$\frac{1}{2}(1+\frac{g_a}{g_b})$	$\frac{1}{g_a}$
m	s+i+(i//l) $[v_{01},v_{20}]$	$\frac{g_b}{g_a}$	$\frac{1}{g_a}$	g_b	1	$\frac{1}{2}\frac{g_a}{g_b}$	$\frac{1}{g_a}$
n	s+i+(i//l) $[v_{21},v_{10}]$	$\frac{g_a}{g_a-g_b}$	$\frac{1}{g_a-g_b}$	$\frac{g_ag_b}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$	$\frac{1}{2}(1-\frac{g_b}{g_a})$	$\frac{1}{g_b}$

Table 4-8: The 14 different graphs of VCCS circuits with well-defined input impedance and an electronically variable gain that can be larger than 1.

4.4.4 Choice of Transconductance Values

In the previous paragraph, we found 14 graphs that might be useful to implement the desired transactor. To find out which of them is most suited for a certain application, the most relevant performance criteria have to be evaluated. This can be done by analytical methods, yet it easily becomes cumbersome. On the other hand it can lead to analytical expressions for important performance criteria, which are a powerful design tool. We will return to this item in the next chapter. A quick way of getting an impression of the relative merits of different circuits, is by means of circuit simulation. However, since concrete circuit implementations including component values are needed for simulation, we first

need to choose transconductance values. Important aspects in this matter are the impedance level and gain. Since we are especially interested in a comparison of different topologies, we will first try to keep as many things equal as is possible. In a later design phase, adaptations can be made to fit the specification of the circuit. The following assumptions will be used as a starting point:

- R_{in} should be 1 Kohm and is sometimes implemented using a transconductance of 1 mS. Hence, the transconductance tuning range should include this value, at least in some transactors. To cope with production tolerances, it is useful to choose 1 mS as the centre of the tuning range.
- From chapter 3 and practical experiments, it is known that a tuning range of 1:4 is often achievable. With 1 mS as a centre value, the transconductance range becomes 0.5-2 mS. This range will be used for all VCCS implementations to make them as equal as possible, unless there are urgent reasons not to do so.

Using these assumptions, and the equations in Table 4-8, the gain range was calculated, taking into account the design goal $R_{in}=R_s=1$ Kohm. R_s is equal to half of the resistive part of Z_s, since we consider one circuit half of the AGC amplifier. R_l was chosen such that the minimum gain becomes 1. The results are shown in Table 4-9.

Looking at the table we see that there are significant differences in the functional behaviour of the transactors. Although the VCCSs have the same transconductance control range, their gain control range is very different. In 8 cases, the gain control range is 1:4 as for the transconductance. For case b, signal subtraction occurs, which theoretically makes it possible to reach zero gain (infinite gain control range). A moderately high gain range of about 1:8 was chosen for this case. Other cases with a large gain control range are case g (1:16) and h (1:8.5) and n (1:5.5), due to the presence of a ratio of transconductances that can both be tuned. For case i, which has a similar gain expression, this is not possible, because g_b must also fix R_{in}. This problem also occurs for the remaining cases k and l, and results to an even lower gain range of 1:2 and 1:2.5.

4.4.5 VCCS Implementation

Now we have chosen transconductance values we can look at a transistor level implementation of the VCCSs in the transactor. From Table 4-9 we see that the required transconductance lies in the range of 0.06 mS to 2 mS. According to Table 3.7, the weak inversion MOST has a transconductance which is far too low. MOSTs in strong inversion, either in the triode or saturated region remain as candidates. A saturated MOST transconductor is more easily implemented, because it does not require circuits to buffer the input voltage to the triode MOST or keep V_{DS} constant. This is especially true for rather high frequencies (40 MHz), where it becomes hard to implement sufficient loop gain. Therefore a saturated MOST transconductor will be chosen.

	Graph	g_a (mS)	g_b (mS)	R_l (ohm)	A_v Range ($R_{in}=R_s=Z_s/2=1$Kohm)
a	(s)(i//i//l) [v_{10},v_{10}]	0.5 → 2.0	0.5 → 2.0	2K	-1.0 → -4.0
b	(s)(i//i//l) [v_{10},v_{01}]	2.0	1.8 → 0.45	10K	-1.0 → -7.8
c	(s)(i+i+l) [v_{12},v_{20}]	0.5 → 2.0	0.5 → 2.0	8K	-1.0 → -4.0
d	(s)(i+i+l) [v_{02},v_{21}]	0.5 → 2.0	0.5 → 2.0	8K	1.0 → 4.0
e	(s)(i+i+l) [v_{01},v_{20},v_2]	0.5 → 2.0	0.5 → 2.0	8K	1.0 → 4.0
f	(s)(i+i+l) [v_{02},v_{10},v_2]	0.5 → 2.0	0.5 → 2.0	8K	-1.0 → -4.0
g	(s)(i//i//l) [v_{10},v_{20}]	0.5 → 2.0	0.25 → 0.06	-	-1.0 → -16.0
h	(s)(i//i//l) [v_{01},v_{21}]	0.5 → 2.0	0.5 → 0.13	-	1.0 → 8.5
i	(s//i)(i//l) [v_{20},v_{01}]	0.5 → 0.125	1.0	0.5 → 0.125 (=1/g_a)	1 → 4
j	(s//i)(i//l) [v_{10},v_{10}]	1	0.5 → 2.0	4K	-1.0 → -4.0
k	s+i+(i//l) [v_{01},v_{01}]	1	0.5 → 2.0	1.33K	1.0 → 2.0
l	s+i+(i//l) [v_{01},v_{21}]	1	1.0 → 0.25	-	1.0 → 2.5
m	s+i+(i//l) [v_{01},v_{20}]	1	0.5 → 0.13	-	1.0 → 4.0
n	s+i+(i//l) [v_{21},v_{10}]	1	0.33 → 0.08	-	-1.0 → -5.5

Table 4-9: Transconductance values for the transactors of Table 4-8, chosen to fix R_{in} at 1 Kohm and maximise the gain control range (see text).

Some of the graphs require a VCCS with floating input and output port, which can for instance be implemented with a differential pair with current source as shown in Figure 4-18. Although it is possible in many graphs to implement the transactors with a single transistor, all VCCSs were implemented by such differential pairs. By doing so, the differences in performance are primarily related to differences in topology, and not to the implementation of the VCCS. This seems to be a fair and clear starting point for a comparison of different circuits. An additional advantage is that the DC biasing of the circuits becomes easy, since there are no level shift problems (All VCCSs have zero input voltage in their biasing point). Using the NMOST differential pair implementation, the VCCS graphs of Table 4-8 can be implemented by the circuit shown in Figure 4-20. In this figure, the biasing sources are omitted for simplicity.

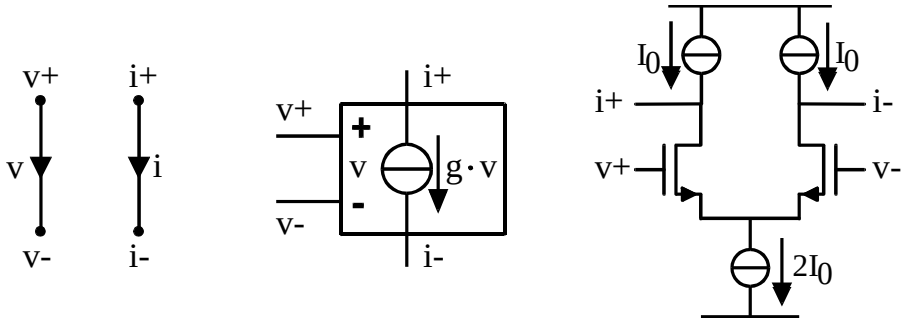


Figure 4-18: VCCS implementation used for the transactors of Table 4-8: a differential pair with current sources.

4.4.6 Sizing and Biasing of the VCCS Circuit

To be able to simulate the circuits of Figure 4-20, we need to choose W/L values for the MOSTs and bias values for the current sources. The transconductance for a differential pair is approximately given by:

$$g = \frac{i}{v} = \sqrt{\frac{W}{2L}\mu_n C_{ox} I_0} \tag{4.2}$$

From eqn. 4.2 we see that a combination of W/L and I_0 has to be chosen. In order to ensure strong inversion behaviour, we want to choose V_{GS} well above V_T. On the other hand, high V_{GS} values result in voltage headroom problems and high currents (the current increases roughly with the square of V_{GT}). As a compromise V_{GT} was chosen in the range of 0.1 to 1 Volt, which results in the desired nominal transconductance range from 0.5 to 2.0 mS for 150/1.5 transistors in a 1 µCMOS process, used in simulations (see also Table 3-1). If needed, the transconductance range was scaled by means of W/L, while keeping the V_{GT} range fixed. To give the transconductors a sufficiently high output conductance, composite MOSTs as shown in Figure 4-19 were used [114], with the upper MOSTs 2 times wider than the lower ones. This results in an output resistance which is roughly 4 times higher than for a single MOST. For simplicity of comparison, bulks were connected to sources.

Parameter	Value	Unit
$W/L_1 \approx W/L_{equivalent}$	150/1.5	-
W/L_2	300/1.5	-
g	$0.5 \rightarrow 2.0$	mS
$2I_0$	$0.25 \rightarrow 5.3$	mA
V_{GT}	$0.1 \rightarrow 1$	V

Table 4-10: Some important properties of the differential pairs used in simulating the transactors of Figure 4-20 (1 µCMOS process).

The performance of the circuit of Figure 4-20 was simulated using PSPICE with MOS level 3 model parameters for a 1µCMOS process. The geometry of the MOS transistors and some important properties of the differential pair are listed in Table 4-10. Since we are primarily interested in the behaviour of the MOSTs handling the signal, all biasing current sources were idealised. In this way an estimate for the best achievable performance of the circuits is found. Figure 4-20 shows a plot of g_m of the transconductor as a function of V_{in},

while V_{GT} for the MOSTs varies from 0.1V to 1V. The transconductance indeed roughly varies between 0.5 and 2 mS for a tail bias current between 0.2mA and 10.4mA.

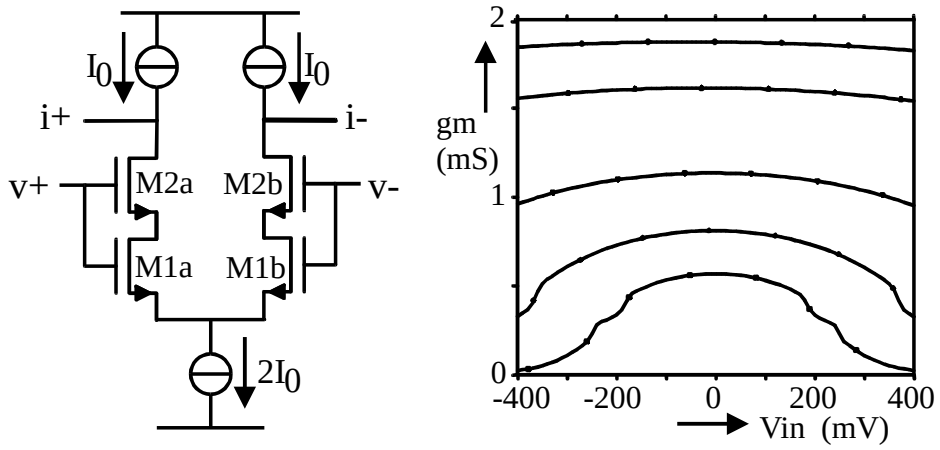


Figure 4-19: Actual transconductor circuit used and its simulated transconductance.

4.4.7 Performance Evaluation

Definition of a Common Gain Control Variable

To compare different AGC amplifier designs, it is convenient to define a common control variable for all cases. Since the range of effective gate-source voltages has been chosen equal for all designs, and as the transconductance is proportional to it, this is a meaningful common variable. Analogous to the definitions in chapter 3 for transconductance tuning range ($g_0/a_c < g < a_c g_0$) the following definitions will be used:

$$V_{GT} = V_{GT,nom}\left(a_c\right)^{pwr\cdot sgn} \quad \text{with} \quad -1 < pwr < 1 \quad \text{and} \quad sgn \in \{-1,0,+1\} \tag{4.3}$$

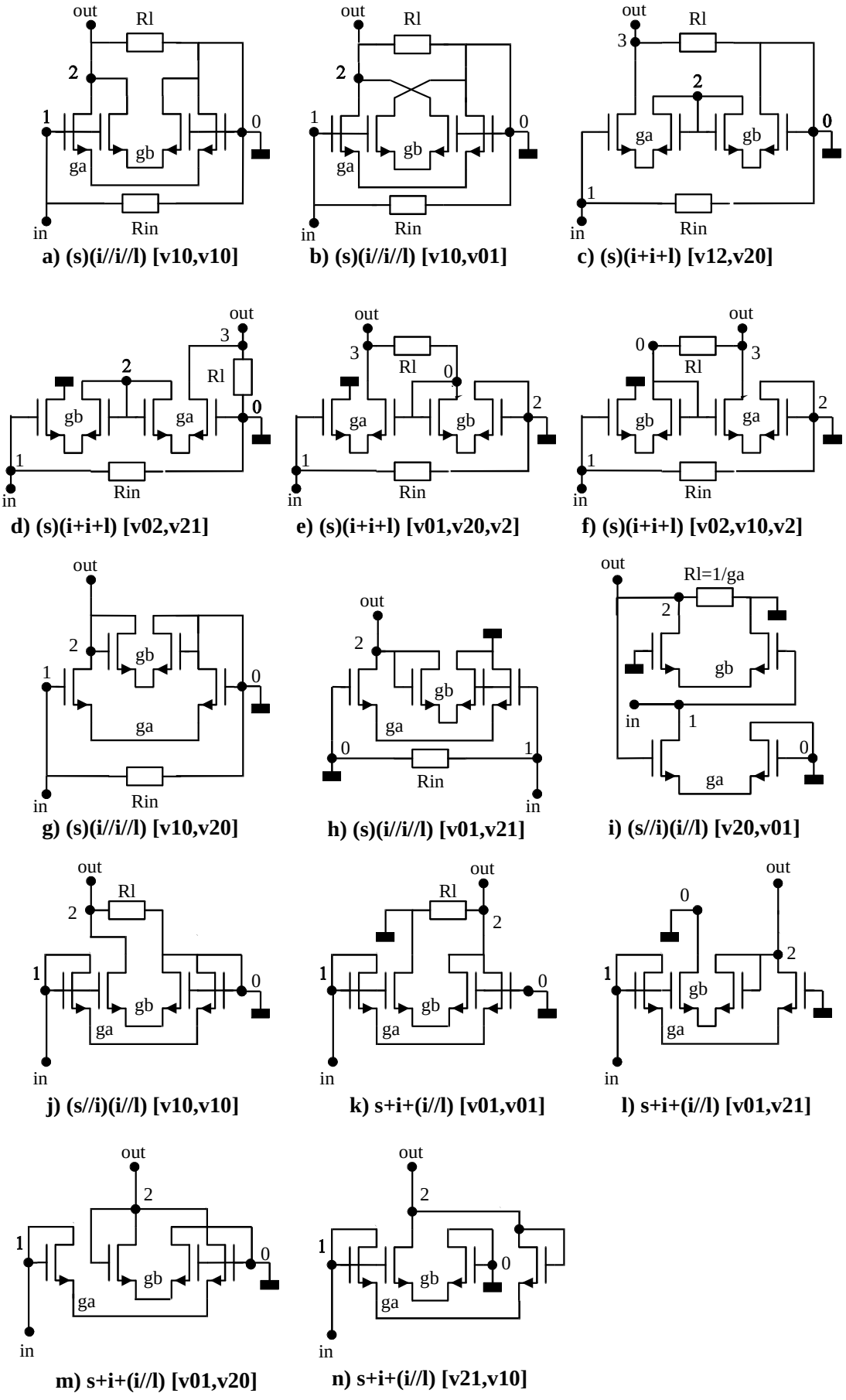
where $V_{GT,nom}$ is the nominal effective gate-source voltage V_{GT}, which is the geometric mean between its maximum and minimum.

$$V_{GT,nom} = \sqrt{V_{GT,max} \cdot V_{GT,min}} \tag{4.4}$$

By means of variable pwr, the effective gate-source voltage is swept between extreme values that are a_c times smaller and larger than $V_{GT,nom}$:

$$\frac{V_{GT,nom}}{a_c} < V_{GT} < a_c V_{GT,nom} \tag{4.5}$$

Finally variable sgn (sign) allows for increasing or decreasing V_{GT} as a function of pwr, in order to obtain a transactor gain that always increases with pwr (in some cases the gain is inversely proportional to transconductance). Furthermore, the transconductance can be fixed to its nominal value by means of sgn=0.



a) (s)(i//i//l) [v10,v10] **b) (s)(i//i//l) [v10,v01]** **c) (s)(i+i+l) [v12,v20]**

d) (s)(i+i+l) [v02,v21] **e) (s)(i+i+l) [v01,v20,v2]** **f) (s)(i+i+l) [v02,v10,v2]**

g) (s)(i//i//l) [v10,v20] **h) (s)(i//i//l) [v01,v21]** **i) (s//i)(i//l) [v20,v01]**

j) (s//i)(i//l) [v10,v10] **k) s+i+(i//l) [v01,v01]** **l) s+i+(i//l) [v01,v21]**

m) s+i+(i//l) [v01,v20] **n) s+i+(i//l) [v21,v10]**

Figure 4-20: Circuits implementing the graphs of Table 4-8, using differential pairs.

Comparison of Simulation Results

Using the parameters discussed in the previous paragraph, the transactors of Figure 4-20 were simulated, using the requirements of Table 4-6 as a starting point. The results are shown in Table 4-11 and Figure 4-21, and show respectively the gain, the equivalent input noise (in nV/√Hz, determined at 40 MHz), HD3 (in $^{0}/_{00}$), the bandwidth BW (in Megahertz) and the total bias current I_{SS} (in mA).

Case	$\|A_v\|$	$v_{n,eq}$ nV/√Hz	HD3 ($^{0}/_{00}$)	BW (MHz) (C_l=0.5pF)	I_{SS} (mA)
a	1.1→3.4	8.9→ 6.6	11.1→0.2	100→ 80	0.5 → 10.6
b	1.1→7.0	36→ 7.8	9.2→0.2	50 → 18	6.3 → 2.9
c	1.1→3.4	14.7→ 8.7	2.4→0.2	45 → 33	0.5→ 10.6
d	1.1→3.4	14.7→ 8.7	2.4→0.2	45 → 33	0.5→ 10.6
e	1.1→3.4	14.7→ 8.7	2.4→0.2	45 → 33	0.5→ 10.6
f	1.1→3.4	14.7→ 8.7	2.4→0.2	45 → 33	0.5→ 10.6
g	1.2→9.8	9.8→ 7.1	9.6→11.8	60 → 22	0.9→ 5.3
h	1.1→6.0	7.7→ 6.9	5.6→20.2	120 → 45	1.6→ 5.4
i	1.1→3.6	7.2→ 4.9	0.4→190	275 → 79	2.7→ 1.4
j	1.1→3.2	14.7→ 6.9	8.5→0.1	63 → 60	1.6→ 6.7
k	1.1→1.8	6.5→ 5.5	3.4→0.02	160 → 180	1.6→ 6.7
l	1.0→2.3	4.9→ 4.7	0.1→43	270 → 80	4.0 → 1.5
m	1.1→3.6	5.9→ 5.0	0.4→140	126→ 50	2.7 → 1.4
n	1.2→4.9	7.1→ 5.2	2.0→205	140 → 45	2.2 → 1.4

Table 4-11: Simulations results for the AGC stages of Figure 4-20, simulated with the parameters given in Table 4-10

The source resistance was 1 Kohm for all cases. HD3 was determined at a low frequency of 4MHz to assess a measure for non-linearity that does not depend on bandwidth limitations. For a voltage gain of one, the source amplitude was 280mV. Furthermore, the amplitude of the signal source was chosen inversely proportional to the gain A_0 (worst case situation; if cascaded stages are used, only the last one experiences this input swing). The bandwidth was determined for a capacitive load of 0.5 pF, roughly equal to the input capacitance of the MOSTs used in the differential pair.

A look at Table 4-11 and Figure 4-21 shows that there are considerable differences in the behaviour of different transactors, although they are all realised with the same or very similar differential pairs.

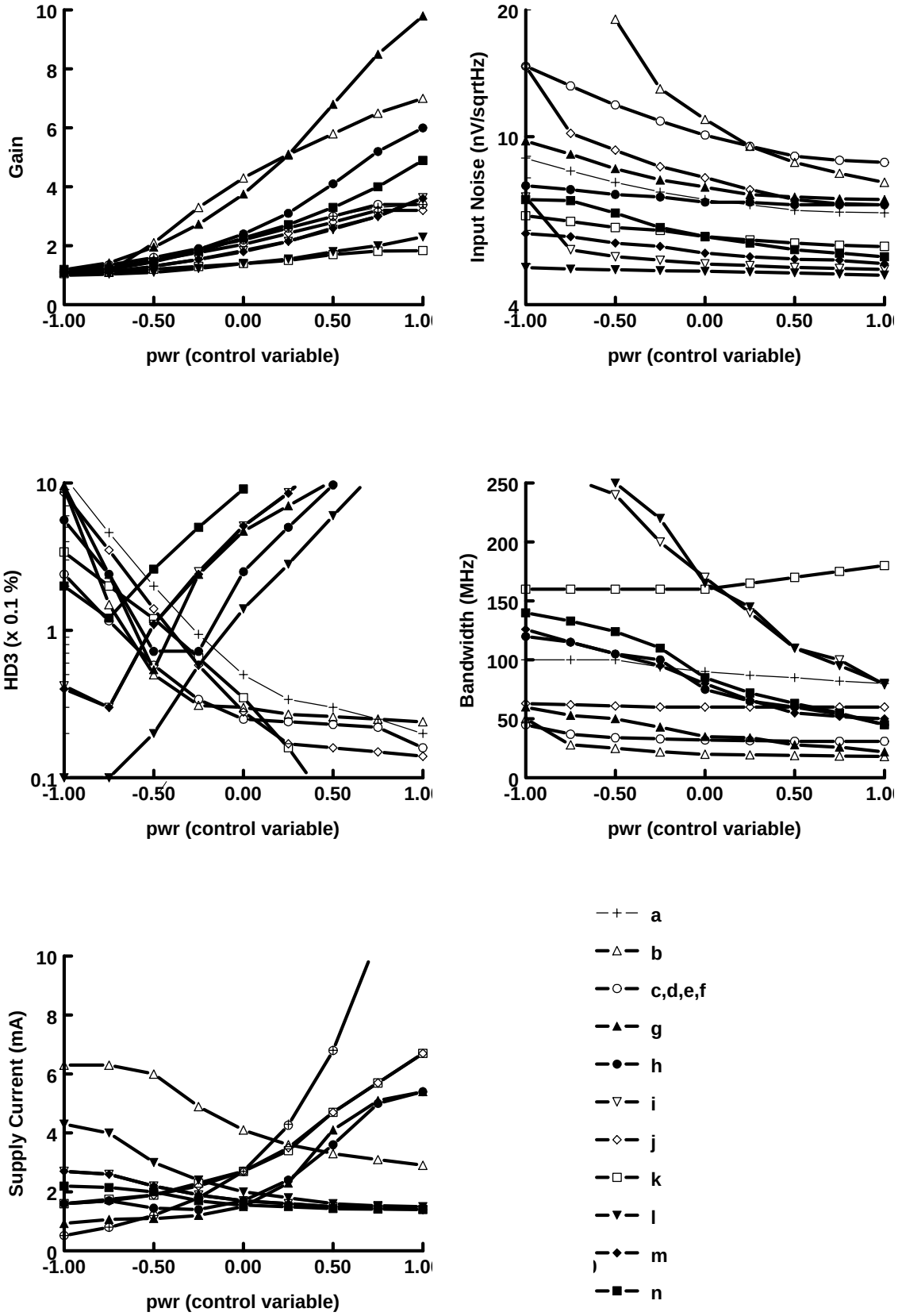


Figure 4-21: Simulation results for the circuits of Figure 4-20.

The following observations can be made:

- The simulation results for the gain are somewhat lower than the calculations results from Table 4-9. Differences are mainly due to output conductance influences, especially for high value of R_l. The gain range that can be achieved is very important, since it determines the number of stages that is required to implement the desired gain range of 66dB: it lies between 4 and 11 stages, depending on the gain range of the individual transactors. This number of stages has a large impact on the required bias current.
- The equivalent input noise varies from 5 to 9 nV/√Hz for high gain values. It is rather constant for some case (e.g. l), but increases substantially with decreasing gain for others: for case b it even increases with 650% due to the signal subtraction. Since the noise requirement of less than 6 nV/√Hz is specified at a gain of 1, only two transactors are good enough in this respect (case l, m). The others will need higher bias current and/or larger W/L ratios to decrease the noise.
- The HD3 specification of less than 0.1% is only satisfied over a part of the gain range, in most cases at high gain values. For low gains, and consequently larger input signal levels, HD3 is 3-11 times larger than the specification limit except for 3 cases (case i, l, m). However, these cases with a low HD3 at low gain, show a very drastic increase of HD3 at high gains. In order to meet the distortion specification, measures are needed. One possibility is the increase of bias current, which generally leads to lower distortion. However, the bias currents are already quite high, and do not leave much room for improvement. Probably alternative linearised VCCS implementations have to be considered.
- Although the desired bandwidth of 40MHz is not achieved in all cases, most of the circuits are good enough. In some cases the bandwidth is rather constant e.g. case c-f and j, while in others it varies strongly with gain, e.g. case i and l.
- The supply current ISS becomes as large a 10mA in some cases (e.g. a, c-f), but is significantly smaller in others (e.g. <3mA for case m). As the transconductance only increases with the square-root of the current, currents easily become large. Case g combines a very large gain range (1:10) with a moderate ISS of less than 5.4mA. This high gain is especially important since thus less cascaded stages are needed to achieve the desired gain range. Since the currents are quite large for IC applications, the gain range and current consumption deserve more attention.

Somewhat aside, some remarks can be made about case c through f. These cases have the same KCL graph, but different control voltages. This common origin is reflected in their performance: the achieved result are quite close. On the other hand, for smaller load capacitance values there is a significant difference in the bandwidth of the circuits: without Cload, case c has a bandwidth that decreases from 190 to 120 MHz with increasing gain, while case d-f show an increase from 140 to 160MHz. This illustrates that circuit details can significantly influence the high-frequency behaviour of a circuit. Thus it can be useful to generate many different possible implementations of a certain VCCS graph (e.g. as for the current and voltage followers), since minor implementation differences may result in

significant performance differences. On the other hand, many properties are equal, which shows promise for a generalised approach, in which groups of circuits are analysed in one run.

Evaluation of the Results

From the simulation results discussed above, it is clear that we are still far away from meeting the desired specs, especially with respect to noise and distortion. The question now arises: what can we do to improve the designs? In order to answer this question we would like to identify the main causes of noise and non-linearity, and change the topology and/or the design parameters to improve them. However, an improvement of one specification point will often come at the cost of a degradation elsewhere. Thus it is very likely that we have to deal with design trade-offs, e.g. between power and noise, or between gain-range and distortion. As a designer we would like be aware of them, and know how strong they are. Although one can get an impression by means of numerical simulations, it is rather hard and risky to base general conclusions and extrapolations on them. For this purpose, symbolic design equations are a more powerful means for analog designers. This is because they render insight in the dependence of performance aspects on design parameters. Thus many "what if" questions can be answered. Thus trade-offs between performance aspects become visible. On the other hand, it is often labour-intensive and cumbersome to produce such design equations. Nevertheless we will give it a try in the rest of this thesis, and look for possibilities for automation.

In the previous chapters we saw that there are more than 150 functional VCCS graphs, which can all be implemented in several ways. If we deal with all of them separately, the amount of analysis effort easily exceeds reasonable bounds. On the other hand we saw that there are only a limited number of different transconductance expressions occurring in transmission parameter equations. This suggests that there are only a limited number of really different cases. It will indeed appear in the next chapter that groups of graphs and circuits can be classified in classes with a lot of common properties. The number of required analysis calculations can thus be reduced largely. Therefore we will look more closely at fundamental differences between VCCS circuits in the next chapter.

4.5 Summary and Conclusions

In this chapter practical application examples were given, demonstrating the usefulness of the previous chapters. First, we examined the topological possibilities to implement often used transactors like transconductors, current amplifiers, transimpedance amplifiers and voltage amplifiers. Thereafter, a more detailed example of an impedance matching AGC amplifier stage was considered. The main results are listed below.

- It was shown that transistor level circuit topologies can be generated in a systematic way, starting from a functional description in terms of non-zero transmission parameters. First all potentially useful VCCS graphs are identified using Appendix A. Thereafter, transistor level implementations are generated, which are finally dimensioned and evaluated on relevant performance criteria. The fact that the approach is systematic makes it potentially suitable for computer aided circuit synthesis.

- All VCCS graphs can be implemented using MOST pairs. If the v- and i-branch of a VCCS in this graph have common nodes, and if the branches have the same orientation, VCCSs can also be implemented by a single MOST (one common node) or even by a simple resistor (two common nodes).
- Apart from many well-known circuits, like transconductors and current mirrors/amplifiers, also less familiar ones are found. Since all circuits with 2 VCCS are covered, all possible circuits up to a given complexity can in principle be found. Many of them are otherwise easily overlooked.
- A design procedure for an impedance matching AGC amplifier stage was discussed in detail. It shows that there are several different possibilities to implement the desired functionality with VCCSs. Furthermore, although very similar VCCS implementations were used, there are significant differences in performance. The analysis of such differences is the main subject of the rest of this thesis. Since the number of implementation possibilities easily becomes quite large, there is a clear need for a generalised approach. The next chapter will concentrate on this.

5

Classification of Circuits with Two VCCSs

5.1 Introduction

In chapter 3, all graphs of transactors with two VCCSs were generated, resulting in 145 graphs. Every graph can be realised in several different MOST circuits, as was shown in chapter 4. However, despite of the large number of realisation options, only a few different expressions for the transmission parameters were found (see Table 3.16). This suggests that there are only a few basically different ways of establishing a transmission parameter. The aim of this chapter is to unveil these different possibilities and classify them.

The classification of circuits is the process of dividing a group of circuits in subgroups, based on certain common properties. This helps to *create overview and insight* by clearly distinguishing different and common properties. Furthermore, since the circuits belonging to a given class *share* certain *properties*, they can often be *analysed in one run*. The present chapter will show that circuits with two VCCSs can fruitfully be classified based on *sets of two independent Kirchhoff relations amongst the VCCS variables* that are established in the circuits. It will appear that this classification largely simplifies the analysis of VCCS circuit performance. Moreover, it *renders insight* into different ways of exploiting VCCSs.

The outline of this chapter is as follows: section 5.2 starts with a discussion on the relation between transmission parameters and Kirchhoff relations for circuits with one VCCS. In section 5.3 circuits with two VCCSs are addressed. It will be shown that two independent relations amongst the VCCS variables are required to establish a unique value for a transmission parameter. Without additional components, these relations can only be Kirchhoff relations established by interconnections. In section 5.4 the different possibilities to impose two such relations are examined. Based on these possibilities 3 main classes of so-called 2VCCS circuits are defined. These 3 classes are subdivided in 14 subclasses. In section 5.5, the transfer functions for the classes are analysed. Finally, in section 5.6, the

relation between the classification proposed in this chapter and the VCCS graphs of chapter 3 is discussed.

5.2 Transmission Parameters and Kirchhoff Relations

We will now consider the transmission parameters for the simple case of circuits with only one VCCS. The aim of the discussion is discover how these parameters are determined and which different possibilities exist.

According to chapter 2, transmission parameters can be determined as shown in Figure 5-1: by forcing a voltage or current at the input of the transactor, and measuring the resulting output voltage or current at an open or short-circuited output respectively. The ratio between the involved input and output variable gives the transmission parameter. The four test conditions shown in Figure 5-1 are such that only one transmission parameter determines the transfer from input to output. From now on, we will refer to a transactor that is forced in one of these four test conditions as an A-, B-, C- or D-determined transactor, respectively.

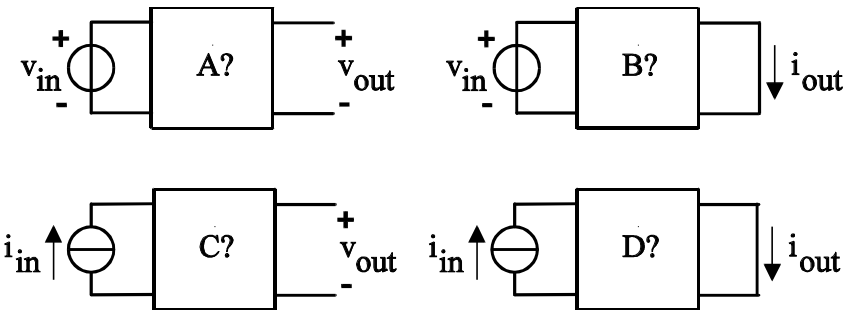


Figure 5-1: Four test set-ups for the determination of A, B, C and D. The transactor is said to be A-, B-, C- and D-determined under these conditions, since only one transmission parameter determines the signal transfer from input to output.

With reference to the definition of these parameters in Figure 5-1, the following statement can now be made:

All transmission parameters that can be realised with a circuit can be found as follows: determine all different ways of forcing a voltage or current to the circuit, and all possible resulting output variables under open- or short-circuit conditions. Finally, calculate ratios of the input and output variables to find the transmission parameters.

The number of different possibilities rapidly increases with the number of components constituting a circuit. However, if we restrict ourselves to circuits with *only one VCCS* apart from the *independent* voltage or current *source*, we can determine all different possibilities. In this case only interconnections are available to force a voltage or current and establish an open or short-circuited output (no other components are allowed). The resulting possibilities are governed by Kirchhoff's voltage law (KVL) and current law (KCL):

$$\text{KVL:} \quad \sum_{\text{in a loop}} \text{Voltages} = 0 \tag{5.1}$$

$$\text{KCL:} \quad \sum_{\text{to a node}} \text{Currents} = 0 \tag{5.2}$$

Figure 5-2 shows all possibilities to force a voltage or current to a circuit with one VCCS and one independent source. Only the crucial part of a circuit is shown.

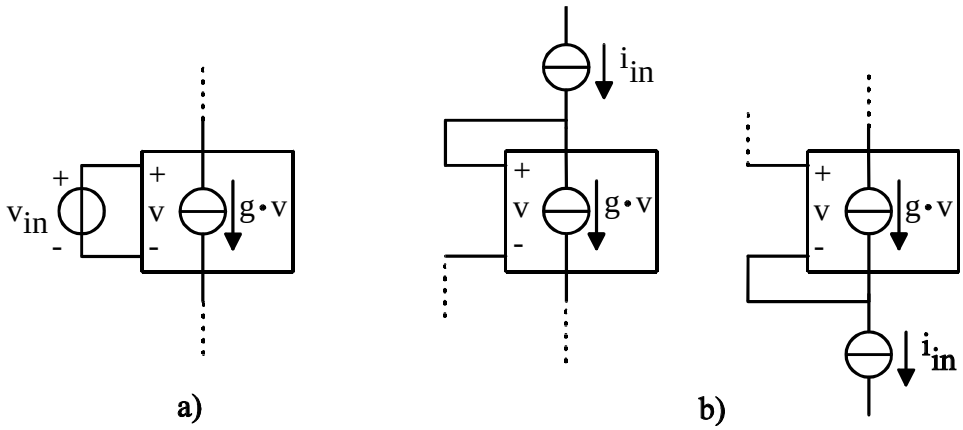


Figure 5-2: The two different ways to force a VCCS variable by means of Kirchhoff's laws: a) the VCCS voltage is forced equal to v_{in} by means of KVL; b) the VCCS current is forced equal to i_{in} by KCL, using negative feedback to the voltage terminals (2 cases).

Figure 5-2a shows an independent voltage source with value v_{in} connected in a loop with the VCCS voltage sense terminals. Since KVL holds for the loop, the VCCS voltage is forced equal to v_{in}. This is the only sensible way, since none of the other VCCS terminals are sensitive to voltage.

Figure 5-2b shows the two possibilities to force the current of a VCCS by means of KCL. The independent current source with value i_{in} is connected to the VCCS at the upper or lower current source node. Since KCL holds for the node, the VCCS current is forced equal to i_{in}, provided that negative feedback to the voltage terminals of the VCCS exists. This is necessary as the current of a VCCS can only be changed by means of the voltage applied to the voltage-sense terminals. To establish negative feedback the connections must be as shown in Figure 5-2b. Other connections render no or positive feedback.

To find transmission parameters, the output variables for an open or short-circuited output are still to be determined. The voltage and current of the VCCS can be chosen for this purpose. If the input voltage of a VCCS is forced and the current of the VCCS is used as output, transmission parameter B is fixed to 1/g. Furthermore, C can be fixed to g, if the VCCS current is forced, while the voltage is used as output.

Apart from using the VCCS variables as output variables, there is an additional possibility if the input and output variables of a transactor are both voltages or currents. This occurs for the A- and D-determined case in Figure 5-1. In these cases the output variable can also be equal to the input variable, or to a sum or difference of the input variable and a VCCS variable of the same type (voltage or current). For circuits with one VCCS, this occurs for the transactors with A=1 and D=1 in Table 3.8. These are the only cases with non-zero A and D. A closer look at the all unity gain cases shows that some are trivial, since there is a direct connection between the input and output terminals (e.g. graph 2a in Figure 3.10). The non-trivial cases are shown in Figure 5-3. In Figure 5-3a, the VCCS current i_p is forced

equal to zero (determining A, i_{out}=0), while the output voltage is the difference between v_{in} and the VCCS voltage. Since i_p=0, the VCCS voltage is also zero and the input voltage is completely transferred to the output (voltage follower). Figure 5-3b shows that the current gain can be equal to 1 (D=1, current follower), if the current of the VCCS is forced equal to the input current, and completely transferred to the output. These voltage and current follower circuits can establish an impedance transformation (high Z_{in} and low Z_{out} respectively low Z_{in} and high Z_{out}). Furthermore they can provide a DC-level shift.

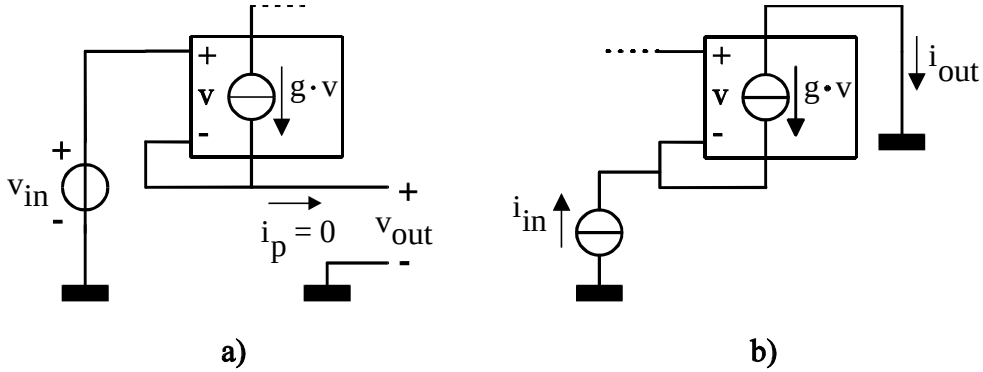


Figure 5-3: Unity gain circuits with one VCCS: a) Voltage buffer; b) Current buffer.

In Table 3.8, zero valued transmission parameters also occur often, which corresponds to an infinite value of the output variable (the input variable that is forced has a finite value). This happens for instance in cases with an open ended current source, either at the input (D equal to 0, if B<>0) or at the output (A or C equal to 0). Furthermore B=0 occurs if a direct connection between input and output exists.

Thus it seems that a transmission parameter for a circuit with one VCCS can be found from two mathematical relations: (1) a relation between the independent source variable and a VCCS variable, and (2) an equation relating the output variable to a source and VCCS variable. Without additional components, these relations can only be KVL or KCL relations.

5.3 Transmission Parameters of Circuits with 2 VCCSs

The possibilities to establish a transmission parameter in a circuits with two VCCSs will now be examined. It will appear that two Kirchhoff relations play a crucial role. To clarify the discussion, first some basic assumptions and conventions that are used will be stated.

5.3.1 Basic Assumptions and Conventions

Circuits with Two VCCSs and Interconnections

The aim of this chapter is to unveil different possibilities to establish transmission parameters with the transactors of chapter 3. Therefore the transactors will only consist of two VCCSs and interconnections as in chapter 3.

I(V) Characteristic and Notation

A VCCS has a voltage-controlled current which can be written as:

$$I = I(V) \tag{5.3}$$

During operation, the VCCS will be biased at a quiescence voltage V_0 and current I_0, that are related by eqn. 5.3. The VCCS characteristic can be approximated by:

$$I(V_0 + v) = I_0(V_0) + i(v) = I_0(V_0) + g(V_0) \cdot v \tag{5.4}$$

where v and i are the small-signal voltage and current excursions from the biasing point, and $g(V_0)$ is the transconductance dI/dV, which depends on the biasing point (V_0,I_0). For shortness, the biasing dependence will often be omitted:

$$i = g \cdot v \tag{5.5}$$

Only one of the variables V and I of the VCCS is independently controllable, the other is dependent according to eqn. 5.3. As discussed in the previous section, only the input voltage of a VCCS can directly be controlled, while current forcing involves feedback to the voltage terminals.

Two VCCSs exist that will be indicated as $VCCS_a$ and $VCCS_b$, and eqn.5.3-5.5 will be used with indices *a* and *b*. The VCCSs are equivalent (the name assignment is arbitrary, but will be standardised later).

Voltage or Current Driven Input, Open or Short-Circuited Output

The transactors have one input and one output. However, this restriction concerns the small-signal variables and not the biasing variables. Since the latter control the transconductance of the VCCSs, and thus the transfer properties of the transactor, these biasing variables will be called control variables from now on. It will be assumed that these control variables are also voltages or currents.

In section 5.2 the transmission parameters of transactors have been defined under *voltage or current driving conditions* at the input. Thus both the input and the control variables can be represented by voltage or current sources. Furthermore, the *output* variables are either *open-circuit voltages* or *short-circuit currents*. It is sometimes convenient to talk about input, control and output variables in a mathematical sense, regardless whether voltage or current variables are concerned. For this purpose the variables S_{in} (input), S_c (control) and S_{out}(output) will be used.

The VCCS Variables and Output Variable are a Function of the Input Variable

During the graph based (small-signal) transmission parameter analysis in chapter 3, the requirement was posed that a unique solution exists for v_a, v_b, i_a and i_b (which may be zero) and a unique non-zero solution for s_{out} (otherwise a transmission parameter is not defined (division by zero)). As s_{in} is the only independent input variable, all variables are functions of s_{in} (non-zero for s_{out}).

In accordance with the requirements of chapter 3, it will now be assumed that the output variable S_{out} and the VCCS variables V_a, V_b, I_a and I_b are functions of S_{in}, i.e. for every value of S_{in} there exists a unique solution for these variables. A transmission parameter is related to these variables as $1/(\delta S_{out}/\delta S_{in})$.

5.3.2 Establishing a Unique Solution for the VCCS Variables

During the graph based (small-signal) transmission parameter analysis in chapter 3, a finite source conductance g_s and load conductance g_l were used. To calculate a transmission parameter, the limit of a ratio of an input and output quantity was evaluated for g_l approaching zero or infinity (depending on the parameter). Now the aim is to determine transmission parameters for transactors with two VCCSs with a voltage or current driven input and an open or short-circuited output. This can render conflicting equations for an open ended current source and for a short-circuited voltage source. If such conflicts occur, a finite impedance is added in series with the involved voltage source or in parallel to the involved current source.

The VCCSs and their voltage and current variables play a crucial role in establishing transmission parameters of VCCS circuits. Suppose now that we realise a transactor using two VCCSs, independent sources and interconnections and want to find a solution for the VCCS variables. Because there are no additional components, KVL and KCL equations are the only means to establish a solution apart from the I(V) relations of the VCCSs. The following observations can now be made:

- The voltage across a current source can take an arbitrary value. Hence, if a current source occurs as a branch in a KVL loop it does not pose constraints on the other voltages in the KVL loop. The same holds for the open terminal output of a transactor. Therefore, such KVL equations do not put any constraints on VCCS voltages.
- The current through a voltage source or through a short-circuit across a transactor output can take an arbitrary value. If such a current occurs in a KCL node equation, the equation does not put constraints on the other currents occurring in the equation. Hence VCCS currents are not affected.
- The current through a voltage sense branch of a VCCS is zero and may force a VCCS current to zero. Similarly a short-circuit may force a VCCS voltage to zero. Such constraints are covered by KVL or KCL equations amongst one or more VCCS variables (these are of the form ....=0).

From these observations the conclusion can be drawn that only Kirchhoff relations amongst the VCCS variables v_a, v_b, i_a, i_b and the independent input variable s_{in} are useful to establish a solution for the VCCS variables v_a, v_b, i_a, i_b (all other seven variables should not occur because of the three observations above).

If we choose to use a DC-coupled circuit biased by voltage and current sources, the small-signal behaviour can be derived from the DC-transfer characteristic by differentiation. For instance, s_{out}/s_{in} is equal to the derivative of S_{out} with respect to S_{in} in the quiescence point. A transactor circuit should have one uniquely defined quiescence point. The above observations on KVL and KCL are independent of the I(V) model. Hence, they can also be applied to large signal variables S_{in}, V_a, V_b, I_a and I_b. It will appear in chapter 6 that this it is often possible to establish a unique quiescence point using the same basic Kirchhoff relations that establish the transmission parameters (but adding additional bias voltage or current variables (control variable S_c)).

In order to establish a unique solution for the VCCS variables V_a, I_a, V_b and I_b, four independent relations amongst the four variables are necessary and sufficient in case of linear equations. If the relations are non-linear, this can also be sufficient, but alternatively no or multiple solutions may exist. This will be discussed in chapter 6 as part of the large signal analysis. Now we will assume that the circuit has a unique biasing point, and evaluate a transmission parameter s_{in}/s_{out}. Since four unknown VCCS variables exist, and two independent VCCS relations (eqn. 5.3 for $VCCS_a$ and $VCCS_b$), *two additional independent relations are needed*. With reference to the observations above it follows that *only KVL and/or KCL relations amongst the VCCS variables and independent input variables are useful* for this purpose. Furthermore, a KVL or KCL equation relating the output variable to the VCCS variables and the input variable is needed.

Figure 5-4 further illustrates the crucial role of the Kirchhoff relations: they establish a relation between the input variables and VCCS variables, and "select" the output variable. Since the *Kirchhoff relations* play such a *crucial role*, they constitute a *suitable classification criterion*. However, as the relation that "selects the output variable" also contains a new unknown (V_{out} or I_{out}), it does not help to establish a solution for the VCCS variables. Therefore it will not be taken into account during the classification, but rather plays a role as a selector of (a linear combination of) variables that are "ready for use".

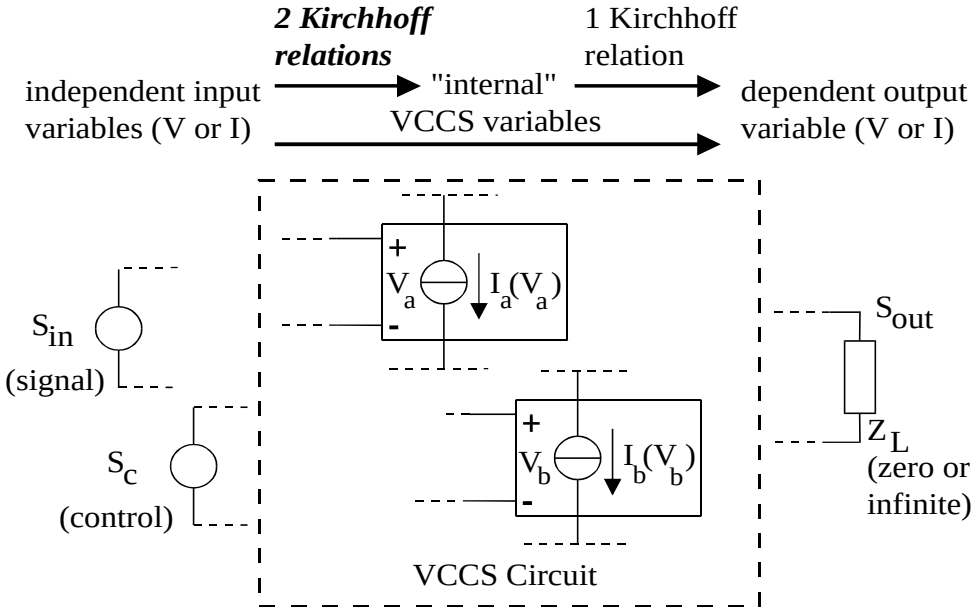
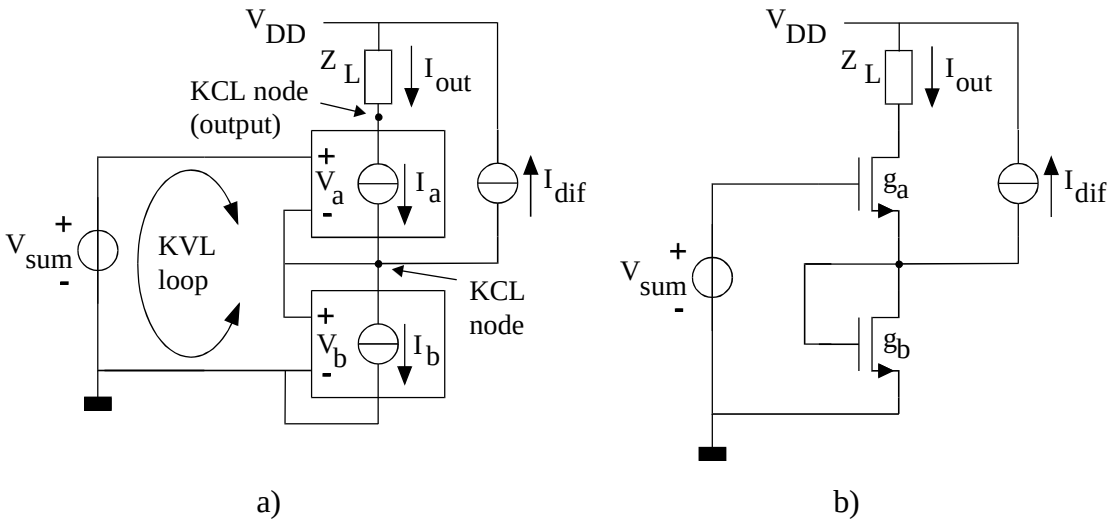


Figure 5-4: The role of Kirchhoff relations in a circuit with two VCCSs: two Kirchhoff relations imposed by interconnections, establish a unique relation between the independent variables S_{in} (input signal), S_c (transactance control), and the "internal" VCCS variables. A third Kirchhoff relation relates S_{out} (output signal) to the independent and/or internal VCCS variables. The ratio S_{in}/S_{out} determines a transmission parameter.

An Example

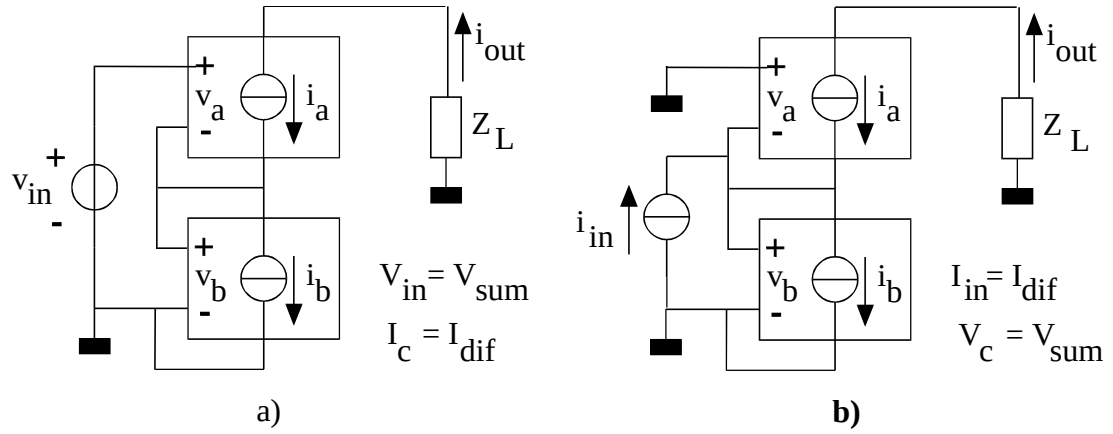
The role of Kirchhoff relations will now be illustrated by an example shown in Figure 5-5a. In this circuit, the sum of the VCCS voltages is forced equal to V_{sum} by a KVL loop, while the difference of the VCCS currents is forced equal to I_{dif} at a KCL node.



a) b)

Figure 5-5: a) Two VCCSs for which the sum of the voltages is forced equal to V_{sum} by KVL and the difference of the currents equal to I_{dif} by KCL, while $I_{out}=I_a$; b) An NMOST circuit implementation.

Furthermore the VCCS current I_a is assigned as output variable I_{out} at a second KCL node (output). By means of the DC values of V_{sum} and I_{dif}, the circuit is biased in a certain quiescence point, which depends on the DC transfer characteristic of the VCCS. This biasing also affects the transconductances g_a and g_b. If the VCCSs are for instance, as shown in Figure 5-5b, equal NMOSTs operating in strong inversion and saturation, the idealised square-law relation eqn. 3.11 can be used to estimate the biasing point. It can easily be shown (see also chapter 6) that both NMOSTs are biased at $V_{TN}+V_0$, if the bias values are $I_{dif0}=0$ and $V_{sum0}=2\cdot V_{TN}+2\cdot V_0$ [49]. In that case both g_a and g_b are equal to $2\cdot k_N\cdot V_0$. If I_{dif} is increased, g_b increases and g_a decreases. Now, there are two possible ways to operate the circuit (assuming $I_{out}=I_a$ is the output variable): either V_{sum} can be the input with I_{dif} as transconductance control variable, or I_{dif} can be the input variable with V_{sum} as current-gain control variable. Figure 5-6 shows the small signal equivalent circuits for these two cases.



a) **b)**

Figure 5-6: Small signal equivalent circuit for the circuit of Figure 5-5. a) V_{sum} is used as the input signal and I_{dif} as a transactance control variable; b) I_{dif} is used as the input signal and V_{sum} as a transactance control variable.

In Figure 5-6a the input signal v_{in} is the signal component of V_{sum}, while the signal component of I_{dif} is zero (I_{dif} is a bias variable). In contrast, in Figure 5-6b input signal i_{in} is the signal component of I_{dif}, while the signal component of V_{sum} is zero. Note, however, that omitting the control variable from the equivalent circuit does not mean that one of the Kirchhoff relations is no longer imposed. Still both the sum of the VCCS voltages and the difference of their currents are imposed, however, one of them is equal to zero ($i_a - i_b = 0$ in Figure 5-6a, $v_a + v_b = 0$ in Figure 5-6b). The small signal equivalent circuit of Figure 5-6a will now be analysed to show that a unique solution exists for the voltages and currrents. The following KVL and KCL equations hold:

$$v_a + v_b - v_{in} = 0 \tag{5.6}$$

$$i_a - i_b = 0 \tag{5.7}$$

Together with eqn. 5.5 for $VCCS_a$ and $VCCS_b$, 4 independent linear equations amongst the VCCS variables exist. This set of equations has a unique solution:

$$v_a = \frac{g_b}{g_a + g_b} \cdot v_{in} \tag{5.8}$$

$$v_b = \frac{g_a}{g_a + g_b} \cdot v_{in} \tag{5.9}$$

$$i_a = i_b = \frac{g_a \cdot g_b}{g_a + g_b} \cdot v_{in} \tag{5.10}$$

Finally, the KCL equation that defines the output current results in:

$$i_{out} = i_a = \frac{g_a \cdot g_b}{g_a + g_b} \cdot v_{in} \tag{5.11}$$

The above equations show that the circuit of Figure 5-6a has a unique solution for the VCCS variables. This holds in general for circuits with two VCCSs in which two independent KVL and/or KCL equations are established, as long as the equations are linear. Note that a given transmission parameter can often be implemented by more than one topology. The circuit of Figure 5-7, for instance, has a different topology in which the difference of the VCCS voltages is forced equal to v_{in} instead of its sum, while the sum of the VCCS currents is the control variable instead of their difference. It realises the same transfer function eqn. 5.11 from v_{in} to i_{out}.

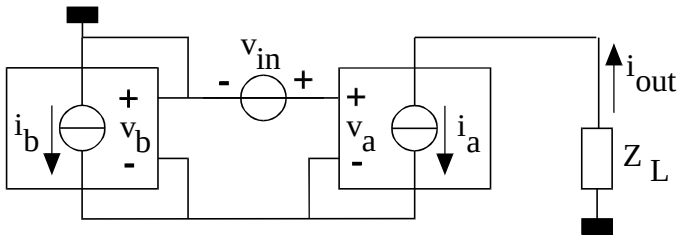


Figure 5-7: Circuit with the same transfer function i_{out}/v_{in} as Figure 5-6a, but with a different topology and a different set of KVL and KCL equations.

In the discussed example there was no effect of the source or load impedance on the transfer function. The transactor had both infinite input and output impedance, i.e. it is a

transconductor. Only transmission parameter B is non-zero, and is determined by a set of two independent Kirchhoff relations and the characteristics of the VCCS. However, in general all 4 transmission parameters may affect the transfer function. For each of these parameters two Kirchhoff relations are crucial. In section 5.6 we will return to this subject.

5.3.3 All Possible Transmission parameters

The aim of this chapter is to find out how transmission parameters are determined and to the classify different possibilities. In the previous section it was shown that two independent Kirchhoff relations are crucial in this respect. We will now consider a procedure to find *all* possible transmission parameters for circuits with two VCCSs, analogously to the procedure discussed in section 5.2:

All transmission parameters, that can be implemented by means of two-port circuits consisting of two VCCSs, are found by the following procedure:

1) ***Generate all different sets of two independent KVL and/or KCL relations amongst the VCCS variables and two independent variables.***
2) ***Calculate for all cases the solution for the VCCS variables in terms of one of the independent variables, while the other independent variable is put to zero.***
3) ***Find all possible output variables under open- or short-circuit conditions for all cases. These are related to VCCS variables and independent variables by means of a KVL or KCL relation.***
4) ***Calculate the transmission parameters as ratios of the non-zero independent variables and output variables.***

Note that this is a mathematical generation procedure that is only partly based on topological constraints. Therefore it is not guaranteed that all cases are physically realisable. Appendix A lists the graphs of VCCS circuits that can actually be implemented.

The open- or short-circuit output variable is related to the VCCS variables by a Kirchhoff relation. This relation is an independent relation, yet one with an additional unknown variable. Hence, it *does not* help to force a solution for the VCCS variables, but serves as a "solved variable selector". Thus two other independent relations between the VCCS variables are needed to force a unique solution for the VCCS variables.

5.4 Classification of Circuits with Two VCCSs

5.4.1 Introduction

As discussed in the previous sections, two Kirchhoff relations play a crucial role in establishing a unique solution for the voltages and currents in transactors with two VCCSs. It will now be examined which different possibilities exist. To create *overview*, the possibilities will be *classificatied* in groups. The classification to be proposed is based on *different sets of two independent Kirchhoff relations amongst the VCCS variables*. It will appear that 3 main classes and 14 subclasses can be distinguished.

The outline of the classification process is as follows: first the different kinds of KVL and KCL equations will be determined in section 5.4.2. Then in section 5.4.3 the difference between circuits with one and *two* VCCSs is clarified by a formal definition of "1VCCS" and "2VCCS" circuits. Finally the 2VCCS circuits are classified in different classes in section 5.4.4. On the fly, 1VCCS circuits are also classified.

5.4.2 Different Kirchhoff Relations amongst VCCS Variables

In this paragraph, the different possibilities to impose KVL and KCL relations amongst the VCCS variables are considered. First all possible sets of relations will be generated. Then the number of sets is reduced, by eliminating sets that are equivalent to others. However, before proceeding, first two types of variables and Kirchhoff relations will be defined, that will appear to be useful during the classification.

Primary VCCS Variable

A primary VCCS variable is the input voltage or output current of a VCCS. A Kirchhoff relation that relates a primary VCCS variable to an independent source variable is referred to as a primary Kirchhoff relation.

Secondary VCCS Variable

A secondary VCCS variable is a sum or difference of primary VCCS variables of the same type (voltage or current) from two VCCSs. A Kirchhoff relation that relates a secondary VCCS variable to an independent source variable is referred to as a secondary Kirchhoff relation.

Considering now first Kirchhoff's voltage law eqn. 5.1. An independent relation between the VCCS voltage variables V_a and V_b and an independent voltage $V_{ind.}$ can be written in the following general form:

$$\alpha_a \cdot V_a + \alpha_b \cdot V_b = V_{ind.} \tag{5.12}$$

$$\alpha_a, \alpha_b \quad \in \quad \left\{ \{-1,0,1\} \middle| \, \alpha_a \neq 0 \vee \alpha_b \neq 0 \right\} \tag{5.13}$$

where α_a and α_b indicate how the corresponding VCCS voltages are connected in the voltage loop. The values -1 and 1 allow for different orientations of the + and - voltage terminals of the VCCSs in the KVL loop. The value 0 indicates that the voltage terminals of a VCCS do not occur in the voltage loop. The condition with both α_a and α_b equal to zero is excluded, since no independent relation amongst the VCCS variables is imposed in that case. Instead of one voltage source in the voltage loop, there could be more voltage sources in series. If this is the case, $V_{ind.}$ can be considered as the sum the voltages of these sources. Working out the combinations defined in eqn. 5.12 systematically renders 8 different voltage relations, as shown in Table 5-1.

If we want to imposes two voltage relations, the number of possibilities is already 8·8=64. Fortunately however, there are a lot of case that need not be considered. The following observations can be made concerning this subject:

a) A lot of relations in Table 5-1 *only differ in sign*. Such a change of sign corresponds to exchanging the + and - terminals of the independent voltage source. Obviously, this does not change the transfer properties of the VCCS circuit, but merely changes the sign of both the excitation and response. Thus, the assignment of the + and - sign to the independent voltage source terminals is arbitrary, and cases with different sign assignments result in the same transfer function.

b) Some relations are equivalent. Forcing VCCS voltage Va is equivalent to forcing Vb, since the VCCSs are assumed to be equivalent. The seeming difference between the VCCSs stems from the fact that different names are assigned to the devices. However, the name assignment is arbitrary and names may be exchanged. Nevertheless, naming VCCSs is necessary, since the currents in de VCCSs are different in general.

α_a	α_b	$V_{ind.}$	**Case identifier**
1	0	$+V_a$	V_P
-1	0	$-V_a$	V_P
0	1	$+V_b$	V_P
0	-1	$-V_b$	V_P
1	1	$V_a + V_b$	V_Σ
-1	-1	$-V_a-V_b$	V_Σ
1	-1	V_a-V_b	V_Δ
-1	1	$-V_a+V_b$	V_Δ

Table 5-1: An overview of the possible KVL equations according to eqn. 5.12.

Looking at Table 5-1 with the above observations in mind, the 8 relations can be reduced to three essentially different ones:

- The first 4 relations all force a VCCS control voltage equal to $V_{ind.}$. The relations either only differ in sign or are equivalent. This case will be referred to as forcing a "Primary voltage" V_P.
- The next *two* relations force the sum of two VCCS voltages. There is only a difference in sign. This case will be referred to as forcing V_Σ.
- The last two relations force the difference of two VCCS voltages. Again, there is only a difference in sign. This case will be referred to as forcing V_Δ.

Thus we see that there are 3 useful different ways of forcing a voltage relation satisfying KVL. These relations can be subdivided into *two* groups: primary and secondary voltage relations. The term primary voltage relation will be used if only one VCCS voltage is involved in the relation (V_P forcing). The term secondary voltage relation will be used when both VCCS voltages are involved (forcing V_Σ or V_Δ).

Consider now Kirchhoff's current law 5.2. It can be written in the following general form that establishes a relation between VCCS currents I_a and I_b and an independent current source value $I_{ind.}$:

$$\beta_a \cdot I_a + \beta_b \cdot I_b = I_{ind.} \tag{5.14}$$

$$\beta_a, \beta_b \in \left\{ \{-1,0,1\} \middle| \beta_a \neq 0 \vee \beta_b \neq 0 \right\} \tag{5.15}$$

Since relation eqn. 5.14 has the same form as eqn. 5.12, an analogous derivation as for voltage relations can be made for current relations. This results in 3 different ways of imposing a current relation satisfying Kirchhoff's current law, namely:

a) Forcing a primary VCCS current denoted as forcing I_P.

b) Forcing a sum of two VCCS currents denoted as forcing I_Σ.

c) Forcing a difference of two VCCS currents denoted as forcing I_Δ.

Analogous to the voltage case, these relations will be subdivided into primary current relations and secondary current relations.

Summarising, both for voltages and for currents, there are 3 different Kirchhoff relations amongst the VCCS variables, as shown in Figure 5-8. These relations can be subdivided in relations involving primary variables (the VCCS voltage or current) and relations involving secondary variables (sums or differences of primary variables).

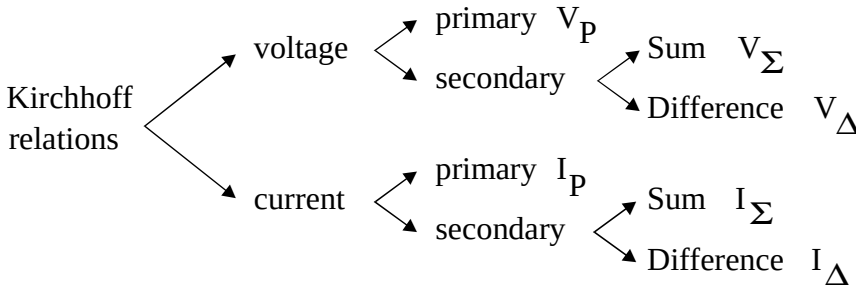


Figure 5-8: Overview of different Kirchhoff relations amongst VCCS variables.

5.4.3 "1VCCS" and "2VCCS" Circuits

As discussed in paragraph 5.3 two independent Kirchhoff relations need to be imposed, to implement a useful transactor with two VCCSs. For a transactor with one VCCS, only one relation is needed. If two of these circuits are combined, again a circuit with two VCCSs results. In this case two primary variables are forced: each VCCS variable merely depends on one independent source variable and the variables of $VCCS_a$ and $VCCS_b$ are independent. Because of this independence, the circuits can be seperated in two subcircuits. In other circuits this is not possible because of interactions. To make a clear distinction, "1VCCS" circuits and "2VCCS" circuits will now be defined.

1VCCS Circuit

A 1VCCS circuit is a circuit with one VCCS, which is connected to ideal voltage or current sources in such a way, that a primary VCCS variable is forced.

2VCCS Circuit

A 2VCCS circuit is a circuit consisting of two VCCSs, which is connected to ideal voltage and/or current sources such that two independent Kirchhoff relations amongst the VCCS variables exist, where at least one of them is a secondary relation.

Now, if two primary Kirchhoff relations hold in a circuit, it *can be seperated* in two 1VCCS circuits. For *2VCCS circuits*, such a *seperation not possible*, since there is interaction between the VCCSs.

5.4.4 Classification: Different Sets of two Kirchhoff Relations

Consider now the classification of possibilities to impose a set of two Kirchhoff relations, given the basic voltage and current relations shown in Figure 5-8. Three main classes can be distinguished based on these sets:

1) The *{V,V} class*, if a set of two voltage relations is imposed.
2) The *{I,I} class*, if a set of two current relations is imposed.
3) The *{V,I} class*, if a set of one voltage and one two current relations is imposed.

Starting with sets of two voltage relations, and keeping in mind that at least one secondary Kirchhoff relation should exist for a 2VCCS circuit, there are two possibilities:

- Sets with one primary and one secondary voltage relation. This renders two sets of relations: $\{V_P,V_\Sigma\}$ and $\{V_P,V_\Delta\}$.
- Sets with two secondary voltage relations. Now there are four possibilities:

  a) $\{V_\Sigma,V_\Sigma\}$

  b) $\{V_\Sigma,V_\Delta\}$

  c) $\{V_\Delta,V_\Sigma\}$

  d) $\{V_\Delta,V_\Delta\}$

  However, a) and d) are sets with two identical and thus not independent relations. Furthermore b) and c) are equivalent sets of relations. Thus, one set $\{V_\Sigma,V_\Delta\}$ remains.

Thus the {V,V} class can be subdivided in 3 subclasses with essentially different sets of independent voltage relations satisfying KVL. The subclasses are listed in Table 5-2.

Subclass	$\mathbf{V_{ind1}}$**=....**	$\mathbf{V_{ind2}}$**=...**
$\{V_P,V_\Sigma\}$	V_a	V_a+V_b
$\{V_P,V_\Delta\}$	V_a	V_a-V_b
$\{V_\Sigma,V_\Delta\}$	V_a+V_b	V_a-V_b

Table 5-2: The 3 different subclasses of the {V,V} class and the corresponding KVL equations that will be used by convention.

For the ease of comparison, uniform naming and sign assignments for the VCCS variables will be introduced. Unless otherwise stated, V_a will be reserved for the primary variable that is forced, and the sign of α_a will be chosen positive. The above conventions are used in the relations given in Table 5-2.

Following an analogous derivation for set of current relations, also three subclasses of the {I,I} class can be defined. These subclasses and the relations that will be used for them by convention are listed in Table 5-3.

Subclass	I_{ind1}=....	I_{ind2}=...
$\{I_P,I_\Sigma\}$	I_a	I_a+I_b
$\{I_P,I_\Delta\}$	I_a	I_a-I_b
$\{I_\Sigma,I_\Delta\}$	I_a+I_b	I_a-I_b

Table 5-3: The 3 different subclasses of the {I,I} class and the corresponding KCL equations that will be used by convention.

Finally, consider the possibilities to construct sets with one voltage and one current relation. Since there are three different voltage relations and three different current relations, 3·3=9 combinations exist. Again, the case with two primary variables can be dropped, since it involves two independent 1VCCS equations. The remaining 8 subclasses and the relations that will be used for them by convention are listed in Table 5-4.

Subclass	V_{ind} =....	I_{ind} =...
$\{V_P,I_\Sigma\}$	V_a	I_a+I_b
$\{V_P,I_\Delta\}$	V_a	I_a-I_b
$\{V_\Sigma,I_P\}$	V_a+V_b	I_a
$\{V_\Delta,I_P\}$	V_a-V_b	I_a
$\{V_\Sigma,I_\Sigma\}$	V_a+V_b	I_a+I_b
$\{V_\Sigma,I_\Delta\}$	V_a+V_b	I_a-I_b
$\{V_\Delta,I_\Sigma\}$	V_a-V_b	I_a+I_b
$\{V_\Delta,I_\Delta\}$	V_a-V_b	I_a-I_b

Table 5-4: The 8 different subclasses of the {V,I} class and the corresponding KVL and KCL equations that will be used by convention.

None of these relations are equivalent. Thus it appears that 2VCCS circuits can be classified in 3 main classes with 3+3+8=14 subclasses, based on different sets of two Kirchhoff relations. In a similar way the previously defined 1VCCS circuits can be classified. In this case there are only two classes as shown in Table 5-5: either the primary voltage, or the primary current of a VCCS is be forced.

Class	KVL or KCL relation
$\{V_P\}$	$V_{ind} = V_P$
$\{I_P\}$	$I_{ind} = I_P$

Table 5-5: The two different classes of the 1VCCS circuits and the corresponding KVL or KCL equation that is imposed.

5.4.5 Possible Output Variables

As discussed in paragraph 5.2 and 5.3, output variables of VCCS circuits are related to VCCS variables and/or independent input variables by KVL or KCL. Thus an output voltage can be written in the following general form:

$$V_{out} = \alpha_a V_a + \alpha_b V_b + \alpha_{ind1} V_{ind1} + \alpha_{ind2} V_{ind2} \tag{5.16}$$

with $$\alpha_a, \alpha_b, \alpha_{ind1}, \alpha_{ind2} \in \left\{ \{-1,0,1\} \middle| \alpha_a \neq 0 \vee \alpha_b \neq 0 \vee \alpha_{ind1} \neq 0 \vee \alpha_{ind2} \neq 0 \right\} \tag{5.17}$$

Analogously, an output current can be written as:

$$I_{out} = \beta_a i_a + \beta_b I_b + \beta_{ind1} I_{ind1} + \beta_{ind2} I_{ind2} \tag{5.18}$$

with $$\beta_a, \beta_b, \beta_{ind1}, \beta_{ind2} \in \left\{ \{-1,0,1\} \middle| \beta_a \neq 0 \vee \beta_b \neq 0 \vee \beta_{ind1} \neq 0 \vee \beta_{ind2} \neq 0 \right\} \tag{5.19}$$

The unknowns in the above equations are the primary VCCS variables V_a, V_b, I_a and I_b. These will be solved in the following sections for the three main classes. All possible output variables and transmission parameters are easily derived from V_a, V_b, I_a and I_b.

5.5 Transfer Function from Input to VCCS Variables

This section deals with the analysis of the small-signal transfer function of all different classes of 1VCCS and 2VCCS circuits. Since the output variables and hence the transmission parameters are related to VCCS variables and the independent input variables by KVL or KCL, it is useful to solve the primary VCCS variables. In section 5.5.1, this is done for the two classes of 1VCCS circuits and in the sections 5.5.2-5.5.4 for all classes of 2VCCS circuits. Especially for the latter case, an advantage of the use of classification will become clear: it is sufficient to calculate the transfer function for the three main classes (section 5.5.2-5.5.4), while the results for the subclasses are found by simple substitutions.

5.5.1 The Solution for the 1VCCS circuits

Table 5-6 shows the analysis results for 1VCCS circuits: as expected only a v-i relation and its inverse are possible. The trivial "1" entries in the table are mentioned for completeness.

Class	Input Variable	Primary VCCS Variables	
	s_{in}	v_a/s_{in}	i_a/s_{in}
$\{V_P\}$	v_a	1	g_a
$\{I_P\}$	i_a	$1/g_a$	1

Table 5-6: Transfer function the all possible input variables to the primary VCCS variables for 1VCCS circuits.

5.5.2 The Solution for the {V,V} Class

The solution for the VCCS variables in the small-signal linearised 2VCCS circuit for the {V,V} class will now be calculated. The two voltage relations that are established for this class are given by:

$$\alpha_{a1} \cdot v_a + \alpha_{b1} \cdot v_b = v_{ind1} \tag{5.20}$$

$$\alpha_{a2} \cdot v_a + \alpha_{b2} \cdot v_b = v_{ind2} \tag{5.21}$$

where coefficients α are for the subclasses $\{V_P,V_\Sigma\}$, $\{V_P,V_\Delta\}$ and $\{V_\Sigma,V_\Delta\}$ are respectively given by:

$$\{\alpha_{a1}, \alpha_{b1}, \alpha_{a2}, \alpha_{b2}\} \in \{\{1,0,1,1\}, \{1,0,1,-1\}, \{1,1,1,-1\}\} \tag{5.22}$$

Since α_{a1} and α_{a2} are always 1, due to the conventions discussed in the previous section, these coefficient can be dropped from eqn. 5.22, resulting in:

$$v_a + \alpha_{b1} \cdot v_b = v_{ind1} \tag{5.23}$$

$$v_a + \alpha_{b2} \cdot v_b = v_{ind2} \tag{5.24}$$

$$\{\alpha_{b1}, \alpha_{b2}\} \quad \in \quad \{\{0,1\},\{0,-1\},\{1,-1\}\} \tag{5.25}$$

From the above equations v_a and v_b can easily be solved as:

$$v_a = \frac{\alpha_{b2} \cdot v_{ind1} - \alpha_{b1} \cdot v_{ind2}}{\alpha_{b2} - \alpha_{b1}} \tag{5.26}$$

$$v_b = \frac{v_{ind2} - v_{ind1}}{\alpha_{b2} - \alpha_{b1}} \tag{5.27}$$

and assuming small-signal values v_{ind1} or v_{ind2} for the sources, the following solutions are found for the small-signal value of the VCCS currents i_a and i_b:

$$i_a = g_a \cdot \frac{\alpha_{b2} \cdot v_{ind1} - \alpha_{b1} \cdot v_{ind2}}{\alpha_{b2} - \alpha_{b1}} \tag{5.28}$$

$$i_b = g_b \cdot \frac{v_{ind2} - v_{ind1}}{\alpha_{b2} - \alpha_{b1}} \tag{5.29}$$

The secondary voltages and currents are easily calculated as sums and differences of the above solutions for the primary variables.

Class	Input variable sin	Control variable	Primary VCCS Variables			
			v_a/s_{in}	v_b/s_{in}	i_a/s_{in}	i_b/s_{in}
$\{V_P,V_\Sigma\}$	v_a	V_Σ	1	-1	g_a	$-g_b$
	v_Σ	V_a	0	1	0	g_b
$\{V_P,V_\Delta\}$	v_a	V_Δ	1	1	g_a	g_b
	v_Δ	V_a	0	-1	0	$-g_b$
$\{V_\Sigma,V_\Delta\}$	v_Σ	V_Δ	1/2	1/2	$\frac{1}{2} \cdot g_a$	$\frac{1}{2} \cdot g_b$
	v_Δ	V_Σ	1/2	-1/2	$\frac{1}{2} \cdot g_a$	$-\frac{1}{2} \cdot g_b$

Table 5-7: All transfer functions to primary VCCS variables for the {V,V} class.

As discussed in the previous section, one of the independent voltages v_{ind1} and v_{ind2} serves as signal input, and the other as transfer function control input. Substitution of the α coefficients and the actual independent voltage source values (s_{in} if the source is the signal input, zero if it is a control input), leads to the transfer function listed in Table 5-7.

In the table the transfer function from s_{in} to the primary VCCS variables is shown. The voltage ratios that occur are either 0, ±½ or ±1, as is directly forced by KVL, independent of the VCCS characteristics (the independent sources force these voltages, the VCCSs "don't do anything"). The VCCS currents are simply found by multiplying these voltages by g_a and g_b respectively.

5.5.3 The Solution for the {I,I} Class

In an analogous fashion as for the {V,V} class, the solution for the {I,I} class is found starting with the equations:

$$i_a + \beta_{b1} \cdot i_b = i_{ind1} \tag{5.30}$$

$$i_a + \beta_{b2} \cdot i_b = i_{ind2} \tag{5.31}$$

where the values of the coefficients β for the subclasses $\{I_P,I_\Sigma\}$, $\{I_P,I_\Delta\}$ and $\{I_\Sigma,I_\Delta\}$ are respectively given by:

$$\{\beta_{b1},\beta_{b2}\} \in \{\{0,1\},\{0,-1\},\{1,-1\}\} \tag{5.32}$$

Class	Input variable s_{in}	Control variable	Primary VCCS Variables			
			v_a/s_{in}	v_b/s_{in}	i_a/s_{in}	i_b/s_{in}
$\{I_P,I_\Sigma\}$	i_a	I_Σ	$\frac{1}{g_a}$	$-\frac{1}{g_b}$	1	-1
	i_Σ	I_a	0	$\frac{1}{g_b}$	0	1
$\{I_P,I_\Delta\}$	i_a	I_Δ	$\frac{1}{g_a}$	$\frac{1}{g_b}$	1	1
	i_Δ	I_a	0	$-\frac{1}{g_b}$	0	-1
$\{I_\Sigma,I_\Delta\}$	i_Σ	I_Δ	$\frac{1}{2\cdot g_a}$	$\frac{1}{2\cdot g_b}$	1/2	1/2
	i_Δ	I_Σ	$\frac{1}{2\cdot g_a}$	$-\frac{1}{2\cdot g_b}$	1/2	-1/2

Table 5-8: All transfer functions to the primary VCCS variables for the {I,I} class.

This results in I_a and I_b solutions (for both small and large signals):

$$i_a = \frac{\beta_{b2} \cdot i_{ind1} - \beta_{b1} \cdot i_{ind2}}{\beta_{b2} - \beta_{b1}} \tag{5.33}$$

$$i_b = \frac{i_{ind2} - i_{ind1}}{\beta_{b2} - \beta_{b1}} \tag{5.34}$$

and assuming small signals for i_{ind1} or i_{ind2} the following solutions are found for v_a, v_b:

$$v_a = \frac{1}{g_a} \cdot \frac{\beta_{b2} \cdot i_{ind1} - \beta_{b1} \cdot i_{ind2}}{\beta_{b2} - \beta_{b1}} \tag{5.35}$$

$$v_b = \frac{1}{g_b} \cdot \frac{v_{ind2} - v_{ind1}}{\beta_{b2} - \beta_{b1}} \tag{5.36}$$

Substitution of the appropriate values in the expressions leads to the results of Table 5-8. The current ratios that occur are either 0, ±½ or ±1, as follows directly from KCL, independent of the VCCS characteristics (the sources force these currents, the VCCS "does nothing"). The VCCS voltages are found by dividing the currents by g_a and g_b respectively.

5.5.4 The Solution for the {V,I} Class

For the {V,I} case, one voltage and one current relation is imposed, given by:

$$v_a + \alpha_b \cdot v_b = v_{ind} \tag{5.37}$$

$$i_a + \beta_b \cdot i_b = i_{ind} \tag{5.38}$$

where the coefficient α_b and β_b take the following values depending on the subclass:

$$\{\alpha_b, \beta_b\} \in \left\{ \begin{matrix} \{0,1\}, \{0,-1\}, \{1,0\}, \{-1,0\} \\ \{1,1\}, \{1,-1\}, \{-1,1\}, \{-1,-1\} \end{matrix} \right\} \tag{5.39}$$

The solution for the primary variables is now:

$$v_a = -\frac{\beta_b g_b v_{ind}}{\alpha_b g_a - \beta_b g_b} + \frac{\alpha_b i_{ind}}{\alpha_b g_a - \beta_b g_b} \tag{5.40}$$

$$v_b = \frac{g_a v_{ind}}{\alpha_b g_a - \beta_b g_b} - \frac{i_{ind}}{\alpha_b g_a - \beta_b g_b} \tag{5.41}$$

$$i_a = -\frac{\beta_b g_a g_b v_{ind}}{\alpha_b g_a - \beta_b g_b} + \frac{\alpha_b g_a i_{ind}}{\alpha_b g_a - \beta_b g_b} \tag{5.42}$$

$$i_b = \frac{g_a g_b v_{ind}}{\alpha_b g_a - \beta_b g_b} - \frac{g_b i_{ind}}{\alpha_b g_a - \beta_b g_b} \tag{5.43}$$

Looking at the above four equations, we see that singularities can occur, since the denominator of the relations can become zero. This happens for the $\{V_\Sigma, I_\Sigma\}$ (coefficients α_b and β_b both equal to 1) and $\{V_\Delta, I_\Delta\}$ class (both coefficient equal to -1) for $g_a = g_b$. For these cases there is no unique solution or no solution.

By suitable substitutions the transfer functions for the 8 classes are found as shown in Table 5-9. In contrast to the previous classes, now also voltage and current transfer functions occur, that are determined by a ratio of transconductance values. Furthermore transconductances and transresistances determined by both g_a and g_b occur.

5.5.5 Evaluation of the Transmission Parameter Results

Looking at the results of Table 5-7 through Table 5-9, and comparing the results for different classes, we see that none of the classes render the same set of transfer functions. This means that none of the classes is equivalent to another class (the existence of equivalent cases would indicate that there are redundant classes, which is not desirable).

The aim of this chapter was to unveil different possibilities to establish a transmission parameter. Hence, it should be possible to obtain the different transmission parameters expressions found in chapter 3 (e.g. in Table 3.16) from Table 5-7 through Table 5-9. Indeed, this appears to be possible either directly, or after adding or subtracting 1 to a voltage or current ratio (in cases where the output variable is defined by a Kirchhoff relation involving the independent source variable).

Class	Input variable s_{in}	Control variable	Primary VCCS variables			
			v_a/s_{in}	v_b/s_{in}	i_a/s_{in}	i_b/s_{in}
$\{V_P,I_\Sigma\}$	v_a	I_Σ	1	$-\frac{g_a}{g_b}$	g_a	$-g_a$
	i_Σ	V_a	0	$\frac{1}{g_b}$	0	1
$\{V_P,I_\Delta\}$	v_a	I_Δ	1	$\frac{g_a}{g_b}$	g_a	g_a
	i_Δ	V_a	0	$-\frac{1}{g_b}$	0	-1
$\{V_\Sigma,I_P\}$	v_Σ	I_a	0	1	0	g_b
	i_a	V_Σ	$\frac{1}{g_a}$	$-\frac{1}{g_a}$	1	$-\frac{g_b}{g_a}$
$\{V_\Delta,I_P\}$	v_Δ	I_a	0	-1	0	$-g_b$
	i_a	V_Δ	$\frac{1}{g_a}$	$\frac{1}{g_a}$	1	$\frac{g_b}{g_a}$
$\{V_\Sigma,I_\Sigma\}$	v_Σ	I_Σ	$-\frac{g_b}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$	$-\frac{g_a\cdot g_b}{g_a-g_b}$	$\frac{g_a\cdot g_b}{g_a-g_b}$
	i_Σ	V_Σ	$\frac{1}{g_a-g_b}$	$-\frac{1}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$	$-\frac{g_b}{g_a-g_b}$
$\{V_\Sigma,I_\Delta\}$	v_Σ	I_Δ	$\frac{g_b}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$\frac{g_a\cdot g_b}{g_a+g_b}$	$\frac{g_a\cdot g_b}{g_a+g_b}$
	i_Δ	V_Σ	$\frac{1}{g_a+g_b}$	$-\frac{1}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$-\frac{g_b}{g_a+g_b}$
$\{V_\Delta,I_\Sigma\}$	v_Δ	I_Σ	$\frac{g_b}{g_a+g_b}$	$-\frac{g_a}{g_a+g_b}$	$\frac{g_a\cdot g_b}{g_a+g_b}$	$-\frac{g_a\cdot g_b}{g_a+g_b}$
	i_Σ	V_Δ	$\frac{1}{g_a+g_b}$	$\frac{1}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$\frac{g_b}{g_a+g_b}$
$\{V_\Delta,I_\Delta\}$	v_Δ	I_Δ	$-\frac{g_b}{g_a-g_b}$	$-\frac{g_a}{g_a-g_b}$	$-\frac{g_a\cdot g_b}{g_a-g_b}$	$-\frac{g_a\cdot g_b}{g_a-g_b}$
	i_Δ	V_Δ	$\frac{1}{g_a-g_b}$	$\frac{1}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$	$\frac{g_b}{g_a-g_b}$

Table 5-9: All transfer functions to the primary VCCS variables for the {V,I} class.

5.6 Relation between Chapter 3 and 5

The relation between the results of this chapter and the results obtained from the graphs in chapter 3 will now be discussed. This will be done by looking first at an arbitrary example of a transactor shown in Figure 5-9 with its graph and VCCS representation.

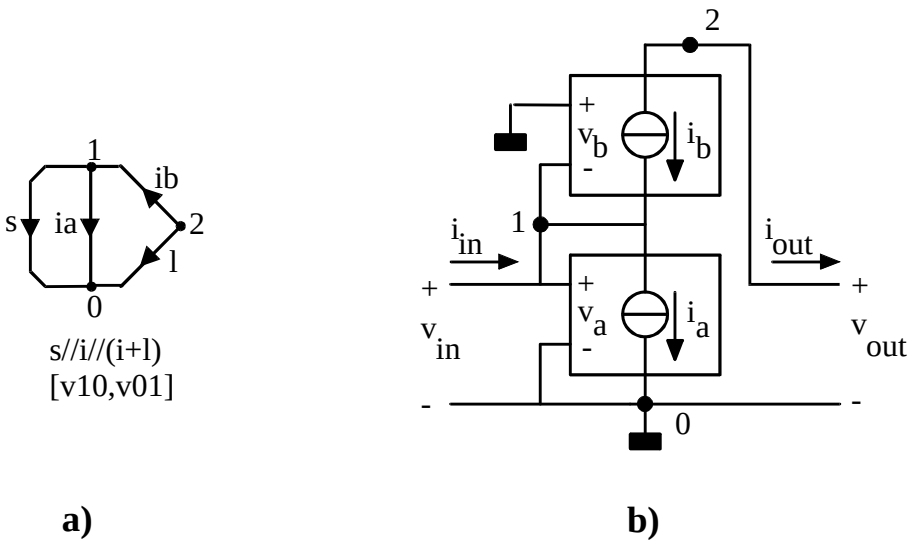


Figure 5-9: Transactor used to discuss the relation between chapter 3 and 5: a) Graph representation; b) VCCS representation.

The graph is a s//i//(i+l) graph, with control voltaged v_{10} and v_{01} for v_a and v_b respectively. According to chapter 3, this graph has the following transmission parameters:

$$A = 0 \quad B = \frac{1}{g_b} \quad C = 0 \quad D = 1 + \frac{g_a}{g_b}$$

Using the results of the current chapter, it should be possible to find the same results. To do so, we have to find out to which class a circuit belongs and what are its input and output variables. We can then use the tables derived in the previous sections to find the transmission parameter values. The classification of VCCS circuits, as proposed in this chapter, takes Kirchhoff relations that are established in a circuit, as a starting point. Since we want to determine the transmission parameters of a transactor, we can consider the transactor biased in its A-, B-, C- and D-determined mode (see section 5.2). Figure 5-10 shows the transactor of Figure 5-9 in these modes.

In principle, it is possible that all of these 4 cases correspond to 4 different classes. However, there are relations between them:

- Case A and B have the same voltage source as input variable.
- Similarly, case C and D share the same current source input variable.
- Case A and C share an open output.
- Case B and D share a short-circuited output.

The class to which a circuit belongs can be determined by systematically writing down Kirchhoff relation for a circuit, and rewriting them as 2 independent relations amongst the VCCS variables. However, with some experience, it is easily determined by inspection from a circuit diagram.

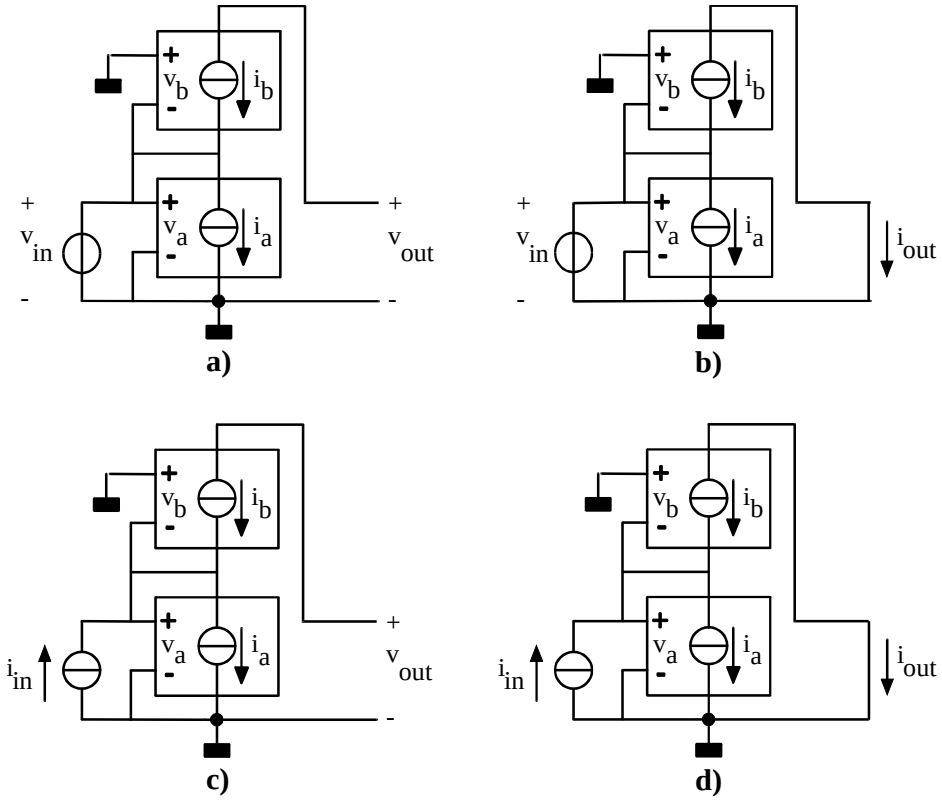


Figure 5-10: The transactor of Figure 5-9, forced in respectively an A-, B-, C- and D-determined mode for figure a, b, c and d.

For the circuits of Figure 5-10 the results are listed in Table 5-10, along with the input and output variables. It appears that circuit a and b, and circuit c and d belong to the same class. However, this is not always true: in some cases the difference between an open- and short-circuit output influences the Kirchhoff relations that determine the classification. Using Table 5-7 and Table 5-9, the transmission shown in the Table 5-10 are found. For case a and c, this leads to infinite output voltages, resulting in zero transmission parameters A and C. For case b and d, the same results as in chapter 3 are found, as expected.

Circuit identifier	Class	Input var. s_{in}	Output var. s_{out}	Transm. par. s_{in}/s_{out}
a (A-determined)	$\{V_P,V_\Sigma\}$	$v_p = v_a = v_{in}$	$v_{out}=-i_b\cdot\infty$	0
b (B-determined)	$\{V_P,V_\Sigma\}$	$v_p = v_a = v_{in}$	$i_{out}=-i_b=g_b v_{in}$	$1/g_b$
c (C-determined)	$\{V_\Sigma,I_\Delta\}$	$i_\Delta=i_{in}$	$v_{out}=-i_b\cdot\infty$	0
d (D-determined)	$\{V_\Sigma,I_\Delta\}$	$i_\Delta=i_{in}$	$i_{out} = -i_b = \frac{g_b}{g_a + g_b} i_{in}$	$1+g_a/g_b$

Table 5-10: Classification of the 4 circuits of Figure 5-10 and the resulting transmission parameters.

Comparison of the Graph Based and Classification Based Analysis

It has now been demonstrated that the transmission parameters for a transactor can be found via the classification of the A-, B-, C- and D-determined transactor. On first sight, this may seem to be a rather indirect way of analysing the properties of a transactor. However, a distinct advantage is its general applicability for all graphs with one and two

VCCSs. Thus 145 transactor graphs are covered with a handful of mathematical equations. Moreover, the number of circuit implementations that is covered in this way is even much higher (several possible transconductor implementations can be used).

At this point, it might be helpful for a clear understanding to compare the analysis method used in chapter 3 to the one presented in this chapter. Table 5-11 summarises the most important differences between the methods. Apart from the fact that classes of circuits can be analysed in one run, an important advantage of the classification based method is that only 2 Kirchhoff relations are needed to solve the VCCS variables. This simplifies the mathematics, and makes it even possible to derive analytical relations for the non-linear behaviour of VCCS circuit as will be discussed in the next chapter.

Graph based Analysis (chapter 3)	**Classification based Analysis (this chapter)**
Analysis of only 1 circuit	Analysis of a class of circuits
Arbitrary source and load impedance	Voltage or current driven input and open or short-circuited output
Requires 6 independent Kirchhoff relations (6 ports with 12 port voltages and currents, 6 element equations => 6 relations needed)	Requires 2 independent Kirchhoff relations (2 VCCSs with 4 relevant VCCS variables, 2 I(V) relation available => 2 relations needed)
Solves all voltages and currents and renders all 4 transmission parameters	Solves only the VCCS variables
-	A third Kirchhoff relation defines the output variable and renders 1 transmission parameter

Table 5-11: Comparison of the transmission parameter analysis method used in chapter 3 and in this chapter.

5.7 Usefulness of the Classification

Limitations: VCCS model

In the previous sections it was shown that considerable analysis effort can be saved by classifying the VCCS circuits, and analysing them in classes rather than individually. However, the VCCS idealisation and the classification that is based on it, also has its limitations. If we are interested in a property that cannot be related directly to the ideal VCCS model, no generalised approach is possible. Unfortunately this occurs for some relevant effects, e.g. the finite input and output impedance. If we want to model these impedances, additional current branches are introduced in the VCCS graphs. As a result the classification cannot be applied, since it holds for circuits with one or two VCCSs and ideal sources.

Another important property that suffers from similar problems is the high-frequency behaviour. Transconductors, but also other VCCS circuits like a current amplifier, are well-known for their good high-frequency behaviour. In fact this is an important motivation for their use in several applications. Unfortunately, the HF behaviour of circuits often critically

depends on circuit details. A generalised approach, that tends to neglect details and parasitics, is then less suitable. A good HF model takes into account several capacitances that exist in the physical VCCS implementation. Again, a graph representation of such a HF model has several additional current branches compared to the VCCS graphs used in chapter 3. Thus the graphs of chapter 3 and the classification in this chapter seem not very useful for this purpose. Nevertheless, there are some possibilities, e.g. to find a coarse first order approximation of the bandwidth of VCCS circuits by means of the dominant pole approximation method [22]. The impedance between node-pairs, that is needed for this method, can easily be derived from the graphs. Furthermore, symbolic analysis CAD tools for AC analysis are available [158]. Also, the HF model of a transactor depends rather strongly on its implementation. Therefore, HF behaviour will not be treated as a general sense, but only on circuit implementation level using simulations.

What Can and Will be Done?

Fortunately quite some important properties of VCCS circuits can be analysed using a generalised approach. Amongst these are the biasing point, non-linearity and noise. The analysis of these properties is the subject of the subsequent chapters.

5.8 Summary and conclusions

In this chapter the classification of circuits with two VCCSs has been addressed. The development of the classification and its main conclusions are summarised below.

Transmission Parameters and Kirchhoff Relations

- A transactor driven by a voltage or current source, which has an open or short-circuited output, has a transfer function that is entirely determined by either parameter A, B, C or D (A-, B-, C- or D-determined transactor).
- The transmission parameters that can be implemented with a circuit can be found by determining all different ways to force a voltage or current to the circuit, and finding all possible resulting open or short-circuit output variables.
- In transactors that merely consist of VCCSs driven by independent sources, KVL and/or KCL relations and the I(V) characteristic of the VCCS determine the transmission parameters.

Imposing Kirchhoff Relations amongst the Variables of Two VCCSs

- In order to force a unique solution for the 4 VCCS variables, 4 independent equations amongst these variables are necessary and sufficient, provided that the equations are linear. If the VCCS characteristics are non-linear, this is not always sufficient as will be discussed in the next chapter.
- Since two I(V) relations for the two VCCSs are available, two additional independent Kirchhoff relations need to be established by interconnections (total: four equations).

- Primary and secondary VCCS variables and Kirchhoff relations have been defined. The adjective primary is used if a single VCCS voltage or current is involved, while secondary is used if sums or differences of VCCS variables are concerned.
- 1VCCS and 2VCCS circuits have been defined. The decisive difference between these circuits is the presence of a secondary Kirchhoff relation for 2VCCS circuits.

Classification of Circuits

- As Kirchhoff relations play a crucial role, 2VCCS circuits are classified based on the sets of two independent Kirchhoff relations amongst the VCCS variables.
- Three main classes of 2VCCS circuits can be defined, indicated as {V,V}, {I,I} and {V,I}, referring to the sets of two equations that are established.
- Three subclasses of the {V,V} class can be defined: $\{V_P,V_\Sigma\}$, $\{V_P,V_\Delta\}$, $\{V_\Sigma,V_\Delta\}$.
- Three subclasses of the {I,I} class can be defined: $\{I_P,I_\Sigma\}$, $\{I_P,I_\Delta\}$, $\{I_\Sigma,I_\Delta\}$.
- Eight subclasses of the {V,I} class can be defined: four with one primary and one secondary variable: $\{V_P,I_\Sigma\}$,$\{V_P,I_\Delta\}$,$\{V_\Sigma,I_P\}$,$\{V_\Delta,I_P\}$; four others with two secondary Kirchhoff relations: $\{V_\Sigma,I_\Sigma\}$, $\{V_\Sigma,I_\Delta\}$, $\{V_\Delta,I_\Sigma\}$, $\{V_\Delta,I_\Delta\}$.
- For 1VCCS circuits two classes can be distinguished for which either one KVL or one KCL relation is imposed. The classes are indicated as {V} and {I}.

Transfer Function Analysis

- All subclasses render different sets of solutions for the VCCS variables (no equivalences).
- All transmission parameter expression found for the graph analysis in the previous chapter 3 are also found using the classification based approach in this chapter.
- The classification is effective in reducing the analysis effort: all 145 graphs are covered by 12 expressions for the VCCS variables.

Relation between Chapter 3 and 5

- The linear transactor graphs in Appendix A contain all information of the connection of two VCCSs to a source and load (6 Kirchhoff relations). If such transactors are forced in their A-, B-, C- or D-determined mode, the solution for the VCCS variables can be found from only 2 Kirchhoff relations. A third relation defines the output. The circuits can either be classified as 2VCCS circuits or as two 1VCCS circuits.
- The class to which a certain transactor circuit belongs depends on the mode in which it is biased (A-, B-, C- or D-determined).

6

Large-Signal Characteristics of 2VCCS Circuits

6.1 Introduction

The previous chapters dealt with the generation and classification of linear transactors, based on a (small-signal) linear VCCS model of the MOST. We will now focus our attention to large-signal aspects of such circuits. The DC transfer characteristics for all classes of circuits defined in the previous chapter will be calculated in section 6.2, based on the LVCCS, SVCCS and EVCCS models defined in chapter 3. A practical circuit is biased in a certain point of this characteristic, in which it approximates the desired linear transactor behaviour. It will be assumed that this biasing is performed by means of ideal voltage and/or current sources. By changing the biasing point, tuning of transmission parameters is possible. Therefore the range of possible bias points, the operating range, of a circuit is very important and will be considered in detail in section 6.2. Boundary conditions for the validity of the generalised VCCS equations will be used to derive limits for the useful operating range. Furthermore, trade-offs between signal swing and electronic tuneability will be identified.

Another important subject of this chapter is the distortion that occurs in VCCS circuits. In section 0 this subject will be considered using a Taylor series expansion of the DC transfer characteristics in the biasing point. It will be shown that different classes of circuits show significant differences in distortion.

6.2 DC transfer Characteristics and Biasing Points

The DC transfer characteristics for the different classes of VCCS circuits will now be calculated, using the three generalised VCCS equations defined in chapter 3. First some general remarks concerning boundary conditions and signal swing limitations will be made in section 6.2.1. Then the analysis results for the 1VCCS circuits will be presented in

section 6.2.2, while the three main classes of 2VCCS circuits are discussed in the sections 6.2.3 to 6.2.5.

6.2.1 Useful Operating Range Considerations

Analog CMOS circuits are often synthesised using rather simple models for the MOS transistors. In this thesis we use the LVCCS, SVCCS and EVCCS model. Despite their inaccuracy, such simple models are useful to gain insight in design trade-offs (analytical design equations can be derived) and make a "first cut design". The generalised VCCS equations are presumed to be valid over a voltage range of V_{min} to V_{max}. The DC transfer characteristic of a VCCS circuit will not be predicted well by the models, if the VCCSs are driven beyond their validity limits. These limits often relate to operating region cross-over points. The transfer characteristic of the VCCS will often change significantly beyond these limits. This happens for instance if a transition from the saturated to the non-saturated region takes place for a MOST, so that current source behaviour is lost. As a result, the DC transfer characteristics of a VCCS circuit can bend sharply at this point, resulting in severe distortion of the output signal. Thus the validity limits of the VCCS equations can often serve as a useful basis to derive limits to the useful operating region of linear transactors. On the other hand, other requirements may be more restrictive, e.g. a distortion or noise requirement. Designers will often explore circuit properties by means of simulations. The estimation of the operating range can then serve as a means to choose the operating points for which simulations are done. Therefore, we will pay quite some attention to operating range limits based on the voltage validity limits V_{min} and V_{max} of the VCCSs.

6.2.2 1VCCS Circuits

First the DC transfer characteristics of 1VCCS circuits will be considered, as shown in Table 6-1 for an LVCCS, SVCCS and EVCCS.

Class	VCCS type	Dependent Variable	Operating Range Limits
$\{V_P\}$	LVCCS	$I_P = G \cdot (V_P - V_L) + I_L$	$V_{min,L} < V_P < V_{max,L}$
	SVCCS	$I_P = k \cdot (V_P - V_T)^2$	$V_{min,S} < V_P < V_{max,S}$
	EVCCS	$I_P = I_E \cdot e^{V_P/V_E}$	$V_{min,E} < V_P < V_{max,E}$
$\{I_P\}$	LVCCS	$V_P = V_L + \frac{I_P - I_L}{G}$	$I_L(V_{min,L}) < I_P < I_L(V_{max,L})$
	SVCCS	$V_P = V_T + \sqrt{\frac{I_P}{k}}$	$I_S(V_{min,S}) < I_P < I_S(V_{max,S})$
	EVCCS	$V_P = V_E \ln \frac{I_P}{I_E}$	$I_E(V_{min,E}) < I_P < I_E(V_{max,E})$

Table 6-1: DC transfer characteristic and operating-range limits for 1VCCS circuits with a LVCCS, SVCCS and EVCCS.

For the $\{V_P\}$ class the current is obviously equal to the linear, square-law and exponential I(V) equation of the VCCS, while for the $\{I_P\}$ class the inverse of these I(V) functions is found: a linear, square-root and logarithmic function.

The operating-range limits for the independent variable V_P or I_P are listed in the last columns of the Table 6-1. These conditions are easily found by applying the VCCS voltage boundary condition $V_{min} < V < V_{max}$.

6.2.3 2VCCS Circuits: The {V,V} Class

The DC transfer characteristics for 2VCCS circuits will now be derived, starting with the {V,V} class. The two voltage relations that are being forced in this class are:

$$V_a + \alpha_{b1} \cdot V_b = V_{ind1} \tag{6.1}$$

$$V_a + \alpha_{b2} \cdot V_b = V_{ind2} \tag{6.2}$$

with: $$\{\alpha_{b1}, \alpha_{b2}\} \in \{\{0,1\},\{0,-1\},\{1,-1\}\} \tag{6.3}$$

and V_{ind1} and V_{ind2} representing two independent voltages as in chapter 5. From the above equations V_a and V_b can easily be solved as:

$$V_a = \frac{\alpha_{b2} V_{ind1} - \alpha_{b1} V_{ind2}}{\alpha_{b2} - \alpha_{b1}} \tag{6.4}$$

$$V_b = \frac{V_{ind1} - V_{ind2}}{\alpha_{b1} - \alpha_{b2}} \tag{6.5}$$

These solutions are independent of the DC transfer characteristic of the VCCS. They are shown in Table 6-2 for the three {V,V} subclasses, together with the operating-range limits for the independent variables. The resulting solutions for the currents I_a and I_b are easily found by substitution of V_a and V_b in the I(V) equations of the VCCS. The secondary voltages and currents can be calculated as sums and differences of the solutions for the primary variables. For shortness, not all of these functions will be listed and considered in detail. However, a few cases of special interest will be discussed. The $\{V_\Sigma,V_\Delta\}$ class is one of these. From Table 6-2 we see that this case corresponds to a balanced voltage drive condition: voltage V_a and V_b have a common component $\frac{1}{2}V_\Sigma$ and a differential component $\frac{1}{2}V_\Delta$. This balanced condition is commonly used to cancel offset and even order harmonics, by using the difference of the output currents of two identical VCCSs. Thus an odd order function of V_Δ results. For the SVCCS case, the result is:

$$I_{\Delta,S} = k\left(V_\Sigma - 2V_T\right)V_\Delta \tag{6.6}$$

We see that this is a linear function from V_Δ to I_Δ, without offset. This balancing technique is often used to linearise transconductor circuits (see chapter 8), while V_Σ is used for transconductance tuning. Alternatively, the role of V_Σ and V_Δ can be exchanged, and moreover both V_Σ and V_Δ can be used as inputs to implement a multiplier [e.g. 137]. In contrast to the odd order function I_Δ, the sum I_Σ for the $\{V_\Sigma,V_\Delta\}$ class is an even order function of V_Δ. This is useful to implement a squarer with an SVCCS (e.g. for RMS-DC conversion [50]):

$$I_{\Sigma,S} = \tfrac{1}{2}k\left(V_\Sigma - 2V_T\right)^2 + \tfrac{1}{2}kV_\Delta^2 \tag{6.7}$$

This current increases with the square of V_Δ, while the usual $V_\Delta \cdot V_T$ cross-product term is cancelled. Based on squarers, multipliers can also be implemented [e.g. 142].

Class	Solution for V_a	Solution for V_b
$\{V_P,V_\Sigma\}$	$V_a = V_P$	$V_b = -V_P+V_\Sigma$
$\{V_P,V_\Delta\}$	$V_a = V_P$	$V_b = V_P-V_\Delta$
$\{V_\Sigma,V_\Delta\}$	$V_a = ½\ V_\Sigma + ½\ V_\Delta$	$V_b = ½\ V_\Sigma - ½\ V_\Delta$

Table 6-2: The solutions of the primary VCCS voltages for the {V,V} class.

Apart from the above discussed $\{V_\Sigma,V_\Delta\}$ case (and the LVCCS circuits that are obviously all linear), two other linear I(V) relations are found:

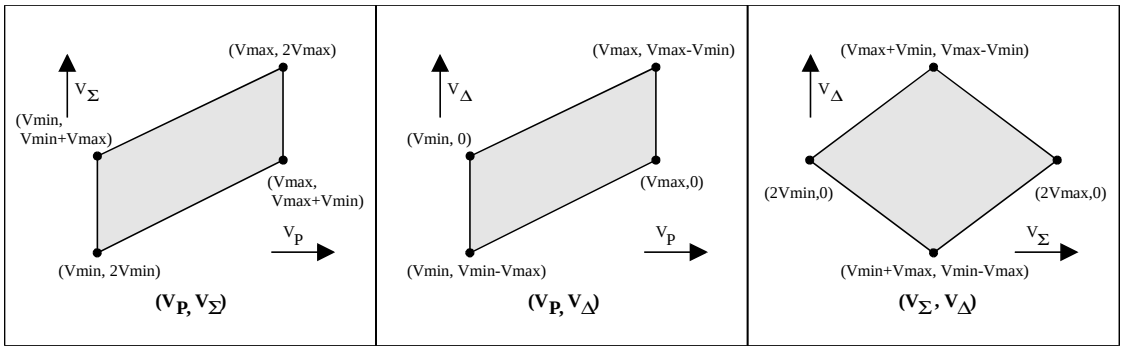
$$I_{\Delta,S} = 2k\left(V_\Sigma - 2V_T\right)V_P - k(V_\Sigma - 2V_T)V_\Sigma \tag{6.8}$$

$$I_{\Delta,S} = 2k\,V_\Delta V_P - k\left(V_\Delta + 2V_T\right)V_\Delta \tag{6.9}$$

The above equations relate to $\{V_P,V_\Sigma\}$ and $\{V_P,V_\Delta\}$ circuits and are linear in V_P, however with an offset current. They are exploited in several well-known transconductor circuits [e.g. 49, 63], using V_Σ and V_Δ for transconductance control.

Operating Range Plots

The limits of the operating range of one independent variable depend on the value of the other. Hence, these two variables can not be chosen independently. In order to show these interdependencies, a two-dimensional graphical representation of the operating range is given in Figure 6-1.



a) b) c)

Figure 6-1: Operating-range plots for the {V,V} subclasses, assuming 2 equal VCCSs (V_{min} and V_{max} are different for the LVCCS, SVCCS and EVCCS!).

The grey areas in these plots indicate the operating range of the $\{V_P,V_\Sigma\}$, $\{V_P,V_\Delta\}$ and $\{V_\Sigma,V_\Delta\}$ subclasses (Figure 6-1a, b and c respectively). Horizontally, the limits for the first variable in the subclass-name are indicated, and vertically the limits for the other variable. The resulting operating area plots have *4 characteristic points* connected by lines. In these points the *primary VCCS voltages* are at their *boundary values*. Since there are 4 possible combinations ((V_a,V_b) equal to (V_{min},V_{min}), (V_{max},V_{min}), (V_{max},V_{max}) and (V_{min},V_{max})), and

since these combination also coincide with extreme values of the secondary variables, 4 of these corner points are found for all cases. This is true for all 2VCCS subclasses, also those in the {I,I} van {V,I} class.

As the 4 above mentioned points are always there, they are useful as "anchor points" to derive and memorise the limits of the operating range. As an example we will derive them for the $\{V_P,V_\Sigma\}$ case, starting reasoning in the point where both VCCS voltages are at their lower limit. This corresponds to the point (V_{min}, $2V_{min}$), the lower left anchor point in Figure 6-1a. If V_P is increased, V_Σ must at least increase with the same amount along the lower limit of the operating area plot, otherwise V_b becomes less then V_{min}. This can be done until V_P reaches V_{max}: the lower right anchor point (V_{max},$V_{max}+V_{min}$). Still V_Σ can be increased further, resulting in the vertical line up to the upper right anchor point (V_{max},$2V_{max}$). If V_P is decreased starting from this point, V_Σ must also be reduced, otherwise V_b becomes higher then V_{max}. By doing so the upper limit of the operating plot is followed until the upper left anchor point is found: (V_{min},$V_{min}+V_{max}$). By decreasing V_Σ we will return to our starting point. Thus we can derive the limits of the operating range. For other cases this can be done in a similar way.

The operating range in terms of V_{min} and V_{max} for the {V,V} subclasses is independent of the type of VCCS. Note however, that the value of V_{min} and V_{max} is in general different for the LVCCS, SVCCS and EVCCS. Because of this, a typical weak inversion circuit will have a significantly smaller voltage range (typically in the order of 100 mVolt) than a circuit using strong inversion MOSTs (often larger than 1 Volt).

An Application Example

The operating-range plots can be used to choose biasing points for a VCCS circuit. It will be shown that design trade-offs can sometimes be derived from these pictures. As an example, we will consider the linear transconductor circuit of Figure 6-2.

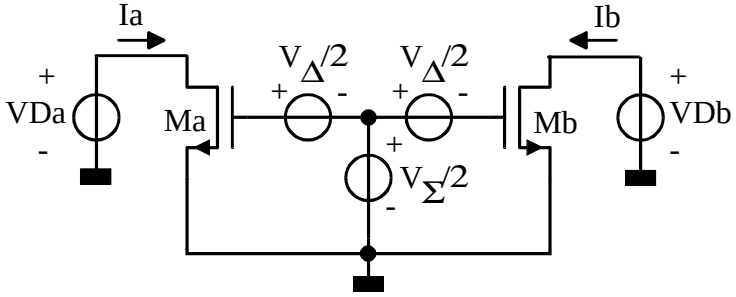


Figure 6-2: Example of a $\{V_\Sigma,V_\Delta\}$ circuit (see text).

It is assumed that MOSTs M_a and M_b operate as SVCCSs, and that V_Δ is used as input signal and V_Σ as control signal. The voltage sources with voltages $V_{Da}=V_{Db}=V_D$ model a low ohmic output circuit. They sense the difference of the output currents, which is given in eqn. 6.6. We can now use Figure 6-1c that relates to the $\{V_\Sigma,V_\Delta\}$ class. We see that the input range for V_Δ is 0 for a minimum value of V_Σ. If we take $V_{min}=V_{TN}$ and $V_{max}=V_D+V_{TN}$ as limits for the SVCCS, this corresponds to the situation that $V_\Sigma=2V_{TN}$, with both MOSTs at V_{TN} with zero current and zero transconductance. If V_Σ is increased, the transconductance $k_N(V_\Sigma-2V_{TN})$ increases linearly above zero, and the allowed input range

for V_Δ increases until the point where $V_\Sigma=2V_{TN}+V_D$ ($V_{min}+V_{max}$), with $|V_\Delta|<V_D$ ($V_{max}-V_{min}$). In the discussed range the limitation of the input swing stems from the MOST that reaches the lower voltage limit V_{TN}. If V_Σ is increased further, the input range decreases, since one of the MOSTs is driven out of saturation for gate-voltages larger than V_D+V_{TN}. From this example we see that the input signal swing depends on the transconductance value (is determined by V_Σ). If we need a certain signal swing, this results in a limitation to the transconductance tuning-range that can be achieved and vice versa.

Thus we see that the operating-range plots render insight in trade-offs between input swing and tuning-range. Note however, that this is only one criterion for defining a limit to the signal swing. Often there will be more stringent limitations, especially if a low distortion is needed. We will look at such limits in more detail in section 0.

6.2.4 2VCCS Circuits: The {I,I} Class

The derivation of the DC transfer characteristics and operating range for the {I,I} class proceeds very similar to that of the {V,V} class. Therefore it will only be discussed briefly. The important starting equations for the {I,I} class are:

$$I_a + \beta_{b1} \cdot I_b = I_{ind1} \tag{6.10}$$

$$I_a + \beta_{b2} \cdot I_b = I_{ind2} \tag{6.11}$$

where the values of the coefficients β for the subclasses $\{I_P,I_\Sigma\}$, $\{I_P,I_\Delta\}$ and $\{I_\Sigma,I_\Delta\}$ are respectively given by:

$$\{\beta_{b1},\beta_{b2}\} \in \{\{0,1\},\{0,-1\},\{1,-1\}\} \tag{6.12}$$

This results in I_a and I_b solutions equal to:

$$I_a = \frac{\beta_{b2}I_{ind1} - \beta_{b1}I_{ind2}}{\beta_{b2} - \beta_{b1}} \tag{6.13}$$

$$I_b = \frac{I_{ind1} - I_{ind2}}{\beta_{b1} - \beta_{b2}} \tag{6.14}$$

Class	Solution for I_a	Solution for I_b
$\{I_P,I_\Sigma\}$	$I_a = I_P$	$I_b = -I_P+I_\Sigma$
$\{I_P,I_\Delta\}$	$I_a = I_P$	$I_b = I_P-I_\Delta$
$\{I_\Sigma,I_\Delta\}$	$I_a = ½\ I_\Sigma + ½\ I_\Delta$	$I_b = ½\ I_\Sigma - ½\ I_\Delta$

Table 6-3: The solutions of the primary VCCS current for the {I,I} class.

The results for the different {I,I} subclasses are shown in Table 6-3. They have the same mathematical form as those for the {V,V} subclasses, with voltages replaced by currents. Again the resulting dependent voltage variables can be found by substitution. One of the results deserves mentioning, since it is often used because of the cancellation of even order distortion products: the $\{I_\Sigma,I_\Delta\}$ case. This balanced current drive condition results in odd order I-V conversion functions:

SVCCS: $$V_\Delta = \sqrt{\frac{I_\Sigma + I_\Delta}{2k}} - \sqrt{\frac{I_\Sigma - I_\Delta}{2k}} \tag{6.15}$$

EVCCS: $$V_\Delta = V_E \ln \frac{I_\Sigma + I_\Delta}{I_\Sigma - I_\Delta} \tag{6.16}$$

The operating-range plots for the {I,I} subclasses are shown in Figure 6-3. The plots have the same shape as for the {V,V} subclasses, with voltages replaced by currents.

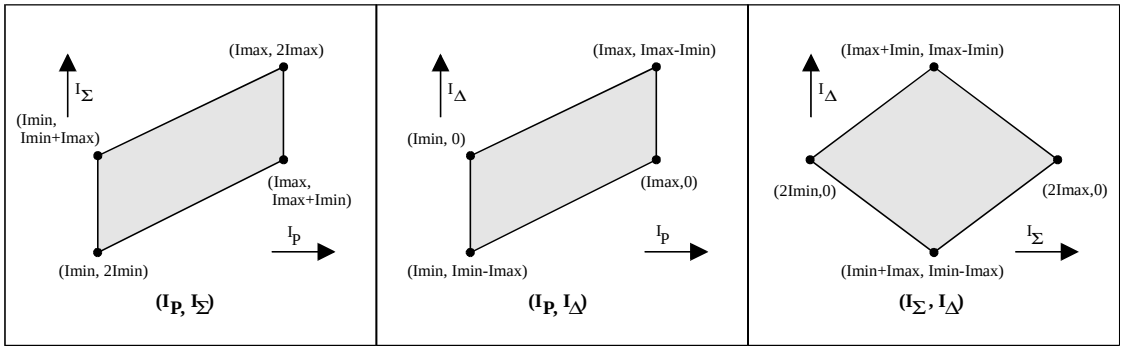


Figure 6-3: Operating-range plots for the {I,I} subclasses, assuming 2 equal VCCSs. (I_{min} and I_{max} are different for the LVCCS, SVCCS and EVCCS!).

6.2.5 2VCCS Circuits: The {V,I} Class

For the {V,I} class, one voltage and one current relation are forced given by:

$$V_a + \alpha_b \cdot V_b = V_{ind} \tag{6.17}$$

$$I_a + \beta_b \cdot I_b = I_{ind} \tag{6.18}$$

where the coefficient α_b and β_b take values depending on the subclass:

$$\{\alpha_b, \beta_b\} \in \left\{ \begin{matrix} \{0,1\}, \{0,-1\}, \{1,0\}, \{-1,0\} \\ \{1,1\}, \{1,-1\}, \{-1,1\}, \{-1,-1\} \end{matrix} \right\} \tag{6.19}$$

In contrast to the {V,V} and {I,I} class cases, the primary variables can not be solved directly from the Kirchhoff relations. At least one I(V) equation of a VCCS is also needed. Since the I(V) equations are different for the 3 generalised VCCSs, the solutions are also different. Furthermore, the non-linear SVCCS and EVCCS equations sometimes result in 2 solutions. The boundary condition for the VCCS voltage, $V_{min} < V < V_{max}$, is then applied to select a valid one. The resulting solutions for V_a and V_b for the LVCCS, SVCCS and EVCCS are presented in Table 6-4, Table 6-5 and Table 6-6 respectively. The other primary and secondary variables can be derived from them rather easily and will only be discussed for some special cases. Since linear circuits are often designed using matched devices, and since this simplifies the equations, equal VCCSs were assumed.

LVCCS

Unfortunately, using 2 equal LVCCSs does not lead to a unique solution for the $\{V_\Sigma, I_\Sigma\}$ and $\{V_\Delta, I_\Delta\}$ subclasses. Only for unequal G-values, a unique solution is found for these two cases. For V_a, the solution for the $\{V_\Sigma, I_\Sigma\}$ and $\{V_\Delta, I_\Delta\}$ cases are:

$$V_a = \frac{G_b}{G_b - G_a} V_\Sigma - \frac{I_\Sigma}{G_b - G_a} - \frac{G_a V_{La} + G_b V_{Lb} - I_{Lb} - I_{La}}{G_b - G_a} \tag{6.20}$$

$$V_a = \frac{G_b}{G_b - G_a} V_\Delta - \frac{I_\Delta}{G_b - G_a} - \frac{G_a V_{La} - G_b V_{Lb} + I_{Lb} - I_{La}}{G_b - G_a} \tag{6.21}$$

For the other 6 cases the solutions can be found in Table 6-4. As might be expected these are linear functions of the independent variables. In some cases, the offset terms with V_L and I_L cancel, which is often desired.

Subclass	**Solution for V_a** **($V_{min,L} < V_a < V_{max,L}$)**	**Solution for V_b** **($V_{min,L} < V_b < V_{max,L}$)**
$\{V_P,I_\Sigma\}$	$V_a = V_P$	$V_b = -V_P + \frac{I_\Sigma - 2I_L}{G} + 2V_L$
$\{V_P,I_\Delta\}$	$V_a = V_P$	$V_b = V_P - \frac{I_\Delta}{G}$
$\{V_\Sigma,I_P\}$	$V_a = \frac{I_P - I_L}{G} + V_L$	$V_b = V_\Sigma - \frac{I_P - I_L}{G} - V_L$
$\{V_\Delta,I_P\}$	$V_a = \frac{I_P - I_L}{G} + V_L$	$V_b = -V_\Delta + \frac{I_P - I_L}{G} + V_L$
$\{V_\Sigma,I_\Sigma\}$	no unique solution (see text)	no unique solution (see text)
$\{V_\Sigma,I_\Delta\}$	$V_a = \frac{1}{2}V_\Sigma + \frac{1}{2}\frac{I_\Delta}{G}$	$V_b = \frac{1}{2}V_\Sigma - \frac{1}{2}\frac{I_\Delta}{G}$
$\{V_\Delta,I_\Sigma\}$	$V_a = \frac{1}{2}V_\Delta + \frac{1}{2}\frac{I_\Sigma - 2I_L}{G} + V_L$	$V_b = -\frac{1}{2}V_\Delta + \frac{1}{2}\frac{I_\Sigma - 2I_L}{G} + V_L$
$\{V_\Delta,I_\Delta\}$	no unique solution (see text)	no unique solution (see text)

Table 6-4: The solution for the LVCCS voltages V_a and V_b for the {V,I} subclasses (equal LVCCSs).

SVCCS

For the SVCCS, the results are shown in Table 6-5. In contrast to the LVCCS case, the $\{V_\Delta,I_\Delta\}$ case now does have a unique solution. Now, the $\{V_\Sigma,I_\Sigma\}$ subclass does not render a unique solution, but instead has two possible solutions. In a practical circuit, it is possible to disable one of these.

Several useful functions are possible, e.g. linear I-V conversion:

$$V_\Delta = \frac{I_\Delta}{k\left(V_\Sigma - 2V_T\right)} \qquad (\{V_\Sigma,I_\Delta\}) \tag{6.22}$$

and:
$$V_\Sigma = 2V_T + \frac{I_\Delta}{kV_\Delta} \qquad (\{V_\Delta,I_\Delta\}) \tag{6.23}$$

These functions constitute the inverse of the V-I conversion functions found for I_Δ for the $\{V_\Sigma, V_\Delta\}$ class. Other linear functions $V_P(I_\Delta)$ exist for the $\{V_\Sigma,I_\Delta\}$ and $\{V_\Delta,I_\Delta\}$ subclasses and are inverse functions of $I_\Delta(V_P)$ for the $\{V_P, V_\Sigma\}$ and $\{V_P, V_\Delta\}$ subclasses. Another transfer characteristic worth mentioning is the $\{V_\Delta, I_\Sigma\}$ subclass, to which the differential pair belongs:

$$I_\Delta = V_\Delta \sqrt{2kI_\Sigma - k^2 V_\Delta^2} \tag{6.24}$$

Although often used as is, this equation can be linearised by enforcing:

$$I_\Sigma = I_{\Sigma 0} + \tfrac{1}{2} k V_\Delta^2 \tag{6.25}$$

so that an ideally linear V-I conversion results:

$$I_\Delta = V_\Delta \sqrt{2kI_{\Sigma 0}} \tag{6.26}$$

Subclass	**Solution for V_a** **($V_{min,S} < V_a < V_{max,S}$)**	**Solution for V_b** **($V_{min,S} < V_b < V_{max,S}$)**
$\{V_P,I_\Sigma\}$	$V_a = V_P$	$V_b = V_T + \sqrt{\frac{I_\Sigma}{k} - (V_P - V_T)^2}$
$\{V_P,I_\Delta\}$	$V_a = V_P$	$V_b = V_T + \sqrt{(V_P - V_T)^2 - \frac{I_\Delta}{k}}$
$\{V_\Sigma,I_P\}$	$V_a = V_T + \sqrt{\frac{I_P}{k}}$	$V_b = V_\Sigma - V_T - \sqrt{\frac{I_P}{k}}$
$\{V_\Delta,I_P\}$	$V_a = V_T + \sqrt{\frac{I_P}{k}}$	$V_b = V_T - V_\Delta + \sqrt{\frac{I_P}{k}}$
$\{V_\Sigma,I_\Sigma\}$	$V_a = \frac{1}{2} V_\Sigma \mp \frac{1}{2} \sqrt{\frac{2I_\Sigma}{k} - (V_\Sigma - 2V_T)^2}$	$V_b = \frac{1}{2} V_\Sigma \pm \frac{1}{2} \sqrt{\frac{2I_\Sigma}{k} - (V_\Sigma - 2V_T)^2}$
$\{V_\Sigma,I_\Delta\}$	$V_a = \frac{1}{2} V_\Sigma + \frac{1}{2} \frac{I_\Delta}{k(V_\Sigma - 2V_T)}$	$V_b = \frac{1}{2} V_\Sigma - \frac{1}{2} \frac{I_\Delta}{k(V_\Sigma - 2V_T)}$
$\{V_\Delta,I_\Sigma\}$	$V_a = V_T + \frac{1}{2} V_\Delta + \frac{1}{2} \sqrt{\frac{2I_\Sigma}{k} - V_\Delta^2}$	$V_b = V_T - \frac{1}{2} V_\Delta + \frac{1}{2} \sqrt{\frac{2I_\Sigma}{k} - V_\Delta^2}$
$\{V_\Delta,I_\Delta\}$	$V_a = V_T + \frac{1}{2} V_\Delta + \frac{1}{2} \frac{I_\Delta}{kV_\Delta}$	$V_b = V_T - \frac{1}{2} V_\Delta + \frac{1}{2} \frac{I_\Delta}{kV_\Delta}$

Table 6-5: The solution for the SVCCS voltages V_a and V_b for the {V,I} subclasses (equal SVCCSs).

Non-linear functions are also possible, e.g. a squarer and square-root function on currents:

$$I_\Sigma = \frac{I_\Delta^2}{2k(V_\Sigma - 2V_T)^2} + \tfrac{1}{2} k (V_\Sigma - 2V_T)^2 \qquad (\{V_\Sigma,I_\Delta\}) \tag{6.27}$$

$$I_\Sigma = \frac{I_\Delta^2}{2kV_\Delta^2} + \tfrac{1}{2} k V_\Delta^2 \qquad (\{V_\Delta,I_\Delta\}) \tag{6.28}$$

$$I_\Delta = 2V_\Delta \sqrt{kI_a} - kV_\Delta^2 \qquad (\{V_\Delta,I_P\}) \tag{6.29}$$

These proportionality factor in these functions is electronically controllable by V_Σ or V_Δ.

EVCCS

For the EVCCS the solutions are shown in Table 6-6. As for the SVCCS, the $\{V_\Sigma,I_\Sigma\}$ subclass has two solutions, but this does not necessarily exclude its use.

Class	Solution for V_a ($V_{min,E} < V_a < V_{max,E}$)	Solution for V_b ($V_{min,E} < V_b < V_{max,E}$)
$\{V_P,I_\Sigma\}$	$V_a = V_P$	$V_b = V_E \ln(\frac{I_\Sigma}{I_E} - e^{V_P/V_E})$
$\{V_P,I_\Delta\}$	$V_a = V_P$	$V_b = V_E \ln(-\frac{I_\Delta}{I_E} + e^{V_P/V_E})$
$\{V_\Sigma,I_P\}$	$V_a = V_E \ln\frac{I_P}{I_E}$	$V_b = V_\Sigma - V_E \ln\frac{I_P}{I_E}$
$\{V_\Delta,I_P\}$	$V_a = V_E \ln\frac{I_P}{I_E}$	$V_b = -V_\Delta + V_E \ln\frac{I_P}{I_E}$
$\{V_\Sigma,I_\Sigma\}$	$V_a = V_E \ln\left(\frac{I_\Sigma}{2I_E} \pm \sqrt{\frac{I_\Sigma^2}{4I_E^2} - e^{V_\Sigma/V_E}}\right)$	$V_b = V_E \ln\left(\frac{I_\Sigma}{2I_E} \mp \sqrt{\frac{I_\Sigma^2}{4I_E^2} - e^{V_\Sigma/V_E}}\right)$
$\{V_\Sigma,I_\Delta\}$	$V_a = V_\Sigma - V_E \ln\left(-\frac{I_\Delta}{2I_E} + \sqrt{\frac{I_\Delta^2}{4I_E^2} - e^{V_\Sigma/V_E}}\right)$	$V_b = V_E \ln\left(-\frac{I_\Delta}{2I_E} + \sqrt{\frac{I_\Delta^2}{4I_E^2} - e^{V_\Sigma/V_E}}\right)$
$\{V_\Delta,I_\Sigma\}$	$V_a = V_\Delta + V_E \ln\left(\frac{I_\Sigma}{I_E(1+e^{V_\Delta/V_E})}\right)$	$V_b = V_E \ln\left(\frac{I_\Sigma}{I_E(1+e^{V_\Delta/V_E})}\right)$
$\{V_\Delta,I_\Delta\}$	$V_a = V_\Delta + V_E \ln\left(\frac{I_\Delta}{I_E(-1+e^{V_\Delta/V_E})}\right)$	$V_b = V_E \ln\left(\frac{I_\Delta}{I_E(-1+e^{V_\Delta/V_E})}\right)$

Table 6-6: The solution for the EVCCS voltages V_a and V_b for the {V,I} subclasses (equal EVCCSs).

Now, some linear DC transfer characteristics from current to current are found, e.g.:

$$I_b = e^{-V_\Delta/V_E} \cdot I_a \qquad (\{V_\Delta, I_P\}) \qquad (6.30)$$

which is known in a BJT implementation as a voltage-controlled gain-stage, and:

$$I_b = \frac{1}{1+e^{V_\Delta/V_E}} I_\Sigma \qquad (\{V_\Delta, I_\Sigma\}) \qquad (6.31)$$

which is known as a linear current-attenuation stage e.g. for AGC [13]. Furthermore, multiplication and division operations are possible. An example of division is:

$$I_b = \frac{I_E^2 e^{V_\Sigma/V_E}}{I_a} \qquad (\{V_\Sigma, I_P\}) \qquad (6.32)$$

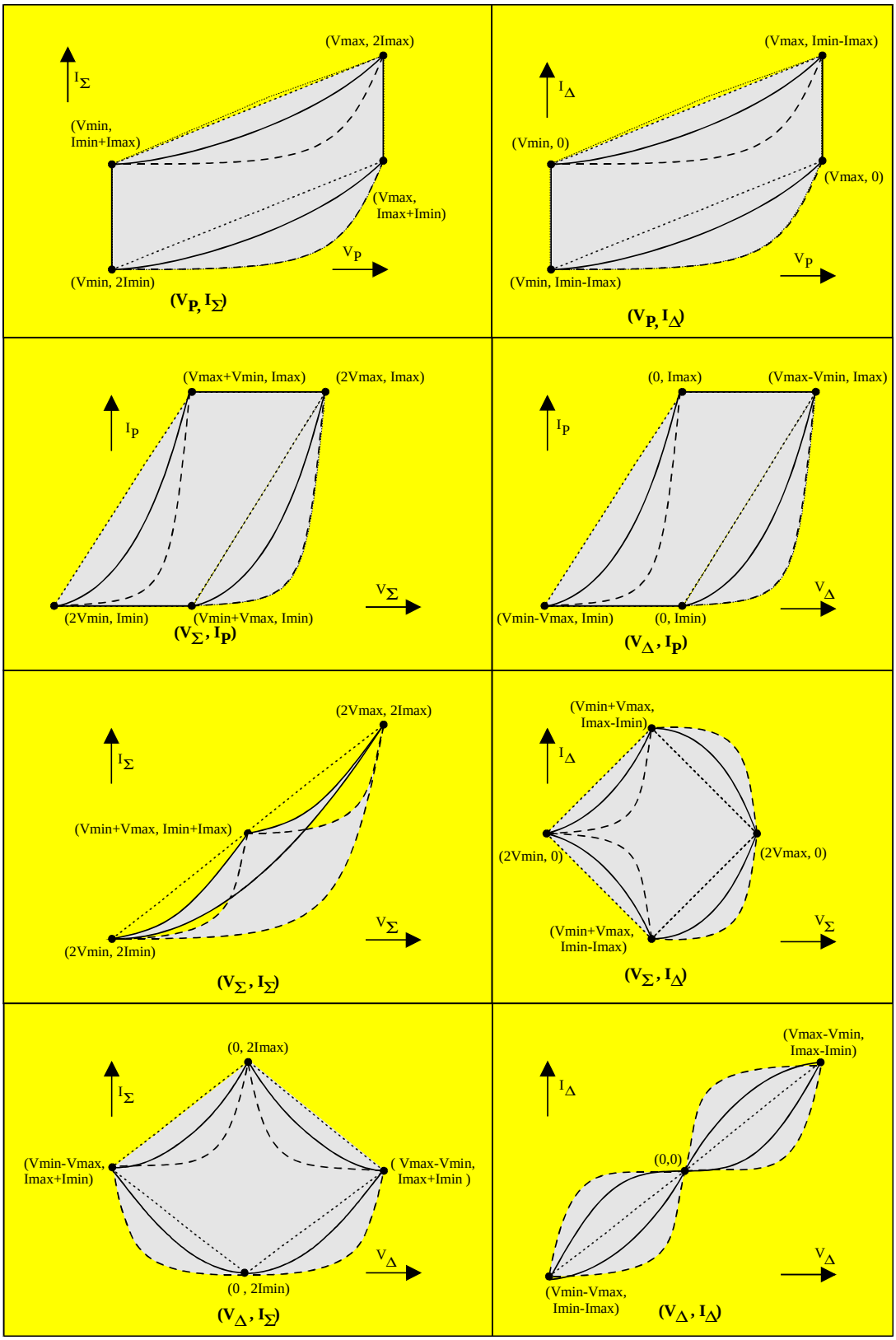


Figure 6-4: Operating-range plots for the {V,I} subclasses (2 equal VCCSs). Dotted, drawn and dashed lines relate to LVCCS, SVCCS and EVCCS. Note that the value of V_{min}, V_{max} , I_{min} and I_{max} depends on the type of VCCS.

Operating-range Plots

As for the {V,V} and {I,I} class, we would like to generate operating range plots. Since different solutions are found for different types of VCCSs, this is less straightforward as for the {V,V} and {I,I} class. Fortunately the anchor points derived from different V-limit combinations (see section 6.2.3) also exist for the {V,I} circuits. By means of numerical simulations with data from Table 3.7, the plots of Figure 6-4 were derived. The anchor point are again indicated in terms of V_{min}, V_{max}, I_{min} and I_{max}. Note that these boundary values depend on the specific VCCS implementation. Dotted, drawn and dashed boundary lines are used for the LVCCS, SVCCS and EVCCS, repectively. Now the limits of the operating range are only straight lines for the LVCCS. For the SVCCS and EVCCS non-linear boundary lines are found. The lines for the SVCCS lie between those of the LVCCS and EVCCS.

The operating-range plots of Figure 6-4 help to determine trade-offs between input range and tuning range. Furthermore, it can be seen that the $\{V_\Sigma,I_\Sigma\}$ and $\{V_\Delta,I_\Delta\}$ cases have no solution for an LVCCS: to satisfy the boundary conditions, the two variables have to be chosen linearly dependent (straight dotted lines in Figure 6-4). Hence, the input and control signal can not be chosen independently as is required. In contrast, a valid operating range does exist for the SVCCS and EVCCS. More precisely, 2 valid operating range areas exist for the $\{V_\Delta,I_\Delta\}$ case.

6.3 Distortion in 2VCCS Circuits

In the previous sections limits for the operating range of 1VCCS and 2VCCS circuits have been derived, based on VCCS model validity limits. If driven beyond these limits, the output signal is usually severely distorted. However, most circuits already show significant distortion before reaching the operating range limits. The distortion requirements for linear transactors depend on the application, but are typically in the range of 0.01% to 1% (THD). The corresponding non-linearity is hardly visible from a plot of the DC transfer characteristic, and this operating range is often referred to as the "weakly non-linear" region. The distortion is commonly evaluated by means of a Taylor series approximation of the transfer characteristic of a transactor. Usually the 2^{nd} and 3^{rd} order distortion are the most important. These distortion products are mainly determined by the 2^{nd} and 3^{rd} order Taylor series terms [15], so that a third order Taylor series will be used to model the distortion of transactors.

We can find the non-linearity of individual circuits directly from their DC transfer characteristics. However, a more general approach will be adopted based on the classification proposed in the previous chapter. The non-linearity for every class will be expressed analytically in terms of the Taylor coefficients of the constituting VCCSs. In this way the results can be presented in a compact form, while simple substitutions yield the results for different VCCS models. Moreover, an *explicit relation* between the non-linearity of a VCCS and that of a VCCS circuit is thus found, *providing insight* in the effect of circuit topology on distortion. Another important reason for the above mentioned approach is the inaccuracy of the generalised VCCS equations. This makes them often inappropriate for distortion or transconductance estimations. This is especially true for submicron

MOSTs with severe second order effects. On the other hand, more complex equations are not tractable for DC transfer characteristic calculations, as done in the previous sections. As a compromise we will use the LVCCS, SVCCS and EVCCS equations to estimate the biasing point. However, the transconductance and non-linear terms will be analysed using more refined models. Although there is a modelling inconsistency in this approach, it is justified by the observation that the derivatives of the VCCS current are much more sensitive to details of the VCCS equation than the VCCS current itself. Therefore, neglecting second order effects is less harmful for biasing points estimations than for transconductance and distortion calculations.

The analysis of the distortion of VCCS circuits will now be discussed in more detail.

6.3.1 Taylor Series and Intercept Point Definitions

During analysis, a third order Taylor series model for a VCCS will be used, describing the effect of a voltage excursion v from the bias point on the current excursion i as:

$$i \cong i_{t3} = g_1 \cdot v + g_2 \cdot v^2 + g_3 \cdot v^3 \tag{6.33}$$

where g_1, g_2 and g_3 are the Taylor coefficients of the DC I(V) transfer characteristic of the VCCS, calculated in its biasing point (V_0,I_0):

$$g_1 = \left.\frac{dI}{dV}\right|_{V=V_0} \qquad g_2 = \left.\frac{1}{2!}\cdot\frac{d^2I}{dV^2}\right|_{V=V_0} \qquad g_3 = \left.\frac{1}{3!}\cdot\frac{d^3I}{dV^3}\right|_{V=V_0} \tag{6.34a,b,c}$$

In these equations coefficient g_1 is the transconductance g of the MOST. Index 1 is added to distinguish clearly between the 1st, 2nd and 3rd order coefficients. The coefficients of 2 different VCCSs will be indicated by index a and b, as in previous chapters. Hence, g_{1b} and g_b are synonyms.

Apart from the i(v) relation, the inverse relation v(i) will be needed to solve the non-linear equations for the {V,I} and {I,I} class. These can be calculated by postulating a solution $v_{t3}(i)$, expressed as a Taylor series, and substituting this in eqn. 6.33: $i_{t3}(v=v_{t3}(i))$. Since the inverse of a function that has been applied to a variable should render the original variable, the Taylor coefficients up to the third order should be such that $i_{t3}(v_{t3}(i))=i$ is satisfied [129]. Applying this to a single VCCS, we can postulate the following inverse Taylor series:

$$v \cong v_{t3} = r_1 \cdot i + r_2 \cdot i^2 + r_3 \cdot i^3 \tag{6.35}$$

Substituting eqn. 6.35 in eqn. 6.33, collecting terms of equal order up to the 3rd order, and putting the solution equal to i results in:

$$i = g_1 \cdot r_1 \cdot i + \left(g_1 \cdot r_2 + g_2 \cdot r_1^2\right)\cdot i^2 + \left(g_1 \cdot r_3 + 2 \cdot g_2 \cdot r_1 \cdot r_2 + g_3 \cdot r_1^3\right)\cdot i^3 \tag{6.36}$$

By equating the i-terms and equating the coefficients of the i^2- and i^3-terms to zero, the following relations between r_i and g_i are found:

$$r_1 = \frac{1}{g_1} \quad r_2 = -\frac{g_2}{g_1^3} \qquad r_3 = \frac{2 \cdot g_2^2 - g_1 \cdot g_3}{g_1^5} \tag{6.37a,b,c}$$

These relations are identical to the relation found in [54], derived using a more general mathematical derivation.

Basically, the above described procedure results in an approximate solution for x in y(x), where y(x) is a power-series in x, and the solution for x is a power-series in y. This method will also be used to find a solution for the non-linear transfer function of the different classes of VCCS circuits, needed in section 6.6.

For weakly non-linear circuits the relation between the 2nd and 3rd order harmonic distortion HD2 and HD3 and the Taylor coefficients can be approximated by [15]:

$$HD2 \cong \frac{1}{2} \cdot \frac{a_{t2}}{a_{t1}} \cdot \hat{s}_{in} \tag{6.38}$$

$$HD3 \cong \frac{1}{4} \cdot \frac{a_{t3}}{a_{t1}} \cdot \hat{s}_{in}^2 \tag{6.39}$$

where $\hat{s}_{in}$ is the amplitude of the input sine-wave signal, and a_{t1}, a_{t2} and a_{t3} are the 1st, 2nd and 3rd order Taylor coefficients of the transactance. Other distortion specifications like IMD and differential error can also be expressed in terms of Taylor coefficients.

Usually, a maximum allowed distortion level at a given signal level is specified, e.g. <1% HD3 at 100mV input voltage. In the region where eqn. 6.38 and eqn. 6.39 are valid, the relation between signal amplitude and distortion is known. Thus extrapolation to a normalized condition of 100% distortion is possible, as is commonly done when defining intercept points. By equating the expressions for HD2 and HD3 and taking absolute values, the following relations for intercept voltages and currents are found:

$$V_{IP2} = 2|g_1|/|g_2| \qquad V_{IP3} = 2\sqrt{|g_1|/|g_3|} \tag{6.40a,b}$$

$$I_{IP2} = 2|r_1|/|r_2| \qquad I_{IP3} = 2\sqrt{|r_1|/|r_3|} \tag{6.41a,b}$$

In the next section these relations will be evaluated for different MOST VCCS models.

6.3.2 Distortion in Single MOST VCCSs

In order to get a notion of distortion properties of single VCCSs, the Taylor coefficients and intercept points for the 3 generalised VCCS models will be evaluated. Table 6-7 shows their Taylor coefficients.

Obviously, the LVCCS has zero second and third order Taylor coefficients, while the SVCCS has a zero g_3-coefficient. However, practical VCCS implementations show non-linearity, and we have to refine our model to find at least a first order estimate. It is well-known from literature that mobility reduction in MOSTs is the main source of distortion in triode and "square-law" MOST transconductors. As discussed in chapter 3, the θ-model will be used for both a MOST in the triode and saturation region. These models will be referred to as the LVCCSθ and SVCCSθ model, denoted with indices Lθ and Sθ. Their Taylor coefficients are shown in Table 6-8.

Taylor coefficient	LVCCS	SVCCS	EVCCS
g_1	G	$2\,k\,(V_0 - V_T) = 2\sqrt{k\,I_0}$	$\frac{I_E\,e^{V_0/V_E}}{V_E} = \frac{I_0}{V_E}$
g_2	0	k	$\frac{I_E\,e^{V_0/V_E}}{2\,V_E^2} = \frac{I_0}{2\,V_E^2}$
g_3	0	0	$\frac{I_E\,e^{V_0/V_E}}{6\,V_E^3} = \frac{I_0}{6\,V_E^3}$
r_1	1/G	$\frac{1}{2\,k\,(V_0 - V_T)} = \frac{1}{2\sqrt{k\,I_0}}$	$\frac{V_E}{I_E\,e^{V_0/V_E}} = \frac{V_E}{I_0}$
r_2	0	$-\frac{1}{8k^2\,(V_0 - V_T)^3} = -\frac{1}{8I_0\sqrt{k\,I_0}}$	$-\frac{V_E}{2I_E^2\,e^{2V_0/V_E}} = -\frac{V_E}{2I_0^2}$
r_3	0	$\frac{1}{16\,k^3\,(V_0 - V_T)^5} = \frac{1}{16\,I_0^2\sqrt{k\,I_0}}$	$\frac{V_E}{3I_E^3\,e^{3V_0/V_E}} = \frac{V_E}{3I_0^3}$

Table 6-7: Taylor coefficients for the 3 generalised VCCS models.

Taylor coefficient	LVCCSθ	SVCCSθ
g_1	$\frac{kV_{DS}(2+\theta V_{DS})}{(1+\theta(V_0 - V_T))^2} \approx 2kV_{DS} = G$	$\frac{k(V_0 - V_T)(2+\theta(V_0 - V_T))}{(1+\theta(V_0 - V_T))^2} \approx 2\,k\,(V_0 - V_T)$
g_2	$-\frac{kV_{DS}\theta(2+\theta V_{DS})}{(1+\theta(V_0 - V_T))^3} \approx -G\theta$	$\frac{k}{(1+\theta(V_0 - V_T))^3} \approx k$
g_3	$\frac{kV_{DS}\theta^2(2+\theta V_{DS})}{(1+\theta(V_0 - V_T))^4} \approx G\theta^2$	$-\frac{k\theta}{(1+\theta(V_0 - V_T))^4} \approx -k\theta$
r_1	$\frac{(1+\theta(V_0 - V_T))^2}{kV_{DS}(2+\theta V_{DS})} \approx \frac{1}{G}$	$\approx \frac{1}{2k(V_0 - V_T)}$
r_2	$\frac{\theta(1+\theta(V_0 - V_T))^3}{k^2V_{DS}^2(2+\theta V_{DS})^2} \approx \frac{\theta}{G^2}$	$\approx -\frac{1}{8k^2\,(V_0 - V_T)^3}$
r_3	$\frac{\theta^2(1+\theta(V_0 - V_T))^4}{k^3V_{DS}^3(2+\theta V_{DS})^3} \approx \frac{\theta^2}{G^3}$	$\approx \frac{1}{16\,k^3\,(V_0 - V_T)^4}\left(\frac{1}{V_0 - V_T} + \theta\right)$

Table 6-8: Taylor coefficients for a triode and saturated strong inversion MOST, modelled with a LVCCS and SVCCS equation, divided by $(1+\theta(V_0-V_T))$.

Looking at the results of table Table 6-7 and Table 6-8 two interesting notes can be made on the bias dependence of the Taylor coefficients:

1. The EVCCS and LVCCSθ have Taylor coefficients g_1, g_2 and g_3 that depend on biasing in the same way: all g-coefficients are proportional to I_0 for the EVCCS and LVCCSθ (G is proportional to I_0).
2. The SVCCSθ model, has a g_1-term that depends linearly on V_0. However, the g_2- and g_3-term are independent of V_0 in first order approximation.

The notes above can help to find a first order estimate for the distortion properties of a VCCS circuit. Substituting the values of the tables above in eqn. 6.40 and eqn. 6.41, the expressions for the intercept voltages and currents shown in Table 6-9 are found.

VCCS type	V_{IP2}	V_{IP3}	I_{IP2}	I_{IP3}
LVCCS	∞	∞	∞	∞
SVCCS	$4\left(V_0 - V_T\right)$	∞	$8I_0$	$4\sqrt{2}\,I_0$
EVCCS	$4V_E$	$2\sqrt{6}V_E$	$4I_0$	$2\sqrt{3}\,I_0$
LVCCSθ	$\frac{2}{\theta}$	$\frac{2}{\theta}$	$G\frac{2}{\theta} \approx \frac{I_0 - I_L}{V_0 - V_L}\frac{2}{\theta}$	$G\frac{2}{\theta} \approx \frac{I_0 - I_L}{V_0 - V_L}\frac{2}{\theta}$
SVCCSθ	$4\left(V_0 - V_T\right)$	$2\sqrt{2}\sqrt{\frac{V_0 - V_T}{\theta}}$	$8I_0$	$4\sqrt{2}\,I_0$

Table 6-9: 2nd and 3rd order intercept voltages and currents for the VCCS models.

To get a notion of practical achievable values, Table 6-10 shows numerical values for a 1μCMOS process. Looking at the results of Table 6-9 and Table 6-10, the following observations can be made:

- A MOST in weak inversion has a significantly smaller intercept voltage than in strong inversion. The second and third order intercept voltages are 4, respectively 5 times V_E, and are bias independent.
- The triode MOST has equal second and third order intercept voltages, which are bias independent, and inversely proportional to θ.
- The saturated MOST has a *second* order intercept voltage proportional to V_0-V_T (the effective gate-source voltage V_{GT}). Its value is between that of a weak inversion and a triode MOST for the case of a 1μCMOS process.
- The saturated MOST has a *third* order intercept voltage proportional to the square-root of V_{GT}/θ. Its value is an order of magnitude higher than for a weak inversion MOST, however somewhat smaller than for a triode MOST. However, the advantage of a triode MOST over a saturated MOST is lost for high values of θ.
- The intercept currents vary between 3.5 and 13 times I_0. Again the triode MOST has the highest value, followed by the saturated strong inversion MOST and weak inversion MOST. However, the differences between different VCCS models are much less pronounced than for intercept voltages.

Transconductor Implementation	V_{IP2}	V_{IP3}	I_{IP2}	I_{IP3}
Triode MOST (LVCCSθ)	13	13	$13I_0$	$13I_0$
Strong inversion, saturated MOST (SVCCSθ)	0.4..8.0	2.3...10	$8I_0$	$5.7I_0$
Weak inversion (EVCCS)	0.16	0.20	$4I_0$	$3.5I_0$

Table 6-10: Typical values for 2nd and 3rd order intercept voltages and currents for CMOS VCCS implementations (1μCMOS, see Table 3.7).

6.3.3 Distortion Analysis of 2VCCS Circuits

The attention will now be focussed on circuits with 2 VCCSs and the analysis of their distortion. The main question that serves as a guideline for the discussion is: can distortion be decreased by using 2 VCCSs instead of 1?

In general, the Taylor coefficients of the 2 VCCSs will be different, unless the VCCSs are equal and are biased in the same biasing point. Non-linearity cancellation may occur in this case. Alternatively, sometimes a certain ratio between Taylor coefficients of 2 VCCSs is needed to achieve a non-linearity cancellation. To cover these cases, and to make the analysis results more generally applicable, it is useful to allow for different Taylor coefficients for the two VCCSs (index a and b). Unfortunately, this leads to very complex analytical expressions, which are hard to interpret for a human. Nevertheless, simple first order analytical expressions are very much desired to gain insight in the distortion behaviour of VCCS circuits. In order to arrive at *manageable expressions*, the following *simplifying assumptions* will be used:

$$\begin{aligned} g_{1a} &= g_1 \quad g_{1b} = m \cdot g_1 \\ g_{2a} &= g_2 \quad g_{2b} = m \cdot g_2 \\ g_{1a} &= g_3 \quad g_{3b} = m \cdot g_3 \end{aligned} \qquad (6.42a,b,c,d,e,f)$$

where g_1, g_2 and g_3 are given by 6.34a,b,c. The *ratio* between g_{ia} and g_{ib} of *1:m* occurs if $VCCS_b$ consists of *m parallel-connected* copies of $VCCS_a$, all biased at *the same voltage*. If an accurate g_i-ratio is needed, this implementation that relies on matching of identical circuits is preferred. The r-coefficients corresponding to these assumption can be derived using eqn. 6.37:

$$\begin{aligned} r_{1a} &= r_1 \quad r_{1b} = r_1 / m \\ r_{2a} &= r_2 \quad r_{2b} = r_2 / m^2 \\ r_{3a} &= r_3 \quad r_{3b} = r_3 / m^3 \end{aligned} \qquad (6.43a,b,c,d,e,f)$$

Using the above mentioned assumptions, the Taylor coefficients of the transfer characteristic of 1VCCS and 2VCCS circuits will now be calculated in terms of the Taylor coefficients of the VCCSs.

6.4 The {V} and {V,V} Class

For the {V,V} class, both input variables are voltages. The relevant output variables are currents (see the solution for the {V,V} class in chapter 5). The Taylor coefficients for the VCCS currents are easily found in 2 steps:

- Express the VCCS voltages as a function of the input voltage v_{in} (and v_c=0).
- Substitute the VCCS voltage expressions in eqn. 6.33 to find the VCCS currents.

The Taylor coefficients of the resulting currents are listed in Table 6-11.

Class	Input variable v_{in}	Output variable i_{out}	linear coefficient	second order coefficient	third order coefficient
$\{V_P\}$	v_p	i_p	g_1	g_2	g_3
$\{V_P,V_\Sigma\}$	v_a (v_Σ=0)	i_a	g_1	g_2	g_3
		i_b	$-m\cdot g_1$	$m\cdot g_2$	$-m\cdot g_3$
	v_Σ (v_a=0)	i_a	0	0	0
		i_b	$m\cdot g_1$	$m\cdot g_2$	$m\cdot g_3$
$\{V_P,V_\Delta\}$	v_a (v_Δ=0)	i_a	g_1	g_2	g_3
		i_b	$m\cdot g_1$	$m\cdot g_2$	$m\cdot g_3$
	v_Δ (v_a = 0)	i_a	0	0	0
		i_b	$-m\cdot g_1$	$m\cdot g_2$	$-m\cdot g_3$
$\{V_\Sigma,V_\Delta\}$	v_Σ (v_Δ = 0)	i_a	$\frac{1}{2}\cdot g_1$	$\frac{1}{4}\cdot g_2$	$\frac{1}{8}\cdot g_3$
		i_b	$m\cdot\frac{1}{2}\cdot g_1$	$m\cdot\frac{1}{4}\cdot g_2$	$m\cdot\frac{1}{8}\cdot g_3$
	v_Δ (v_Σ = 0)	i_a	$\frac{1}{2}\cdot g_1$	$\frac{1}{4}\cdot g_2$	$\frac{1}{8}\cdot g_3$
		i_b	$-m\cdot\frac{1}{2}\cdot g_1$	$m\cdot\frac{1}{4}\cdot g_2$	$-m\cdot\frac{1}{8}\cdot g_3$

Table 6-11: Taylor coefficients of the VCCS currents, for the {V} and {V,V} classes.

Comparing the results of Table 6-11 with those of a single VCCS, we see that the sign is different for the $\{V_P,V_\Sigma\}$ and $\{V_P,V_\Delta\}$ classes. Furthermore, sometimes zero coefficients occur, if V_P is the control variable (v_P=0). For the $\{V_\Sigma,V_\Delta\}$ case, basically also coefficients g_i are found ($i \in \{1,2,3\}$), but with a scale factor $(½)^i$, since the input voltage swing of the VCCS is $½\cdot V_\Delta$. For all subclasses, the sign of the Taylor coefficients of $VCCS_a$ is positive. This also holds for the second order coefficient of $VCCS_b$. However, the first and third order coefficient of i_b can also be negative. This difference results from the square-law term, that always renders a positive result in contrast to the linear and third order terms. As a result a even order non-linearity cancellation is possible for m=1 (equal VCCSs):

$$i_\Delta = g_1 v_{in} + g_2 v_{in}^2 + g_3 v_{in}^3 - (-g_1 v_{in} + g_2 v_{in}^2 - g_3 v_{in}^3) = 2g_1 v_{in} + 2g_3 v_{in}^3 \qquad (6.44)$$

From eqn. 6.44 we see that the even order terms cancel in i_Δ while the odd order terms are doubled. This effect occurs for the $\{V_P,V_\Sigma\}$ class (input V_P) and $\{V_\Sigma,V_\Delta\}$ class (input V_Δ). In fact the $\{V_P,V_\Sigma\}$ and $\{V_\Sigma,V_\Delta\}$ subclasses are closely related: if v_P respectively $v_\Delta/2$ are the input signal, and the bias variables are chosen as $V_{\Sigma 0}$, $V_{P0}=V_{\Sigma 0}/2$ and $V_{\Delta 0}=0$, the circuits have the same behaviour. For other bias points of V_P this is not the case. Similar observations hold for the $\{V_P,V_\Delta\}$ and $\{V_\Sigma,V_\Delta\}$ subclass, with v_P, respectively v_Σ as input.

A subtraction of currents can also be exploited. In general, the difference of the currents of 2 VCCSs, both experiencing an input voltage v_{in}, can be written as:

$$i_\Delta = (g_{1a} - g_{1b})v_{in} + (g_{2a} - g_{2b})v_{in}^2 + (g_{3a} - g_{3b})v_{in}^3 \qquad (6.45)$$

For a fixed ratio 1:m between the coefficient g_i of $VCCS_a$ and $VCCS_b$ ($i \in \{1,2,3\}$), as assumed in Table 6-11, the subtraction leads to the same distortion. Since the signal component is reduced, this is useless. However, if we allow for different biasing of $VCCS_a$ and $VCCS_b$, a distortion advantage may sometimes be obtained, e.g. if coefficient g_2 and g_3 hardly change with biasing, *but* g_1 *does*. A general disadvantage of the subtraction is its increased sensitivity for mismatch and the reduction of the SNR (less signal, more noise).

6.5 The {I} and {I,I} Class

Table 6-11 shows the Taylor coefficients of v_a and v_b for the {I} and {I,I} class.

Class	Input variable	Output variable	linear coefficient	second order coefficient	third order coefficient
$\{I_P,I_\Sigma\}$	i_a (i_Σ=0)	v_a	r_1	r_2	r_3
$\{I_P,I_\Sigma\}$	i_a (i_Σ=0)	v_a	r_1	r_2	r_3
		v_b	$-r_1/m$	r_2/m^2	$-r_3/m^3$
	i_Σ (i_a=0)	v_a	0	0	0
		v_b	r_1/m	r_2/m^2	r_3/m^3
$\{I_P,I_\Delta\}$	i_a (i_Δ=0)	v_a	r_1	r_2	r_3
		v_b	r_1/m	r_2/m^2	r_3/m^3
	i_Δ (i_a = 0)	v_a	0	0	0
		v_b	$-r_1/m$	r_2/m^2	$-r_3/m^3$
$\{I_\Sigma,I_\Delta\}$	i_Σ (i_Δ = 0)	v_a	$\frac{1}{2}\cdot r_1$	$\frac{1}{4}\cdot r_2$	$\frac{1}{8}\cdot r_3$
		v_b	$\frac{1}{2}\cdot r_1/m$	$\frac{1}{4}\cdot r_2/m^2$	$\frac{1}{8}\cdot r_3/m^3$
	i_Δ (i_Σ = 0)	v_a	$\frac{1}{2}\cdot r_1$	$\frac{1}{4}\cdot r_2$	$\frac{1}{8}\cdot r_3$
		v_b	$-\frac{1}{2}\cdot r_1/m$	$\frac{1}{4}\cdot r_2/m^2$	$-\frac{1}{8}\cdot r_3/m^3$

Table 6-12: Taylor coefficients of the VCCS voltages for the {I} and {I,I} classes.

The derivation of the Taylor coefficients for the {I,I} class are dual to those of the {V,V} class: their mathematical form is identical, yet voltages replace currents and vice versa. Therefore it is convenient to use the inverse Taylor series expression of eqn. 6.35. Similar non-linearity cancellation consideration as for the {V,V} class hold.

6.6 The {V,I} Class

The analysis of the Taylor coefficients for the {V,I} class is somewhat more complex than for the {V,V} and {I,I} class, since a voltage or current has to be solved from a non-linear relation. However, the method used in section 6.3.1 can be used to do this. Since voltages and currents can be both input and output variables, four types of transfer functions are possible. The results are therefore presented in four tables: Table 6-13 (v→i), Table 6-15(v→v), Table 6-16 (i→i) and Table 6-17(i→v).

Sub-class	Input var.	Output var.	linear coeff.	second order coefficient	third order coefficient
$\{V_P,I_\Sigma\}$	v_a (i_Σ=0)	i_a	g_1	g_2	g_3
		i_b	$-g_1$	$-g_2$	$-g_3$
$\{V_P,I_\Delta\}$	v_a (i_Δ=0)	i_a	g_1	g_2	g_3
		i_b	g_1	g_2	g_3
$\{V_\Sigma,I_P\}$	v_Σ (i_a=0)	i_a	0	0	0
		i_b	$m\cdot g_1$	$m\cdot g_2$	$m\cdot g_3$
$\{V_\Delta,I_P\}$	v_Δ (i_a=0)	i_a	0	0	0
		i_b	$-m\cdot g_1$	$-m\cdot g_2$	$-m\cdot g_3$
$\{V_\Sigma,I_\Sigma\}$ *	v_Σ (i_Σ=0)	i_a	$\frac{m}{m-1}g_1$	$\frac{m(m^2+1)}{(m-1)^3}g_2$	$\frac{m(m^3-1)}{(m-1)^4}g_3+\frac{2m^2(m+1)^2}{(m-1)^5}\frac{g_2^2}{g_1}$
		i_b	$-\frac{m}{m-1}g_1$	$-\frac{m(m^2+1)}{(m-1)^3}g_2$	$-\frac{m(m^3-1)}{(m-1)^4}g_3-\frac{2m^2(m+1)^2}{(m-1)^5}\frac{g_2^2}{g_1}$
$\{V_\Sigma,I_\Delta\}$	v_Σ (i_Δ=0)	i_a	$\frac{m}{m+1}g_1$	$\frac{m(m^2+1)}{(m+1)^3}g_2$	$\frac{m(m^3+1)}{(m+1)^4}g_3-\frac{2m^2(m-1)^2}{(m+1)^5}\frac{g_2^2}{g_1}$
		i_b	$\frac{m}{m+1}g_1$	$\frac{m(m^2+1)}{(m+1)^3}g_2$	$\frac{m(m^3+1)}{(m+1)^4}g_3-\frac{2m^2(m-1)^2}{(m+1)^5}\frac{g_2^2}{g_1}$
$\{V_\Delta,I_\Sigma\}$	v_Δ (i_Σ=0)	i_a	$\frac{m}{m+1}g_1$	$\frac{m(m-1)}{(m+1)^2}g_2$	$\frac{m(m^2-m+1)}{(m+1)^3}g_3-\frac{2m^2}{(m+1)^3}\frac{g_2^2}{g_1}$
		i_b	$-\frac{m}{m+1}g_1$	$-\frac{m(m-1)}{(m+1)^2}g_2$	$-\frac{m(m^2-m+1)}{(m+1)^3}g_3+\frac{2m^2}{(m+1)^3}\frac{g_2^2}{g_1}$
$\{V_\Delta,I_\Delta\}$ *	v_Δ (i_Δ=0)	i_a	$\frac{m}{m-1}g_1$	$\frac{m(m+1)}{(m-1)^2}g_2$	$\frac{m(m^2+m+1)}{(m-1)^3}g_3+\frac{2m^2}{(m-1)^3}\frac{g_2^2}{g_1}$
		i_b	$\frac{m}{m-1}g_1$	$\frac{m(m+1)}{(m-1)^2}g_2$	$\frac{m(m^2+m+1)}{(m-1)^3}g_3+\frac{2m^2}{(m-1)^3}\frac{g_2^2}{g_1}$

Table 6-13: Taylor coefficients of the VCCS currents for the {V,I} class with voltage input. The cases marked with * only have a solution for m≠1.

Unfortunately, the $\{V_\Sigma,I_\Sigma\}$ and $\{V_\Delta,I_\Delta\}$ subclass have zero denominator terms for m=1 in all cases. The expressions are not valid for m=1, since there is no unique solution in that case. The results will now be discussed, focusing on cases with attractive distortion properties. Special attention will be paid to circuits with a v→i transfer function, since these can be used as alternative implementations for the VCCSs introduced in chapter 3.

6.6.1 The {V,I} Class: Voltage Input, Current Output

Table 6-13 shows Taylor coefficients for v→i transfer characteristics. The first 4 cases, involving a primary variable V_P or I_P, render Taylor coefficients equal to those of a single VCCS (apart from the sign). Thus no distortion advantage is obtained.

The Taylor expressions for the 4 subclasses with two secondary variables are much more involved. The i-th order coefficients all have a term proportional to g_i, but the third order coefficient also has a term proportional to g_2^2/g_1. Furthermore, the 2nd and 3rd order distortion depends on m for these cases. Now there are possibilities to improve the linearity compared to a single VCCS. For the $\{V_\Sigma,I_\Delta\}$ case with m=1, for instance, the following 2nd and 3rd order intercept voltages are found:

$$V_{IP2} = 4\left|g_1\right|/\left|g_2\right| \qquad V_{IP3} = 4\sqrt{\left|g_1\right|/\left|g_3\right|} \qquad (\{V_\Sigma,I_\Delta\};V_\Sigma \rightarrow I_a \text{ or } I_b) \quad (6.46)$$

These values are 2 times larger as for a single VCCS. Intuitively, this can be understood by realising that the input voltage is divided equally over two VCCSs. Thus, for the same input voltage swing, HD2 is two times smaller and HD3 four times smaller, i.e. V_{IP2} and V_{IP3} are doubled. Figure 6-5a shows an example of a $\{V_\Sigma,I_\Delta\}$ circuit, for which V_{IP3} is doubled compared to a single differential pair [40]. V_{IP2} is infinite for differential pairs biased at zero as g_2=0 in that case. An example of a circuit with doubled V_{IP3} and V_{IP2} is the "stacked MOST" circuit of Figure 6-5b. It shows less deviation from square-law behaviour than a single MOST [90] (reduced influence of mobility reduction).

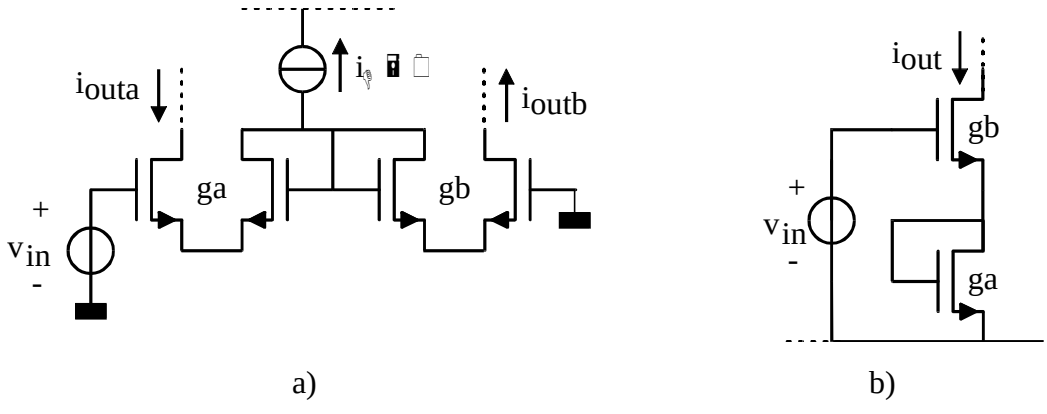


Figure 6-5: $\{V_\Sigma,I_\Delta\}$ circuits ($v_\Sigma \rightarrow i_a$; m=1) with doubled V_{IP2} and V_{IP3} compared to a single VCCS: a) 2 differential pairs [40]; b) Stacked MOSTs [90].

Cancellation of Non-linear Terms

In some cases (partial) distortion cancellation can occur. A case of special interest is the $\{V_\Delta,I_\Sigma\}$ case, to which the differential pair belongs, with VCCS currents for m=1:

$$i_a = -i_b = \tfrac{1}{2} g_1 v_\Delta + \left(\tfrac{1}{8} g_3 - \tfrac{1}{4} \frac{g_2^2}{g_1} \right) v_\Delta^3 \tag{6.47}$$

In eqn. 6.47 the 2nd order term is cancelled (for m≠1 it does occur). The 3rd order term depends on the difference of a g_3-term and a g_2^2/g_1-term. Thus the 2nd order Taylor coefficients of the VCCSs also affect the 3rd order distortion. Since the g_2^2/g_1-term is always positive, a cancellation of 3rd order terms can occur if g_3 is also positive and has the same magnitude. The resulting 3rd order intercept voltage becomes:

$$V_{IP3} = 4 \left| g_1 \right| \Big/ \sqrt{\left| g_1 g_3 - 2 g_2^2 \right|} \tag{6.48}$$

Using Table 6-8, a relation between $g_1 g_3$ and g_2^2 for the LVCCSθ model can be found:

$$g_{1L\theta} \cdot g_{3L\theta} = g_{2L\theta}^2 \tag{6.49}$$

Substituting eqn. 6.49 in eqn. 6.48, the same value for V_{IP3} as for $g_2=0$ is found. Thus no third order distortion cancellation occurs, but only a sign reversal. Still V_{IP3} is two times larger than for a single LVCCSθ, since only half of the input voltage is present at a every VCCS (as for the $\{V_\Sigma, I_\Delta\}$ case, discussed above).

For the EVCCS, the following relation can be derived, using Table 6-7:

$$g_{1E} \cdot g_{3E} = \tfrac{2}{3} \cdot g_{2E}^2 \tag{6.50}$$

Unfortunately, this only does not lead to exact 3rd order distortion cancellation, but to 50% "overcompensation". Still, this improves the intercept voltage by a factor $\sqrt{2}$. Furthermore only half of the input voltage is present at the individual VCCS terminals, so that overall a $2\sqrt{2}$ times higher intercept voltage is found than for a single EVCCS.

VCCS model	**V_{IP3} for a $\{V_\Delta, I_\Sigma\}$ circuit**	**V_{IP3} for a single VCCS**	**Ratio**
Triode MOST (LVCCSθ)	$\frac{4}{\theta}$	$\frac{2}{\theta}$	2
Strong inversion, saturated MOST (SVCCSθ)	$4\sqrt{2}\left(V_0 - V_T\right)$	$2\sqrt{2}\sqrt{\frac{V_0 - V_T}{\theta}}$	$2\sqrt{\theta\left(V_0 - V_T\right)}$
EVCCS	$4\sqrt{3}V_E$	$2\sqrt{6}\,V_E$	$\sqrt{2}$

Table 6-14: Comparison of V_{IP3} for $\{V_\Delta, I_\Sigma\}$ circuits with m=1 and a single VCCS for different VCCS models.

A saturated strong inversion MOST has negative g_3 according to the SVCCSθ-model, so that the g_2^2/g_1 and g_3-terms add up. The resulting expression for V_{IP3} is shown in Table 6-14, along with that for a single VCCS, and their ratio. This ratio is usually smaller than 1, i.e. a differential pair shows more 3rd order distortion than a single MOST (e.g. for a 1µCMOS process with θ=0.15 1/V and V_0-V_T=0.5Volt, a ratio ½ is found). However, with increasing values of θ and for large values of (V_0-V_T), the ratio becomes close to 1 or even larger. Table 6-14 summarises the above discussed results.

Distortion Cancellation and Model Accuracy

The above mentioned sign reversal of the third order term for the LVCCSθ $\{V_\Delta,I_\Sigma\}$ case can be used to linearise a transconductor, by putting it in parallel to a LVCCSθ $\{V_\Sigma,V_\Delta\}$ class V-I converter [124]. Unfortunately, measurements results indicate that this only results in a moderate improvement of third order distortion (8 dB improvement in HD3), while it increases circuit complexity significantly. An essential problem with this type of linearisation is that it relies heavily on the accuracy of the device model. The same holds for the transconductor proposed by Coban et al [112] as discussed in a comment letter [113]. As reported in [34, 113, 124, 129], state of the art MOST models are not accurate enough to reliable predict the distortion performance, especially if cancellation of distortion terms is at stake. Another important problem relating to the cancellation technique is the question of reproducibility during IC-fabrication, and related issues of process characterisation and guaranteed device performance.

Although care should be taken in relying on device characteristics, it can sometimes be acceptable. The expressions in Table 6-13 can be used to conceive linearised transconductor circuits. As an example, consider a $\{V_\Delta,I_\Sigma\}$ circuit and calculate the condition for which the third order Taylor coefficient of i_a and i_b becomes 0. If we substitute the g-Taylor coefficient for a EVCCS, we find the following condition:

$$\frac{m\left(m^2-m+1\right)}{(m+1)^3}\frac{I}{6V_E^2}-\frac{2m^2}{(m+1)^3}\frac{I}{4V_E^2}=0 \qquad (6.51)$$

Solving for m gives: $m=0 \quad \vee \quad m=2\pm\sqrt{3}$ (6.52)

Obviously m=0 is not useful (zero g_1), but m=3.73 or m=0.37 can be used. The second order term is non-zero, but can be cancelled by a balanced configuration. This linearisation principle has been used with bipolar transistors as EVCCS, e.g. as described by Voorman [9], and with weak inversion MOSTs as EVCCS [116]. Similarly, it is possible to achieve linearity improvements based on the equations shown in Table 6-13 through Table 6-17.

6.6.2 The {V,I} Class: Voltage Input, Voltage Output

Table 6-15 gives the Taylor coefficients for the v→v transfer characteristics. For shortness, the discussion is confined to cases with simple non-linearity cancellations. The $\{V_\Sigma,I_P\}$ and $\{V_\Delta,I_P\}$ circuits implement a linear voltage gain of 1 and -1, i.e. a voltage copier. However, in fact only VCCSa plays an active role in these cases (e.g. as a source follower) and VCCSb can be left out. Alternatively, a voltage copier can be implemented with $\{V_P,I_\Sigma\}$ and $\{V_P,I_\Delta\}$ circuits for m=1. Examples of such circuits are shown in Figure 6-6. Now $VCCS_b$ contributes to the operation of the circuit as an I-V converter. It is easily verified from Table 6-15, that the $\{V_P,I_\Sigma\}$ circuit only has zero 2nd and 3rd order distortion, if g_2 is zero and m=1. This can be implemented in Figure 6-6a by using differential pairs biased at zero differential bias voltage. For the $\{V_P,I_\Delta\}$ circuit in Figure 6-6b, the condition m=1 is sufficient for linearity (equal VCCSs operating in the same bias point, i.e. I_Δ=0).

Sub-class	Input var.	Output var.	linear coeff.	second order coefficient	third order coefficient
$\{V_P,I_\Sigma\}$	v_a (i_Σ=0)	v_b	$-\frac{1}{m}$	$-\frac{m+1}{m^2}\frac{g_2}{g_1}$	$-\frac{m^2-1}{m^3}\frac{g_3}{g_1}-2\frac{(m+1)}{m^3}\frac{g_2^2}{g_1^2}$
$\{V_P,I_\Delta\}$	v_a (i_Δ=0)	v_b	$\frac{1}{m}$	$\frac{m-1}{m^2}\frac{g_2}{g_1}$	$\frac{m^2-1}{m^3}\frac{g_3}{g_1}-2\frac{(m-1)}{m^3}\frac{g_2^2}{g_1^2}$
$\{V_\Sigma,I_P\}$	v_Σ (i_a=0)	v_a	0	0	0
		v_b	1	0	0
$\{V_\Delta,I_P\}$	v_Δ (i_a=0)	v_a	0	0	0
		v_b	-1	0	0
$\{V_\Sigma,I_\Sigma\}$*	v_Σ (i_Σ=0)	v_a	$\frac{m}{m-1}$	$\frac{m(m+1)}{(m-1)^3}\frac{g_2}{g_1}$	$-\frac{m(m+1)}{(m-1)^3}\frac{g_3}{g_1}-4\frac{m^2(m+1)}{(m-1)^5}\frac{g_2^2}{g_1^2}$
		v_b	$-\frac{1}{m-1}$	$-\frac{m(m+1)}{(m-1)^3}\frac{g_2}{g_1}$	$\frac{m(m+1)}{(m-1)^3}\frac{g_3}{g_1}+4\frac{m^2(m+1)}{(m-1)^5}\frac{g_2^2}{g_1^2}$
$\{V_\Sigma,I_\Delta\}$	v_Σ (i_Δ=0)	v_a	$\frac{m}{m+1}$	$-\frac{m(m-1)}{(m+1)^3}\frac{g_2}{g_1}$	$-\frac{m(m-1)}{(m+1)^3}\frac{g_3}{g_1}+4\frac{m^2(m-1)}{(m+1)^5}\frac{g_2^2}{g_1^2}$
		v_b	$\frac{1}{m+1}$	$\frac{m(m-1)}{(m+1)^3}\frac{g_2}{g_1}$	$\frac{m(m-1)}{(m+1)^3}\frac{g_3}{g_1}-4\frac{m^2(m-1)}{(m+1)^5}\frac{g_2^2}{g_1^2}$
$\{V_\Delta,I_\Sigma\}$	v_Δ (i_Σ=0)	v_a	$\frac{m}{m+1}$	$-\frac{m}{(m+1)^2}\frac{g_2}{g_1}$	$-\frac{m(m-1)}{(m+1)^3}\frac{g_3}{g_1}$
		v_b	$-\frac{1}{m+1}$	$-\frac{m}{(m+1)^2}\frac{g_2}{g_1}$	$-\frac{m(m-1)}{(m+1)^3}\frac{g_3}{g_1}$
$\{V_\Delta,I_\Delta\}$*	v_Δ (i_Δ=0)	v_a	$\frac{m}{m-1}$	$\frac{m}{(m-1)^2}\frac{g_2}{g_1}$	$\frac{m(m+1)}{(m-1)^3}\frac{g_3}{g_1}$
		v_b	$\frac{1}{m-1}$	$\frac{m}{(m-1)^2}\frac{g_2}{g_1}$	$\frac{m(m+1)}{(m-1)^3}\frac{g_3}{g_1}$

Table 6-15: Taylor coefficients of the VCCS voltages for the {V,I} class with voltage input. The cases marked with * only have a solution for m≠1.

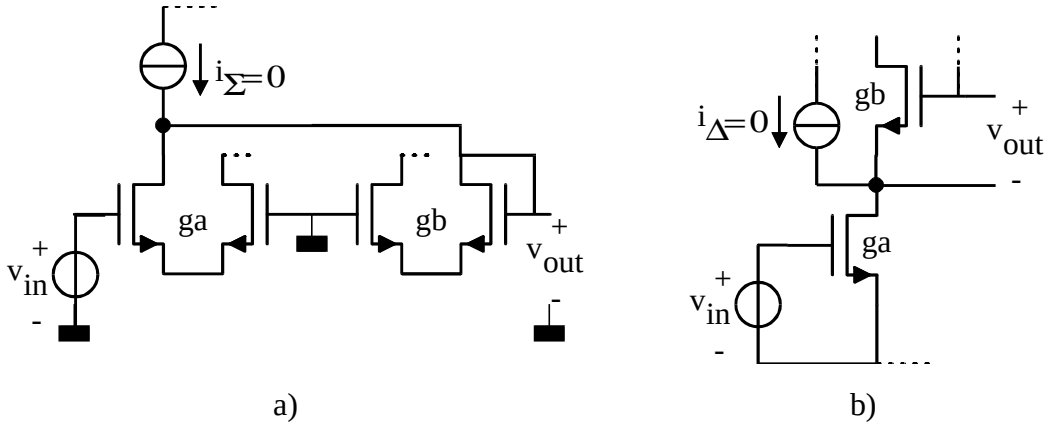


Figure 6-6: Examples of voltage copiers that are linear for m=1: a) $\{V_P,I_\Sigma\}$ circuit ($v_a \rightarrow v_b$); b) $\{V_P,I_\Delta\}$ circuit ($v_a \rightarrow v_b$).

Some cases with a gain equal to ½ at m=1 also render distortion cancellation: the 2nd and 3rd order terms cancel for $\{V_\Sigma,I_\Delta\}$ circuits, and the 3rd order term cancels for $\{V_\Delta,I_\Sigma\}$ circuits. Examples of such circuits are shown in Figure 6-7. Other gain values are also possible for m≠1, however in general with non-zero 2nd and 3rd order distortion.

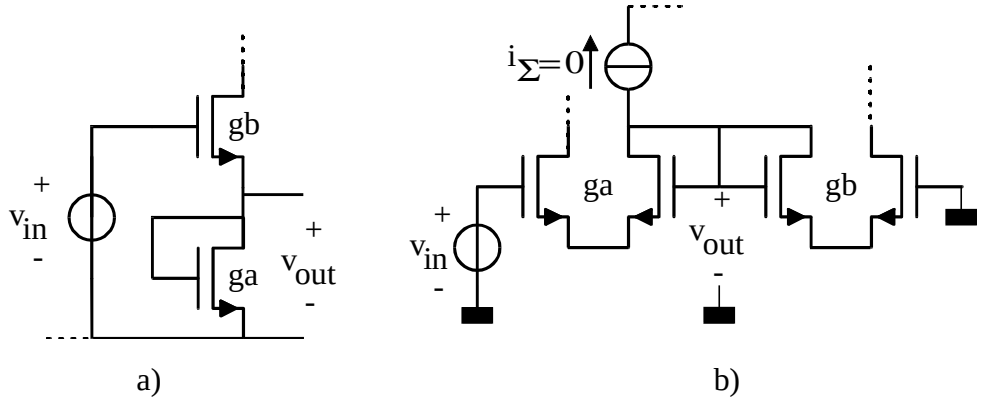


Figure 6-7: Examples of linear voltage dividers with gain ½: a) $\{V_\Sigma,I_\Delta\}$ circuit ($v_\Sigma \rightarrow v_a$); b) $\{V_\Delta,I_\Sigma\}$ circuit ($v_\Sigma \rightarrow -v_b$).

With reference to the circuit in Figure 6-7b a remark can be made on its classification as a $\{V_\Delta,I_\Sigma\}$ circuit: it can also be considered as a $\{V_\Sigma,I_\Delta\}$ circuit. In fact the classification depends on the choice of the reference direction for the voltage and current of the VCCS. In accordance with chapter 5, the direction should be chosen such that the I(V) equations of the 2 VCCSs have the same mathematical form. However, a differential pair with equal MOSTs has a point symmetrical transfer characteristic around zero. Hence, exchange of both the voltage and current terminals of a VCCS does not change its transfer characteristic and the classification is not unambiguous in that case. As a result, the Taylor coefficients for the $\{V_\Delta,I_\Sigma\}$ and $\{V_\Sigma,I_\Delta\}$ classes must be equal for the case $g_2=0$ (point symmetrical characteristic). Indeed Table 6-13 through Table 6-17 render the same results, e.g. for the coefficients of v_a or i_a. For bias points with $g_2\neq 0$ this is no longer true.

In interpreting the results in the tables, note that the Taylor coefficients are derived under the assumption that $g_{ib}=m\cdot g_{ia}$ ($i \in \{1,2,3\}$). In general, this assumption is only valid regardless of the VCCS transfer characteristic, if $VCCS_a$ consists of m parallel connected copies of $VCCS_b$, biased at equal bias voltages.

6.6.3 The {V,I} Class: Current Input, Current Output

The Taylor coefficient for {V,I} circuits with a current input and current output are shown in Table 6-16. Looking at the rightmost column of Table 6-16, it appears that r_3 coefficients cancel in the current expression. This is only for the presumed case of a ratio of 1:m between the Taylor coefficients of $VCCS_a$ and $VCCS_b$. A distortion free current gain of 1 and -1 is possible with $\{V_P,I_\Sigma\}$ and $\{V_P,I_\Delta\}$ circuits. Figure 6-8 show two well-known examples of these circuits: cascode circuits. A very useful circuit class is the $\{V_\Delta,I_P\}$ class, implementing electronically variable current gain. For $V_\Delta=0$, a current amplifier with fixed gain 1:m is found (e.g. the current mirror of Figure 6-9a). Circuits belonging to the $\{V_\Sigma,I_P\}$ class implement a similar function, however, in general with non-zero second and third

order distortion. If r_2 of the VCCS is zero, these distortion terms are nullified, e.g. in the circuit of Figure 6-9b (the differential pairs have zero r_2 for zero differential bias voltage).

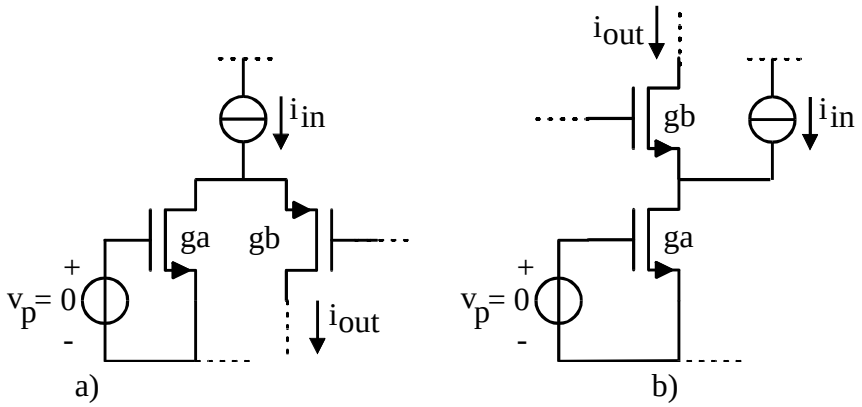


Figure 6-8: Current copier circuits: a) {V_P,I_Σ} circuit ($v_\Sigma \rightarrow i_b$); b) {V_P,I_Δ} circuit ($i_\Delta \rightarrow i_b$).

Class	Input var.	Output var.	linear coeff.	second order coefficient	third order coefficient
$\{V_P,I_\Sigma\}$	i_Σ (v_a=0)	i_a	0	0	0
		i_b	1	0	0
$\{V_P,I_\Delta\}$	i_Δ (v_a=0)	i_a	0	0	0
		i_b	-1	0	0
$\{V_\Sigma,I_P\}$	i_a (v_Σ=0)	i_b	-m	$-2m\frac{r_2}{r_1}$	$-4m\frac{r_2^2}{r_1^2}$
$\{V_\Delta,I_P\}$	i_P (v_Δ=0)	i_b	m	0	0
$\{V_\Sigma,I_\Sigma\}^*$	i_Σ (v_Σ=0)	i_a	$\frac{m}{m-1}$	$\frac{2m}{(m-1)^3}\frac{r_2}{r_1}$	$4\frac{m(m+1)}{(m-1)^5}\frac{r_2^2}{r_1^2}$
		i_b	$-\frac{1}{m-1}$	$-\frac{2m}{(m-1)^3}\frac{r_2}{r_1}$	$-4\frac{m(m+1)}{(m-1)^5}\frac{r_2^2}{r_1^2}$
$\{V_\Sigma,I_\Delta\}$	i_Δ (v_Σ=0)	i_a	$\frac{1}{m+1}$	$-\frac{2m}{(m+1)^3}\frac{r_2}{r_1}$	$4\frac{m(m-1)}{(m+1)^5}\frac{r_2^2}{r_1^2}$
		i_b	$-\frac{m}{m+1}$	$-\frac{2m}{(m+1)^3}\frac{r_2}{r_1}$	$4\frac{m(m-1)}{(m+1)^5}\frac{r_2^2}{r_1^2}$
$\{V_\Delta,I_\Sigma\}$	i_Σ (v_Δ=0)	i_a	$\frac{1}{m+1}$	0	0
		i_b	$\frac{m}{m+1}$	0	0
$\{V_\Delta,I_\Delta\}^*$	i_Δ (v_Δ=0)	i_a	$-\frac{1}{m-1}$	0	0
		i_b	$-\frac{m}{m-1}$	0	0

Table 6-16: Taylor coefficients of the VCCS currents for the {V,I} class with current input. The cases marked with * only have a solution for $m \neq 1$.

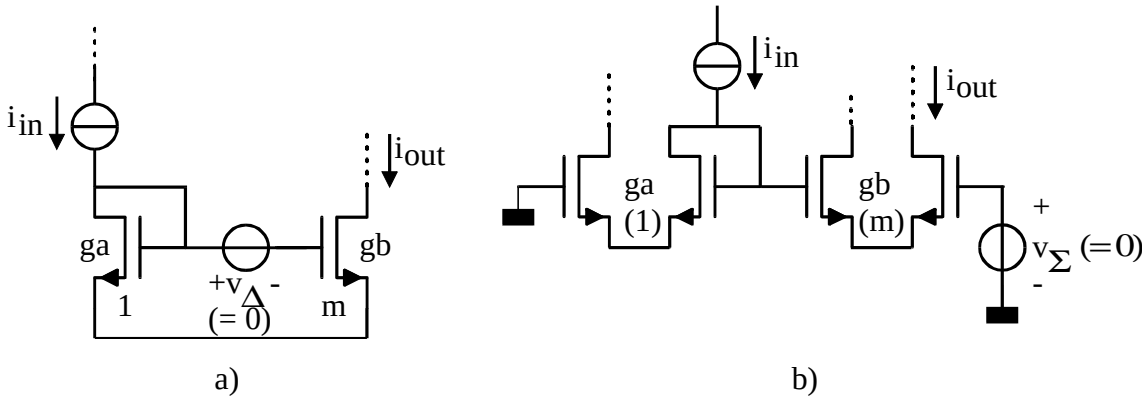


Figure 6-9: Current amplifiers: a) {V_Δ,I_P} circuit ($i_a \rightarrow i_b$); b) {V_Σ,I_P} circuit ($i_a \rightarrow i_b$).

A last circuit worth mentioning is a current divider or current splitter with zero 2nd and 3rd order distortion: the {V_Δ,I_Σ} circuit shown in Figure 6-10. A linear division is achieved for a differential bias voltage of zero, satisfying $g_{ib}=m \cdot g_{ia}$ ($i \in \{1,2,3\}$).

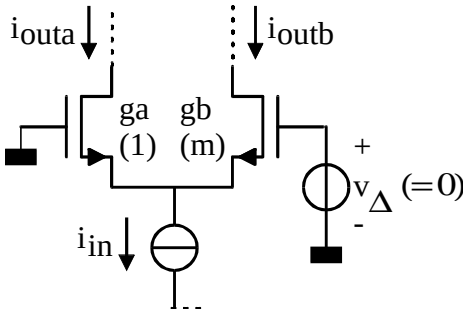


Figure 6-10: Current divider circuit belonging to the {V_Δ,I_Σ} class ($i_\Sigma \rightarrow i_a$).

6.6.4 The {V,I} Class: Current Input, Voltage Output

Finally the Taylor coefficient of circuits with current input and voltage output are shown in Table 6-17. The first 4 classes involving a primary variable result in the same coefficients as for a single VCCS, except for sign changes. The classes with 2 secondary variables do allow for linearity improvements compared to a single VCCS. For instance, for m=1 the 2nd order coefficients for the {V_Σ,I_Δ} class is cancelled. Furthermore, the 2nd and 3rd order intercept current are doubled for the {V_Δ,I_Σ} case compared to a single VCCS.

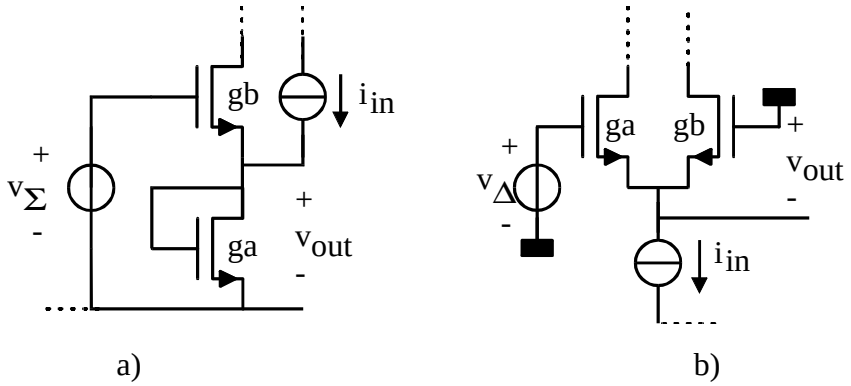


Figure 6-11: I-Vconverter circuits with a better linearity than a single VCCS: a) {V_Σ,I_Δ} circuit ($i_\Delta \rightarrow v_a$); b) {V_Δ,I_Σ} circuit ($i_\Sigma \rightarrow v_b$).

Class	Input var.	Output var.	linear coeff.	second order coefficient	third order coefficient
$\{V_P,I_\Sigma\}$	i_Σ (v_a=0)	v_b	$\frac{r_1}{m}$	$\frac{r_2}{m^2}$	$\frac{r_3}{m^3}$
$\{V_P,I_\Delta\}$	i_Δ (v_a=0)	v_b	$-\frac{r_1}{m}$	$\frac{r_2}{m^2}$	$-\frac{r_3}{m^3}$
$\{V_\Sigma,I_P\}$	i_a (v_Σ=0)	v_a v_b	r_1 $-r_1$	r_2 $-r_2$	r_3 $-r_3$
$\{V_\Delta,I_P\}$	i_P (v_Δ=0)	v_a v_b	r_1 r_1	r_2 r_2	r_3 r_3
$\{V_\Sigma,I_\Sigma\}^*$	i_Σ (v_Σ=0)	v_a v_b	$-\frac{r_1}{m-1}$ $-\frac{1}{m-1}$	$-\frac{(m+1)}{(m-1)^3}r_2$ $\frac{(m+1)}{(m-1)^3}r_2$	$-\frac{m}{(m-1)^3}r_3-8\frac{m}{(m-1)^5}\frac{r_2^2}{r_1}$ $\frac{m}{(m-1)^3}r_3+8\frac{m}{(m-1)^5}\frac{r_2^2}{r_1}$
$\{V_\Sigma,I_\Delta\}$	i_Δ (v_Σ=0)	v_a v_b	$\frac{r_1}{m+1}$ $-\frac{r_1}{m+1}$	$-\frac{(m-1)}{(m+1)^3}r_2$ $\frac{(m-1)}{(m+1)^3}r_2$	$\frac{1}{(m+1)^3}r_3-8\frac{m}{(m+1)^5}\frac{r_2^2}{r_1}$ $-\frac{1}{(m+1)^3}r_3+8\frac{m}{(m+1)^5}\frac{r_2^2}{r_1}$
$\{V_\Delta,I_\Sigma\}$	i_Σ (v_Δ=0)	v_a v_b	$\frac{r_1}{m+1}$ $\frac{r_1}{m+1}$	$\frac{r_2}{(m+1)^2}$ $\frac{r_2}{(m+1)^2}$	$\frac{r_3}{(m+1)^3}$ $\frac{r_3}{(m+1)^3}$
$\{V_\Delta,I_\Delta\}^*$	i_Δ (v_Δ=0)	v_a v_b	$-\frac{1}{m-1}$ $-\frac{m}{m-1}$	$-\frac{r_2}{(m-1)^2}$ $-\frac{r_2}{(m-1)^2}$	$-\frac{r_3}{(m-1)^3}$ $-\frac{r_3}{(m-1)^3}$

Table 6-17: Taylor coefficients of the VCCS voltages for the {V,I} class with current input. The cases marked with * only have a solution for $m\neq 1$.

6.7 Summary and Conclusions

In this chapter, the large signal behaviour of VCCS circuits has been analysed. The most important results and conclusion are listed below.

Bias Point and DC Transfer Characteristic

- DC transfer characteristics have been derived for all classes of 1VCCS and 2VCCS circuits, biased with DC voltage and/or current sources. The VCCSs were modelled using the 3 generalised VCCS models. The resulting expressions can be used to calculate bias points, and find the approximate large signal transfer characteristic.
- The upper and lower limits for the input and control variables of 1VCCS and 2VCCS circuits have been derived, based on the validity voltage-limits of the generalised VCCS models.

- The operating-range of 2VCCS circuits has been presented in a two-dimensional graphical way, visualising design trade-offs between the 2 independent input variables. Independent of the VCCS model equation, 4 "anchor points" exist in these figures, corresponding to the 4 possible combinations of extreme values of the primary VCCS variables.

Non-linearity of a Single VCCS

- The non-linearity of a VCCS is modelled by means of a third order Taylor series. Apart from the i(v) relation with Taylor coefficient g_1, g_2 and g_3, Taylor coefficients for the inverse function v(i) have been derived (r_1, r_2 and r_3).
- Second and third order *intercept voltages* were derived for several important MOST VCCS implementations. It appears that a triode MOST has the highest intercept voltages (order of magnitude: 10Volt for a 1µmCMOS process), closely followed by a saturated MOS transistor (1-7 Volt, increasing with the gate-source overdrive voltage). A weak inversion MOST typically has an order of magnitude lower intercept voltages (roughly 150-200mV).
- Second and third order intercept *currents* have also been derived. The differences between different VCCS types are less pronounced in this case.

Distortion in Different Classes of 2VCCS Circuits

The transfer characteristics of 2VCCS circuits have been expressed as Taylor series in terms of the Taylor coefficients of the constituting VCCSs. In this way, the linearising effect of different circuit topologies becomes explicitly visible.

{V,V} Class

The {V,V} class allows for linearity improvements compared to a single VCCS in at least two ways:

1. $\{V_P,V_\Sigma\}$ circuits with V_P as input and $\{V_\Sigma,V_\Delta\}$ circuits with V_Δ as input render even order distortion cancellation for equal VCCSs. The odd order terms are doubled (balancing) in this case, so that odd order distortion remains the same.
2. $\{V_P,V_\Delta\}$ circuits with V_P as input and $\{V_\Sigma,V_\Delta\}$ circuits with V_Σ as input, reduce the coefficients g_1, g_2 and g_3 to the difference of g_1, g_2 and g_3 of the 2 VCCSs involved. If g_2 and/or g_3 are relatively bias independent, whereas g_1 strongly varies with bias, this can be advantageous. A general disadvantage of this technique is its sensitivity for mismatch and noise, because of the subtraction of signals.

{I,I} Class

The results for the {I,I} class are dual to those of the {V,V} class. Thus similar observations as for the {V,V} class hold, with voltages replaced by current and g-coefficients by r-coefficients.

{V,I} Class

The {V,I} class results in much more complex Taylor coefficient expressions. In order to make them tractable for hand calculations it was assumed that a fixed ratio exists between the coefficients of $VCCS_a$ and $VCCS_b$. Using this assumption, Taylor coefficient for v→i, v→v, i→i and i→v transfer functions were derived.

For v→i and i→v relations this lead to the following results:

- The circuit classes involving forcing a primary VCCS variable, have Taylor coefficients equal to those of a single VCCS, and thus no linearity improvement.
- For cases with 2 secondary variables, more complex Taylor coefficients occur. The 3rd order distortion is not only determined by 3rd order Taylor coefficients of the constituting VCCSs, but also by 2nd order Taylor coefficients. This effect allows for manipulation of distortion coefficients to improve linearity.
- Compared to a single VCCS, a reduction in distortion is often possible with a 2VCCS circuit, if the input signal is divided over two VCCSs. If each VCCS experiences half of the input signal swing, this leads to a doubled 2nd and 3rd order intercept voltage or current.

For v→v and i→i relations the following results were found:

- Linear voltage and current copier circuits can be realised with several subclasses of {V,I} circuits.
- Voltage and current attenuators and amplifiers are also possible. For current outputs, the 3rd order coefficients of the VCCSs cancel in the expressions. The 3rd order distortion is determined by 2nd order coefficients.

7

Noise Analysis of 2VCCS Circuits

7.1 Introduction

The dynamic range of linear circuits is a property of paramount importance for signal processing. In the previous chapter the upper limit of the dynamic range, determined by non-linearity, was discussed. This chapter deals with the lower boundary, the noise floor. In section 7.2 and 7.3 the equivalent input noise of VCCS circuits is analysed, aiming at a systematic method. Again the classification of chapter 5 appears to be of great help.

7.2 Noise analysis of 2VCCS circuits

To analyse the noise properties of a linear transactor, the noise contribution of individual VCCSs needs to be modelled. As the squared white noise current of a VCCS is usually closely related to its transconductance, it is convenient to express it as:

$$\overline{i_{n,gm}^2} = 4 \cdot k_B \cdot T \cdot NEF \cdot g_m \cdot \Delta f \qquad (7.1)$$

where *NEF* denotes the *Noise Excess Factor*, which is defined as the ratio of the noise power produced by a VCCS and the noise power produced by a resistor with value $1/g_m$ (squared noise current equal to $4 \cdot k_B \cdot T \cdot g_m \cdot \Delta f$). Apart from white thermal noise, MOSTs show 1/f noise. However, the main application area of VCCS circuits is in broadband circuits, where 1/f noise is usually of less concern. Therefore only thermal noise will be considered in this thesis. If needed, 1/f noise can be included in the model, e.g. by allowing NEF to be a function of frequency. The value of NEF according to simple MOST models for different operating regions in shown in Table 7-1 [32]. For a saturated MOST in weak and in strong inversion it is somewhat smaller than 1 (in practice somewhat higher values are found). For a triode-MOST NEF is roughly equal to $V_{DS,sat}/V_{DS}$. Hence it increases drastically from a value close to 1 in saturation to large values for large ratios of $V_{DS,sat}/V_{DS}$.

VCCS model	NEF
Triode MOST	$V_{DS,sat}/V_{DS}$-1/3
Strong Inversion, Saturated MOST	2/3
Weak Inversion MOST	1/2

Table 7-1: NEF for a MOST in different operating regions.

The noise contributions of individual VCCSs can be analysed by means of superposition. All independent noise sources are then put to zero, except for one. The resulting output noise is the noise contribution for that source. Dividing by the transfer function renders the equivalent input noise. By repeating this analysis for all independent noise sources, and adding the individual noise power contributions (assuming they are independent), the total noise is found. We will now follow this analysis procedure for 1VCCS and 2VCCS circuits, and calculate the output noise due to $VCCS_a$ and $VCCS_b$. Fortunately, we can fruitfully use the classification from chapter 5, to simplify the analysis task. This is explained conveniently by considering Figure 7-1: here the noise current sources $i_{n,ga}$ and $i_{n,gb}$ are drawn in parallel to the controlled current source i_a and i_b of the VCCSs.

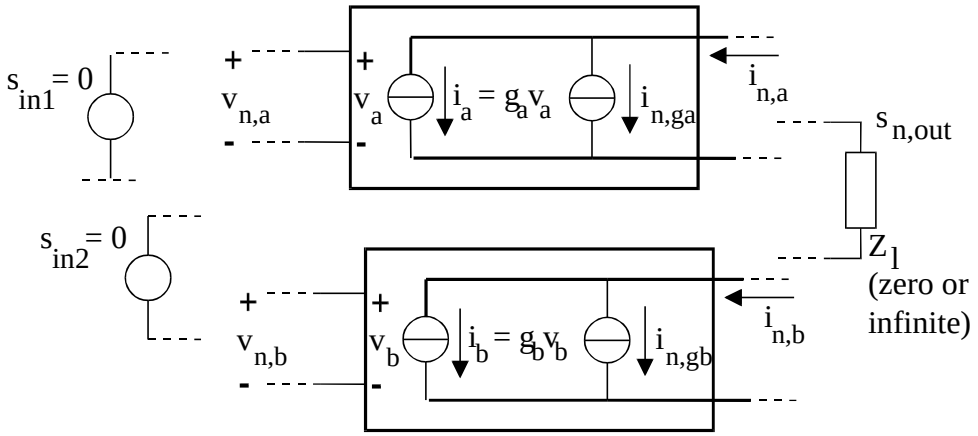


Figure 7-1: Noise model for a VCCS circuit: the independent noise source $i_{n,ga}$ and $i_{n,gb}$ result in noise voltage $v_{n,a}$ and $v_{n,b}$ and noise current $i_{n,a}$ and $i_{n,b}$.

Comparing the circuit with one without noise sources, it can be concluded that the differences can be accounted for by means of the following substitutions:

$$i_a \longrightarrow i_a + i_{n,ga} \tag{7.2}$$

$$i_b \longrightarrow i_b + i_{n,gb} \tag{7.3}$$

Substituting these values in the results of the small signal analysis of chapter 5, and putting s_{in1} and s_{in2} to zero, the noise voltages $v_{n,a}$ and $v_{n,b}$ and noise current $i_{n,a}$ and $i_{n,b}$ are found (see Figure 7-1). Since a linear combination of the primary VCCS variables and input variables constitutes the output variable s_{out}, the noise at the output $s_{n,out}$ can easily be calculated from $v_{n,a}$, $v_{n,b}$, $i_{n,a}$, $i_{n,b}$. Note that the latter variables are also determined by the circuit environment. If, for example, $i_{n,ga}$ would "see" equal impedances "looking into" $VCCS_a$ and to the rest of the circuit, half of $i_{n,ga}$ will flow in $VCCS_a$ ($i_a = -\frac{1}{2} i_{n,ga}$), and $i_{n,a}$ will be equal to $\frac{1}{2} i_{n,ga}$.

Table 7-1 lists the noise contributions of $VCCS_a$ ($i_{n,ga}$) to $v_{n,a}$, $v_{n,b}$, $i_{n,a}$ and $i_{n,b}$ for different classes of VCCS circuits. Some of the results will be discussed for good understanding. If primary VCCS voltage V_a is forced equal to a noiseless voltage ({V,V} class and {V,I} classes involving forcing V_P), in effect $v_{n,a}$ is forced equal to zero (it is equal to the noise part of this voltage, which is supposed to be zero). In these cases, noise current $i_{n,ga}$ contributes directly (gain 1) to $i_{n,a}$ ($v_a=0 \Rightarrow i_a=0$). On the other hand, if the current of $VCCS_a$ is forced equal to a noiseless current ({I,I} class and {V,I} classes involving forcing I_P), in effect $i_{n,a}$ is forced equal to zero (and $i_a= -i_{n,ga}$). The resulting noise voltage $v_{n,a}$ is $-i_{n,ga}/g_a$ in this case.

Class	$v_{n,a,ga}/\ i_{n,ga}$	$v_{n,b,ga}/\ i_{n,ga}$	$i_{n,a,ga}/\ i_{n,ga}$	$i_{n,b,ga}/\ i_{n,ga}$
{V,V}	0	0	1	0
{I,I}	$-1/g_a$	0	0	0
$\{V_P,I_\Sigma\}$	0	$-\frac{1}{g_b}$	1	-1
$\{V_P,I_\Delta\}$	0	$\frac{1}{g_b}$	1	1
$\{V_\Sigma,I_P\}$	$-\frac{1}{g_a}$	$\frac{1}{g_a}$	0	$\frac{g_b}{g_a}$
$\{V_\Delta,I_P\}$	$-\frac{1}{g_a}$	$-\frac{1}{g_a}$	0	$-\frac{g_b}{g_a}$
$\{V_\Sigma,I_\Sigma\}$	$-\frac{1}{g_a-g_b}$	$\frac{1}{g_a-g_b}$	$-\frac{g_b}{g_a-g_b}$	$\frac{g_b}{g_a-g_b}$
$\{V_\Sigma,I_\Delta\}$	$-\frac{1}{g_a+g_b}$	$\frac{1}{g_a+g_b}$	$\frac{g_b}{g_a+g_b}$	$\frac{g_b}{g_a+g_b}$
$\{V_\Delta,I_\Sigma\}$	$-\frac{1}{g_a+g_b}$	$-\frac{1}{g_a+g_b}$	$\frac{g_b}{g_a+g_b}$	$-\frac{g_b}{g_a+g_b}$
$\{V_\Delta,I_\Delta\}$	$-\frac{1}{g_a-g_b}$	$-\frac{1}{g_a-g_b}$	$-\frac{g_b}{g_a-g_b}$	$-\frac{g_b}{g_a-g_b}$

Table 7-1: Noise contributions of $VCCS_a$ to $v_{n,a}$, $v_{n,b}$, $i_{n,a}$, $i_{n,b}$. The output noise $s_{n,out}$ is a linear combination of them (should be added fully correlated).

Finally, if two secondary variables are forced, both VCCSs determine the noise contribution to $v_{n,a}$ and $i_{n,a}$. In these cases the transconductances g_a and g_b determine which part of $i_{n,ga}$ "flows inside $VCCS_a$" and which part "flows out". As seen in Table 7-1, $i_{n,ga}$ does not contribute to $v_{n,b}$ and $i_{n,b}$ for the {V,V} and {I,I} class. This is because there is no interaction between $VCCS_a$ and $VCCS_b$ in these classes: if one of them is changed, only variables relating to that VCCS change. For the {V,I} class, such an interaction does exist, so that the noise current of $VCCS_a$ also influences noise voltages and currents measured at the terminals of $VCCS_b$.

Table 7-2 lists the noise contributions of $VCCS_b$ ($i_{n,gb}$) to $v_{n,a}$, $v_{n,b}$, $i_{n,a}$ and $i_{n,b}$. Observations, very similar to those of $VCCS_a$ can be made. However, the results for the {V,I} class for cases involving forcing a primary variable are different. This is because, by convention, a primary variable is always assumed to be forced to $VCCS_a$. If this concerns

primary voltage V_a (classes $\{V_P,I_\Sigma\}$ and $\{V_P,I_\Delta\}$), I_a is fixed by the I(V) relation of the VCCS, and effectively I_b is forced equal to I_Σ-I_a or I_a-I_Δ. The latter currents are assumed to be noiseless during the analysis of the noise contribution of $VCCS_b$. Thus, I_b is forced equal to a noiseless current, as for the {I,I} class, and the same noise contribution is found. Similar reasoning leads to noise contributions for the $\{V_\Sigma,I_P\}$ and $\{V_\Delta,I_P\}$ class that are equal to those of the {V,V} class.

Class	$v_{n,a,gb}/\ i_{n,gb}$	$v_{n,b,gb}/\ i_{n,gb}$	$i_{n,a,gb}/\ i_{n,gb}$	$i_{n,b,gb}/\ i_{n,gb}$
{V,V}	0	0	0	1
{I,I}	0	$-\frac{1}{g_b}$	0	0
$\{V_P,I_\Sigma\}$	0	$-\frac{1}{g_b}$	0	0
$\{V_P,I_\Delta\}$	0	$-\frac{1}{g_b}$	0	0
$\{V_\Sigma,I_P\}$	0	0	0	1
$\{V_\Delta,I_P\}$	0	0	0	1
$\{V_\Sigma,I_\Sigma\}$	$-\frac{1}{g_a-g_b}$	$\frac{1}{g_a-g_b}$	$-\frac{g_a}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$
$\{V_\Sigma,I_\Delta\}$	$\frac{1}{g_a+g_b}$	$-\frac{1}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$
$\{V_\Delta,I_\Sigma\}$	$-\frac{1}{g_a+g_b}$	$-\frac{1}{g_a+g_b}$	$-\frac{g_a}{g_a+g_b}$	$\frac{g_a}{g_a+g_b}$
$\{V_\Delta,I_\Delta\}$	$\frac{1}{g_a-g_b}$	$\frac{1}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$	$\frac{g_a}{g_a-g_b}$

Table 7-2: Noise contributions of $VCCS_b$ to $v_{n,a}$, $v_{n,b}$, $i_{n,a}$, $i_{n,b}$. The output noise $s_{n,out}$ is a linear combination of them (should be added fully correlated).

An Example

As an example, the noise of a differential pair with noiseless current mirror as shown in Figure 7-2 is calculated. Using the table entries for the $\{V_\Delta,I_\Sigma\}$ case, the total noise in the differential output current $i_{n,\Delta}$ at short-circuited input and output is found to be:

$$\overline{i_{n,\Delta}^2}=\left(\frac{i_{n,a,ga}-i_{n,b,ga}}{i_{n,ga}}\right)^2\overline{i_{n,ga}^2}+\left(\frac{i_{n,a,gb}-i_{n,b,gb}}{i_{n,gb}}\right)^2\overline{i_{n,gb}^2}=\left(\frac{2g_b}{g_a+g_b}\right)^2\overline{i_{n,ga}^2}+\left(\frac{-2g_a}{g_a+g_b}\right)^2\overline{i_{n,gb}^2} \qquad (7.4)$$

The factor 2 in this expression results from the presence of a current mirror that doubles the output current. For $g_a=g_b$ the contributions of $VCCS_a$ and $VCCS_b$ are equal, and the sum of the mean squared noise currents is found. For $g_a>>g_b$ the noise term of $VCCS_a$ vanishes, while the contribution of $VCCS_b$ is quadrupled (due to the subtraction of correlated noise contributions of $i_{n,gb}$ to $i_{n,a}$ and $i_{n,b}$).

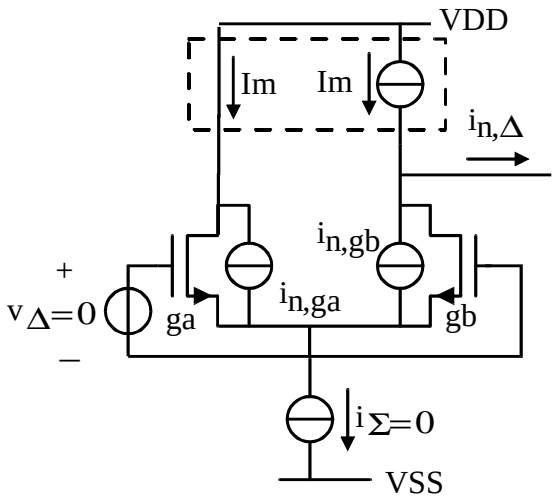
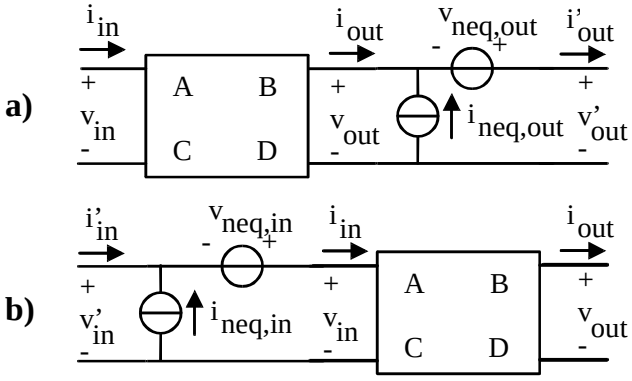


Figure 7-2: Example circuit for noise calculation: NMOST differential pair.

7.3 Multiple Non-zero Transmission Parameters

For the differential pair, the squared equivalent input noise voltage is easily derived from eqn. (7.4 by multiplication with transmission parameter B^2. However, the question arises how this should be done in cases with multiple non-zero transmission parameters. To answer this question reconsider the analysis procedure. Since the classification relates to transmission parameter test-conditions, the noise data relate to zero or infinite source- and load-impedance. If a transactor is used under such conditions, the noise data for the class corresponding to the conditions can be applied directly. However, if finite source- and/or load-impedances are connected, the situation is different.



$$v_{neq,in} = A \cdot v_{neq,out} + B \cdot i_{neq,out} \qquad (7.5)$$

$$i_{neq,in} = C \cdot v_{neq,out} + D \cdot i_{neq,out} \qquad (7.6)$$

Figure 7-3: Model of a noisy two-port as a noiseless two-port with 2 equivalent output noise sources $v_{neq,out}$ and $i_{neq,out}$ (a) or input noise sources $v_{neq,in}$ and $i_{neq,in}$.

It is common practice to model a noisy two-port by a noiseless two-port with equivalent noise sources added either at the output or at the input port as in Figure 7-3. The relation between the equivalent noise source in these models is given by eqn. 7.5 and 7.6 [24]. The values of these two equivalent sources can be determined by two suitable experiments. One would like to calculate them from the data listed in Table 7-1 and Table 7-2. The data correspond to transmission parameter test-conditions. Hence, one of the equivalent noise sources does not contribute to the noise (short-circuit across noise current source or noise voltage source with open terminal).

Table 7-1 and Table 7-2 provide us with 4 noise contributions for a two-port with 4 non-zero transmission parameters. This suggests that these noise data are not independent. Indeed this is true, as will be shown using the following reasoning. Assume that the two-port with equivalent input noise source in Figure 7-3b is shorted at the input ($v'_{in}=0$) and that the resulting open-output noise-voltage and short-circuit output-current are to be determined (respectively A and B test condition). In this case the noise current $i_{neq,in}$ flows entirely in the short-cut, and *cannot* produce any output noise. Thus the open-output noise-voltage is $v_{neq,in}/A$ while the short-circuit output noise-current is $v_{neq,in}/B$. The ratio between this output voltage and output current is B/A, which is the output impedance of the two-port under short circuit input conditions. Hence, these noise-data are not independent. By similar reasoning, the transmission parameter test conditions for C and D render redundant information about $i_{neq,in}$. If one wants to calculate the equivalent input noise sources, one should only take into account the noise contribution for case A *or* B (equivalent input noise voltage), and the contribution of case C *or* D (equivalent input noise current). If we arbitrarily favour A and C, the following relations can be used:

$$v_{neq,in} = \begin{cases} A \cdot v_{n,out}\big|_{v_{in}=0,i_{out}=0} & \text{if} \quad A \neq 0 \\ B \cdot i_{n,out}\big|_{v_{in}=0,v_{out}=0} & \text{if} \quad A = 0 \wedge B \neq 0 \\ 0 & \text{if} \quad A = 0 \wedge B = 0 \end{cases} \tag{7.7}$$

$$i_{neq,in} = \begin{cases} C \cdot v_{n,out}\big|_{i_{in}=0,i_{out}=0} & \text{if} \quad C \neq 0 \\ D \cdot i_{n,out}\big|_{i_{in}=0,v_{out}=0} & \text{if} \quad C = 0 \wedge D \neq 0 \\ 0 & \text{if} \quad C = 0 \wedge D = 0 \end{cases} \tag{7.8}$$

An Example

As an example we will calculate the equivalent noise sources for the AGC amplifier case l encountered in chapter 4. This circuit has 4 non-zero transmission parameters and Table 7-3 shows these, along with the class to which it belong, the output variable, and the noise contribution of $i_{n,ga}$ and $i_{n,gb}$ to the output variable. Using the data from Table 7-3, and eqns. 7.7 and 7.8, the following results are found:

$$\overline{v_{neq,in}^2} = A^2 \cdot \overline{v_{n,out}^2}\Big|_{v_{in}=0,i_{out}=0} = \frac{g_b^2}{(g_a+g_b)^2}\left(\left(\frac{1}{g_b}\right)^2 \overline{i_{n,ga}^2} + \left(\frac{1}{g_b}\right)^2 \overline{i_{n,gb}^2}\right) \tag{7.9}$$

$$\overline{i_{neq,in}^2} = C^2 \cdot \overline{v_{n,out}^2}\Big|_{i_{in}=0,v_{out}=0} = \frac{(g_a g_b)^2}{(g_a+g_b)^2}\left(\left(-\frac{1}{g_a}\right)^2 \overline{i_{n,ga}^2} + \left(\frac{1}{g_b}\right)^2 \overline{i_{n,gb}^2}\right) \tag{7.10}$$

Figure 7-3a and Figure 7-3b show the circuit under transmission parameter test condition A and C respectively, used to obtain this result. With some practice, the equations can be derived from Figure 7-4a and Figure 7-4b by inspection: e.g. for Figure 7-4a, noise current $i_{n,ga}$ flows through resistance $1/g_b$, producing $v_{n,out}$ (first term between brackets in eqn. 7.9). Dividing by the voltage gain $(g_a+g_b)/g_b$ (or multiplication with A) and squaring the whole

term renders the contribution to $v^2_{neq,in}$. Similar reasoning renders the other noise contributions.

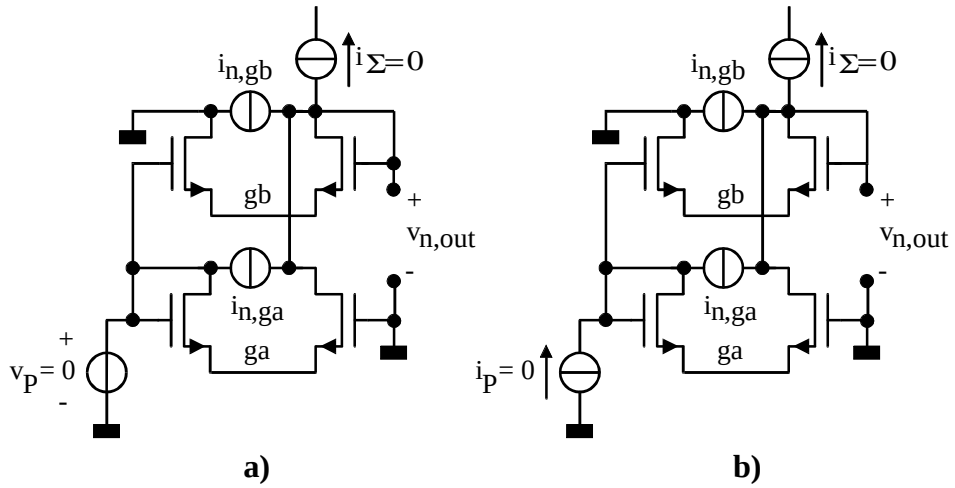


Figure 7-4: The equivalent circuits used for the calculation of the noise contributions for AGC amplifier case l of chapter 4: a) Transmission parameters test condition A; b) Transmission parameters test condition C.

Transmission parameter	Class	Output Variable s_{out}	$s_{n,out}/i_{n,ga}$ (Table 7-1)	$s_{n,out}/i_{n,gb}$ (Table 7-2)
$A = g_b/(g_a+g_b)$	$\{V_P,I_\Sigma\}$	$v_{in}-v_b$	$1/g_b$	$1/g_b$
$B = 1/(g_a+g_b)$	$\{V_P,V_\Delta\}$	i_Σ	1	1
$C = g_ag_b/(g_a+g_b)$	$\{I_P,I_\Sigma\}$	v_a-v_b	$-1/g_a$	$1/g_b$
$D = g_a/(g_a+g_b)$	$\{V_\Delta,I_P\}$	i_Σ	$-g_b/g_a$	1

Table 7-3: Classification data on the circuit of Figure 7-4: the transmission parameters, classification, output variable and output noise contributions.

Note that $v_{neq,in}$ and $i_{neq,in}$ are correlated. Therefore, the sign of the individual noise contributions is also listed in Table 7-3. If we assume for instance that a source with a source resistance R_s is connected to the input of the transactor, and calculate the total equivalent noise $v_{neq,Rs}$ in R_s, both $v_{neq,in}$ and $i_{neq,in}$ contribute to that noise. By means of superposition of the noise contributions, taking into account correlations, it is found that:

$$\overline{v^2_{neq,Rs}} = \overline{v^2_{n,Rs}} + \left(\frac{1-g_bR_s}{g_a+g_b}\right)^2 \overline{i^2_{n,ga}} + \left(\frac{1+g_aR_s}{g_a+g_b}\right)^2 \overline{i^2_{n,gb}} \qquad (7.11)$$

Remarkably, according to the equation, the noise contribution of $i_{n,ga}$ can be nullified for $g_bR_s=1$. The noise cancellation is illustrated in Figure 7-5 for short-circuited and open output. A fraction $\gamma \cdot i_{n,ga}$ of $i_{n,ga}$ flows to the output, but also through resistor R_s, resulting in a voltage $\gamma \cdot i_{n,ga}R_s$. This voltage renders a fully correlated noise current in the upper differential pair equal to $g_bi_{n,ga}R_s$. If $g_bR_s=1$, this current is equal to $\gamma \cdot i_{n,ga}$, and the short-circuit output noise current $i_{n,out}$ becomes zero (all of $i_{n,ga}$ flows through $VCCS_b$). For a voltage output two anti-phase voltages are added cancelling each other for $g_bR_s=1$.

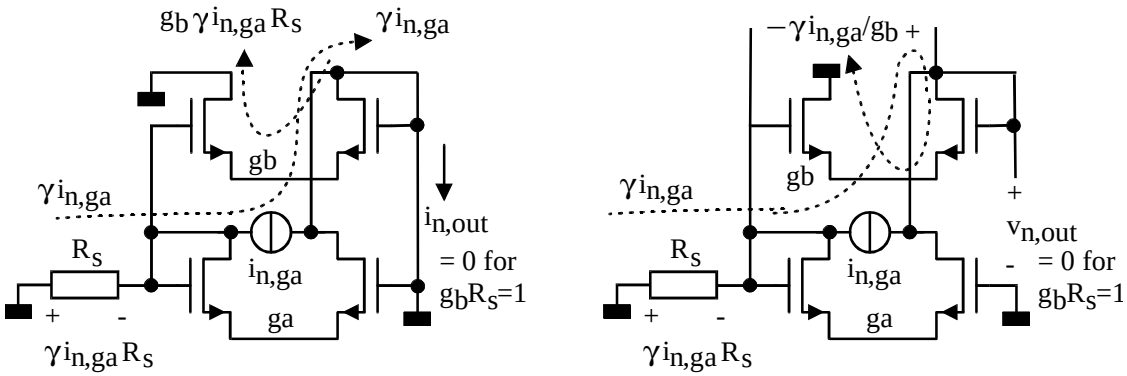


Figure 7-5: Noise cancellation: the effect of $i_{n,ga}$ on $i_{n,out}$ and $v_{n,out}$ is zero for $g_bR_s=1$.

7.4 Summary and Conclusions

The noise behaviour of 2VCCS circuits has been analysed in a systematic way. The main results that were achieved are summarised below.

- A noise current source $i_{n,ga}$ and $i_{n,gb}$ in parallel to the output of $VCCS_a$ and $VCCS_b$ has been used to model the noise of the VCCSs. For every class of 2VCCS circuits the noise contribution of $i_{n,ga}$ and $i_{n,gb}$ to output variable $s_{n,out}$ was calculated, under transmission-parameter test-conditions.
- The output noise contributions found in this way are not independent. The values found for test-condition A and B on the one hand, and for C and D on the other, have a ratio determined by the output impedance of an transactor.
- As a result, only noise contribution for case (A or B) and case (C or D) are needed to calculate the equivalent input noise sources for a transactor. Suitable multiplications with transmission parameters render the equivalent input noise.
- In some cases, cancellation of noise contributions may occur. This happens for example in the circuit shown in Figure 7-5.

8

Application Examples II

8.1 Introduction

This chapter presents applications of the classification and analysis techniques developed in the chapters 5, 6 and 7. Section 8.2 and 8.2.8 deal with the *classification* of linear CMOS transactors described in literature. It will be shown that many of them can be considered as circuits with 2 VCCSs as covered by this thesis. Mainly linear V-I converters or transconductors will be discussed in section 8.2, as these can be used to implement VCCSs in the circuit graphs generated in chapter 3. Furthermore some other transactors, especially amplifiers will be discussed in Section 8.2.8. The *analysis* of VCCS circuits is exemplified in section 8.4 and section 8.5. In section 8.4, the dynamic range of an important class of V-I Kernels is compared: the Kernels consisting of 2 matched MOS Transistors. The analysis techniques of chapter 6 and 7 will be used for this purpose. Finally, section 8.5 deals again with the AGC amplifier design problem discussed in chapter 4. Analytic expressions for the performance of AGC circuits will be derived, to predict, compare and understand the behaviour of transactors.

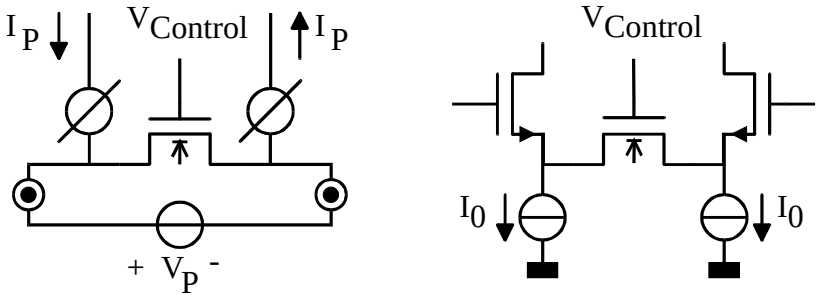
8.2 Classification of Published Transconductors

In the introduction of this thesis it was stated that a lot of individual papers on linear transconductor circuits exist. A few of these papers discuss different approaches [66, 74, 34, 92, 114]. However, different classes of circuits are often defined arbitrarily in these papers. In the paper of Groenewold [34], a more systematic approach is chosen. However, it mainly deals with single MOST devices. The classification system of chapter 5 will now be used to classify transconductor circuits systematically. As in [34], the focus will be on the "Functional Kernel" of the circuits. However, now the accent is on Multiple Kernel Devices and on major differences in circuit implementations. The circuits will be discussed class by class, to stress resemblances between circuits.

8.2.1 $\{V_P\}$ Circuits

In chapter 6 it was shown that 2VCCS circuits can have advantages compared to 1VCCS circuits, e.g. 2^{nd} order distortion cancellation. Nevertheless, for some applications, e.g. with

low level signals and/or low distortion requirements, the use of a single V-I conversion element ({V_P} class) is sometimes acceptable. Especially, transconductors based on the resistance of a triode MOST have been proposed [43]. Figure 8-1a illustrates the principle of operation: 2 nullors copy the input voltage V_P to a conversion resistor (r_{ds} of the MOST), and also convey the resulting current I_P to the output. The nullor can be implemented by a source follower MOST with a large W/L and large current for acceptable distortion [43]. Alternatively, an additional OPAMP can be used.



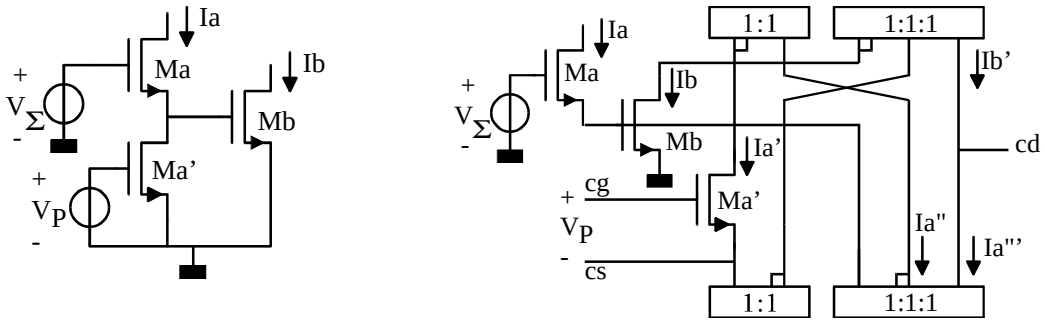
a) b)

Figure 8-1: LVCCS based on a {VP} circuit with passive triode MOST. a) Principle of operation ($V_P \rightarrow I_P$); b) Practical implementation [43].

Other VCCS approximations can also be used (see also the Kernel Devices in [34] and the basic conversion elements in [130]). As these have mainly been used in differential circuits (e.g. {V_Σ,V_Δ} and {V_Δ,I_Σ} class circuits), they will be discussed there.

8.2.2 {V_P,V_Σ} Circuits

A class of circuits exploiting the square-law behaviour of a stacked pair of saturated MOSTs (SVCCS), has been proposed by Bult and Wallinga [49,54]. The basic circuit is shown in Figure 8-2a, where the MOSTs Ma and Mb are the 2 stacked SVCCSs. The other MOST Ma' operates as a voltage copier together with Ma, copying voltage V_P to V_{GSa} ({V_P,I_Δ} circuit with I_Δ=0).



a) b)

Figure 8-2: {V_P,V_Σ} V-I Converter proposed by Bult et al ($V_P \rightarrow I_\Delta$) [49,54]; b) Linear COMFET derived from this circuit ($V_P \rightarrow I_\Delta$) [88,106].

The same functional kernel was later proposed as the hart of a so-called Linear Composite FET (COMFET) circuits by Cheng and Toumazou [88,106], shown in Figure 8-2b. The voltage copier is again implemented by Ma' and Ma, however with 4 additional current

mirrors. In this way overall a versatile floating COMFET with "composite" gate, source and drain terminals "cg", "cs" and "cd" results. It has a linear V-I characteristic from V_P (= $V_{cg,cs}$) to the composite drain and source current I_Δ (= I_a'''-I_b'). The transconductance is tuneable by means of V_Σ. Unfortunately, the flexibility comes at the cost of significant additional current mirror errors and noise [106].

In Figure 8-3, a circuit is shown which can be considered as a V-I converter consisting of two $\{V_P,V_\Sigma\}$ circuits, combined in a $\{V_\Sigma,V_\Delta\}$ configuration, with V_Δ as differential input voltage and I_Δ as output [95,116]. The V_P and V_Σ variables of the 2 circuit halves are indicated with single and double quotes. The $\{V_\Sigma,V_\Delta\}$ voltage drive condition is approximated, by driving the circuit with the drain currents of a differential pair. Thus, overall a transconductor with floating input results [95]. To save voltage headroom, a folded-cascode structure has been proposed by den Besten et al [116]. If voltage-headroom is no problem, CMOS pairs can be used for Ma and Ma' as reported in [95].

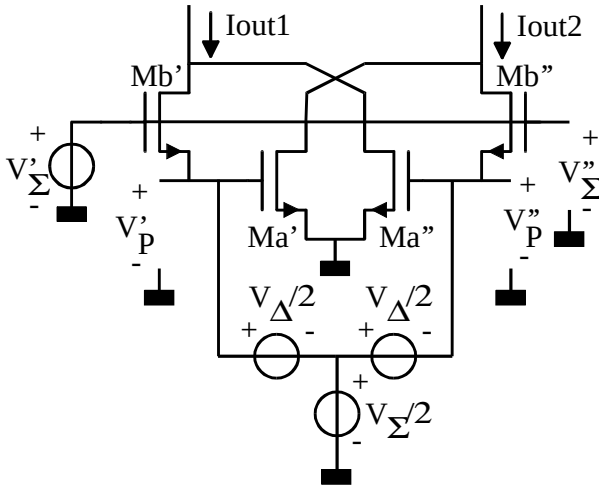


Figure 8-3: Two $\{V_P,V_\Sigma\}$ circuits in a $\{V_\Sigma,V_\Delta\}$ configuration ($V_\Delta \rightarrow I_\Delta$) [116].

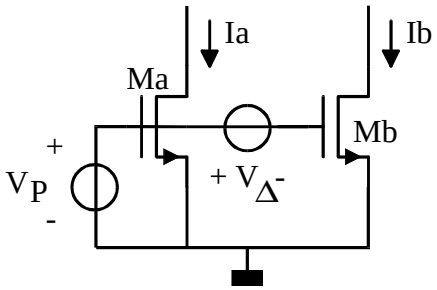
An alternatively way of looking at the circuit of Figure 8-3, is as a current gain-cell with non-linear current transfer characteristic, which is roughly the inverse of the long-tail pair V-I characteristic. With currents as input, the circuit halves can be classified as $\{V_\Sigma,I_P\}$ circuits.

8.2.3 $\{V_P,V_\Delta\}$ Circuits

A $\{V_P,V_\Delta\}$ circuit with two SVCCSs as shown in Figure 8-4, has been proposed as new by Wang and Guggenbühl [63,64]. However, the functional kernel was mentioned earlier by Torrance et al ([40], one half of Fig. 9 in their paper). Furthermore, it was described by Bult in general terms as a four-transistor multiplying core [54], shown in Figure 8-5. Assuming SVCCSs, the output current of this multiplier core is given by:

$$I_{out} = I_1 - I_2 + I_3 - I_4 = 2kV_{in1}V_{in2} \qquad (8.1)$$

As this result is independent of the biasing (V_s cancels in the expressions), a current source I_s can be connected to V_s, so that a floating input is available. The transconductor proposed by Wang is just this circuit, where V_{in1} is the so-called "Bias-offset" [64].



a) b)

Figure 8-4: a) {V_P,V_Δ} circuit proposed by Wang and Guggenbühl [63,64] and the transconductor based on it (b), which is a specific case of Figure 8-5.

As the four-transistor multiplying core of Figure 8-5 consists of 4 SVCCSs, it is not covered by the 2VCCS circuit classification, unless it can be separated in two independent 2VCCS circuits. This is possible if the source voltage V_S is fixed as in the transconductor of Szczepasnski et al [128]. If a tail current source is used as in Figure 8-4b, a separation is not possible, as all 4 MOSTs interact at the common source node. The same observation holds for 4 SVCCS circuits proposed by Czarnul [71,72] and Huang and Ismail [105]. Nevertheless, parts of these circuits can be tackled, e.g. one half of Figure 8-4b, which can be classified as a {V_P,V_Δ} circuit and analysed accordingly.

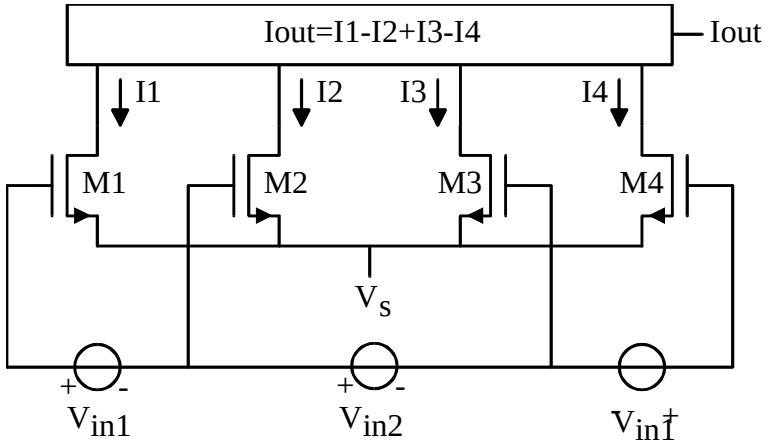


Figure 8-5: Four-Transistor Multiplying Core [54, Figure 3.8].

In contrast, some other {V_P,V_Δ} circuits *can* be separated it in 2 independent 2VCCS circuits. This holds for the circuit of Figure 8-4b, if the common source node is grounded as proposed by Wu and Schaumann [86]. This circuit can actually be classified as a {V_Σ,V_Δ} combination ($V_\Delta \rightarrow I_\Delta$) of two {$V_P$,$V_\Delta$} circuits ($V_\Delta \rightarrow I_\Delta$) using NMOSTs as SVCCSs. Another circuit using the same principle, but with source V_Δ connected between two MOST-sources, instead of two gates, was proposed as a part of a V-I converter by Adams et al [83]. The circuit is preceded by a voltage copier, consisting of a differential pair and 2 self-connected MOSTs, thus overall implementing a V-I converter with floating input. Unfortunately the additional voltage copier introduces extra noise and inaccuracies. Later, Raut proposed a "novel VCT" [101], which has actually the same functional kernel as the circuit of Adams et al [83], with current mirrors added for current copying/subtraction.

Apart from the above described $\{V_P,V_\Delta\}$ configurations of elementary conversion elements, any two transconductors can be used in $\{V_P,V_\Delta\}$ circuits with $V_P \rightarrow I_\Delta$ to enlarge the transconductance control range. This is sometimes referred to as "current differencing" or just "cross-coupling". The multiplier proposed by Qin and Geiger [140], which has been used in variable-gain amplifiers [121] can be considered as a such a $\{V_P,V_\Delta\}$ combination of two long-tail pair transconductors (see Figure 8-15). Similar combinations of transconductors based on triode MOSTs acting as gate-controlled resistors have been proposed by Czarnul [43,45], where source-followers approximate the required nullor as Figure 8-1b. Two different configurations are possible, well-known in bipolar form: one with 2 current sources and a single triode MOST in a so-called π-configuration [43, see also Figure 8-1b], and another one with 1 current-source and 2 triode MOSTs in T-configuration [45].

8.2.4 $\{V_\Sigma,V_\Delta\}$ Circuits

The quarter-square principle, discussed in chapter 1, renders a multiplication of the sum V_Σ and difference V_Δ of the input voltages of 2 squarers. By keeping one of the variables constant, a linear transconductor is obtained. A solution with grounded MOST squarers was proposed by Torrance et al [40]. Viswanathan proposed a floating version shown in Figure 8-6a, where $V_\Delta/2$ is the input voltage and the sources with value $V_\Sigma/2$ are for biasing (note that only half of the value of V_{gsa}-V_{gsb} is present between then gate terminals). The floating voltage sources $V_\Sigma/2$ are implemented using series feedback [42] (see Figure 8-6b).

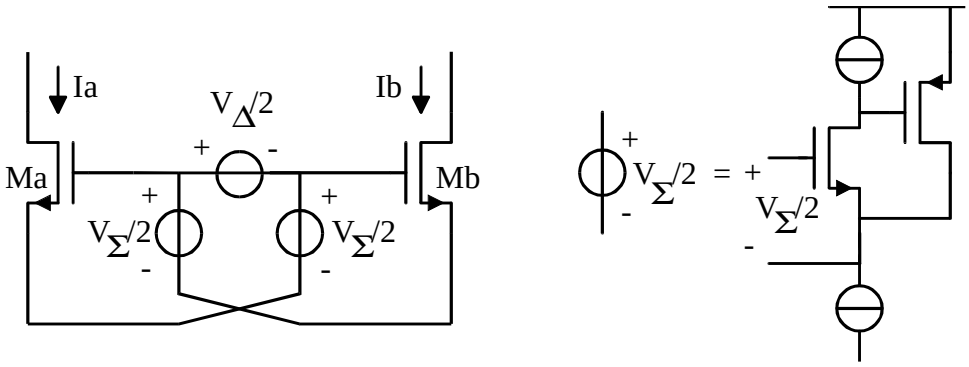
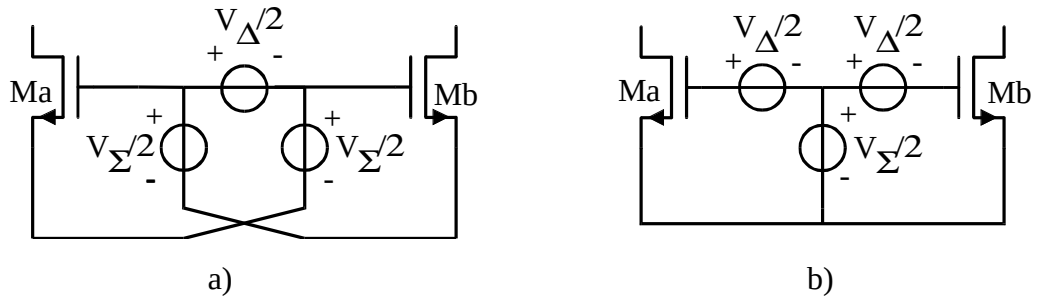


Figure 8-6: Linear Transconductor proposed by Viswanathan et al [42].

The same functional kernel was later used by Filho et al [62], however with a positive feedback loop with current mirrors that keeps the current constant (current bootstrapping). It has been proposed again later by Li et al [109]. In the above mentioned circuits, the input voltage between the gate-terminals is equal to $V_\Delta/2$ (Figure 8-7a). An alternative configuration with input voltage V_Δ is shown in Figure 8-7b. An implementation of the latter principle, as proposed by Wilson et al [69,92] uses two differential pairs to detect the input common voltage level ($\{V_\Sigma,I_\Delta\}$ circuit, $V_\Sigma \rightarrow V_\Sigma$-$V_P$) and buffers this to the common source node of a differential pair, using the buffer of Figure 8-6b.

Yet another implementation of a $\{V_\Sigma,V_\Delta\}$ circuit uses a common detector with source followers and two resistors and an OPAMP that forces the common source node equal to the common-detector voltage by means of the tail current source of a long-tail pair [89].

The detrimental effect of the tail-current variation on the differential output current is compensated to first order by a feedforward compensation loop, so that a large-swing is obtained (3 Volt with 5 Volts supply [89]).



a) b)

Figure 8-7: Two different configuration of a {V_Σ,V_Δ} circuit: a) V_Σ is split into 2 halves; b) V_Δ in split into 2 halves.

Torrance et al [40] and later Klumperink et al [58, 91] proposed to use voltage copiers (2 differential pairs in $\{V_P,I_\Delta\}$ combination, $I_\Delta=0$, $V_{P1}\rightarrow V_{P2}$), in front of 2 grounded squarers, to implement the voltage sources with value $V_\Delta/2$ in Figure 8-7b. The phase shift of the resulting transconductor depends on the bandwidth of the voltage copier and can be tuned independent of the transconductance. By this means, Q-tuning in programmable filters is easier [91]. Unfortunately, the voltage copiers also seriously degrade the noise behaviour, unless significant voltage gain can be applied there (low input-voltage swing).

Instead of multiplying the input voltage by ½, it has also been proposed to pre-process the input signal so that a weighted sum of ¾ and ¼ of the input terminal voltages is supplied to the squarers [76]. In this way the maximum voltage on the squarer is 25% smaller, resulting in a (modest) increase of the transconductance control range (10-20%). However, quite some additional circuitry and current is needed.

Park and Schaumann [47] proposed to use a CMOS pair ($\{V_\Sigma,I_\Delta\}$ circuit consisting of a NMOST and PMOST with $I_\Delta=0$) as an SVCCS instead of a single MOST. With 2 of these pairs a single ended transconductor is possible as shown in Figure 8-8a.

Seevinck and Wassenaar used the same CMOS pairs to implement a differential transconductor [50]. Their paper shows that such a CMOS pair can be viewed as a SVCCS with two high-ohmic current control nodes. If the MOSTs in Figure 8-6 are replaced by CMOS pairs, the $V_\Sigma/2$ sources no-longer "see" a low-ohmic source of a MOST but a gate [50], so that they can be implemented by a current source and CMOS pair (Figure 8-8b). The main drawback of the structure is the large required voltage, because of the stacking of gate-source voltages, and also because of the body effect. This is a severe problem with decreasing supply voltages, especially for CMOS pairs, since commonly only 1 of the two types of MOS devices can be positioned in a floating well, allowing for well-to-source strapping. Instead of CMOS pairs and single MOSTs, also combinations of a Bipolar and MOS Transistors can be used [90]. Because of these different implementations of SVCCSs, many different variations on the above discussed circuits can be devised [e.g. see 131].

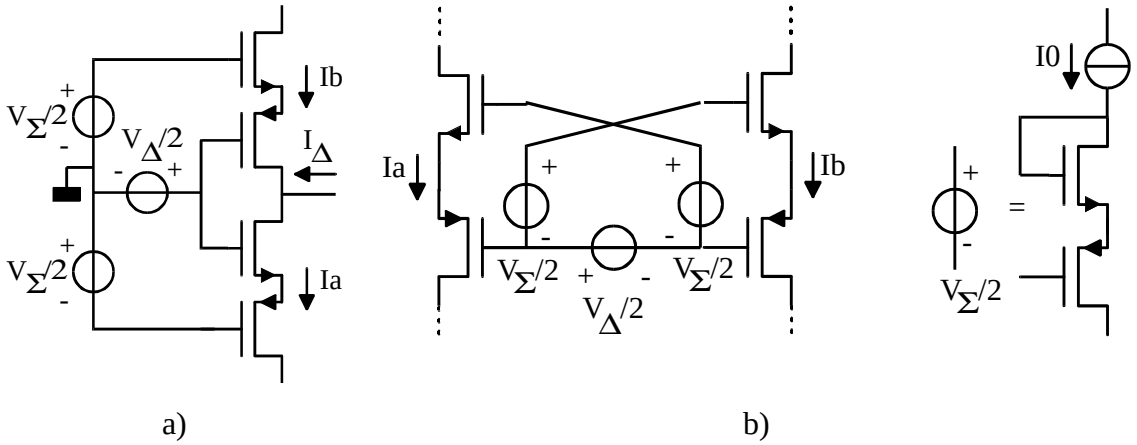


Figure 8-8: a) Single-ended {V_Σ,V_Δ} transconductor based on 2 CMOS pairs [47]; b) Transconductor of Figure 8-6 implemented using CMOS pairs [50].

Another {V_Σ,V_Δ} transconductor, shown Figure 8-9, was proposed by Nauta and Seevinck [56]. It uses a CMOS inverter as transconductor, with $V_{DD}=V_\Sigma$ as the transconductance control variable. The NMOST and PMOST can be considered as SVCCSs, with ideal second order distortion cancellation for $k_N=k_P$. The absence of internal signal carrying nodes results in very low excess phase, so that the transconductor is useful for VHF filters.

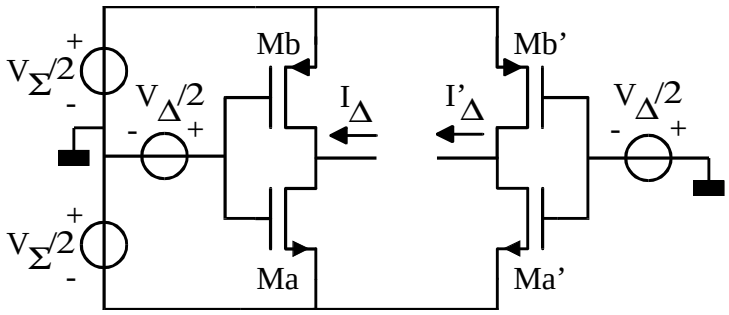


Figure 8-9: CMOS inverters used to implement a linear transconductor [50].

Non-saturated MOSTs have also been used frequently in a balanced {V_Σ,V_Δ} configuration. Especially transconductors using triode MOST at constant V_{DS} have been proposed [41, 55, 67, 70]. The circuits differ mainly in the way V_{DS} is kept constant. Usually this is done by means of feedback [55, 67, 70]. Alternatively a wide MOST or a BJT is sometimes used as a cascode device, approximating the constant V_{DS} goal.

8.2.5 {V_Σ,I_Δ} Circuits

In some publications, the distortion advantage of using a series connection of two devices has been exploited (see also chapter 6). Torrance et al [40] proposed a folded series connection of differential pairs as shown in Figure 8-10. The input voltage is divided over the series elements, leading to an increased intercept voltage and reduced overall transconductance. Recently, a related circuit technique was proposed for use in weak inversion [118]. It was shown that the dynamic range can be preserved or even slightly improved (at the cost of additional offset and power consumption).

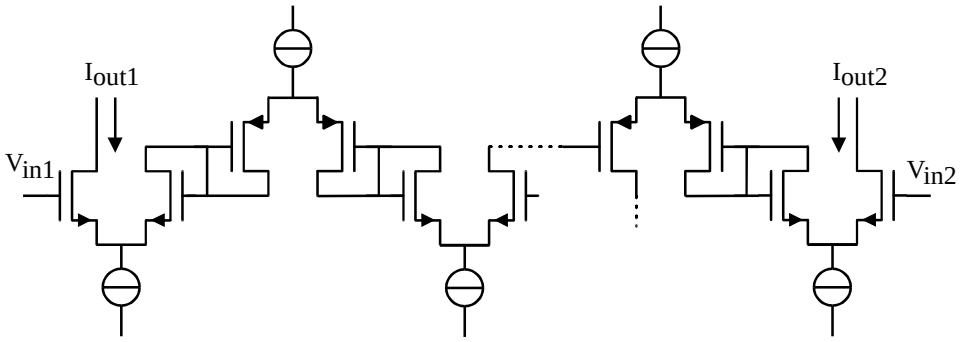


Figure 8-10: Series connection ({V_Σ,I_Δ} class) of differential pairs, reducing distortion and transconductance.

A further example of a {V_Σ,I_Δ} combination of VCCSs was already mentioned: the CMOS pairs used in Figure 8-8a and Figure 8-8b. In fact it can easily be shown that any {V_Σ,I_Δ} combination of 2 SVCCSs with I_Δ=0 forms a new SVCCS (e.g. two stacked NMOSTs [91]). Since each of the stacked MOSTs only experiences part of the voltage swing, this results in a reduction of the distortion due to mobility reduction.

Another example of a {V_Σ,I_Δ} combination of transconductors was proposed by Silva-Martinez et al [85], applied to 2 transconductors proposed by Krummenacher and Joehl [51]. The latter transconductor is similar to the circuit of Figure 8-1b, however with two parallel triode MOSTs, with the gates connected to the input voltage terminals. The aspect ratios in the circuit can be optimised to obtain a 3rd order distortion minimum, due to the interaction between the triode and saturated MOSTs. Since the triode MOSTs themselves don't behave like VCCSs, this circuits can not be classified as a 2VCCS circuit. The same observation holds for a transconductor proposed by VanPeteghem [66]. A disadvantage of these linearisation techniques is that they rely strongly on details of the device transfer characteristics.

8.2.6 {V_Δ,I_Σ } Circuits

A matched differential pair of saturated weak or strong inversion MOSTs, biased by a tail current source is probably the best known V-I converter. Formally it can be classified as a {V_Δ,I_Σ} with SVCCSs or EVCCSs. Instead of using the gate of a MOSFET, the back-gate can also be used [79], provided that the MOSTs have separate floating wells.

Active triode MOSTs can also be used in a {V_Δ,I_Σ} configuration [e.g. 84,125]. Voltage V_{DS} is kept constant by means of feedback [125] or a compensation mechanism [84].

Instead of using matched transistor pairs, deliberately mismatched pairs can be used in parallel, adding the currents [e.g. 68]. In a bipolar version this was proposed by Tanimoto et al [87]. If the aspect ratios are suitably chosen, much larger input voltage ranges than for a single pair can be achieved. However, the achievable linearity is limited by mismatch. Formally such circuits can be classified as {V_P,V_Δ} combinations ($V_P \rightarrow I_\Sigma$) of {V_Δ,I_Σ} circuits ($V_\Delta \rightarrow I_P$), and analysed accordingly.

Assuming that two matched SVCCSs are used in a $\{V_\Delta,I_\Sigma\}$ configuration, a further linearisation is possible by adding a quadratic term to I_Σ as shown in Figure 8-11 (chapter 6, {V,I} class with SVCCS).

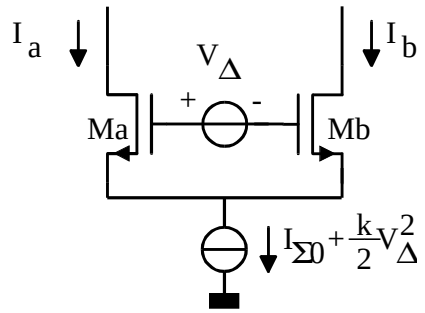


Figure 8-11: Linearisation of a $\{V_\Delta,I_\Sigma\}$ pair with SVCCSs by a quadratic tail current.

This technique was used by Nedungadi in a CMOS V-I converter shown in Figure 8-12 [38, fig. 3a]. Transistor M6 and M7 are the actual V-I conversion transistors ($\{V_\Delta,I_\Sigma\}$). Transistor M1-M4 constitute two mismatched $\{V_\Delta,I_\Sigma\}$ pairs with a k-ratio of 1:m (see Figure 8-12), that deliver a quadratic current (sum of the currents I_{D1} and I_{D2}), which is conveyed to the tail current of M6-M7 by means of a level shift transistor M5. For ideal SVCCSs, Nedungadi found an optimum value of m=2.155.

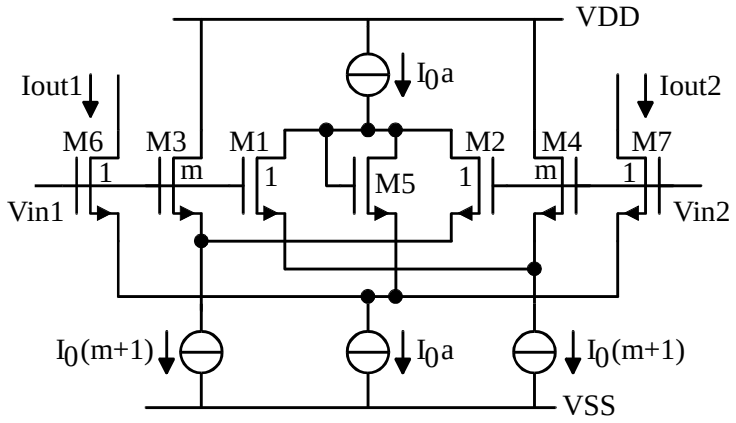


Figure 8-12: Transconductor due to Nedungadi et al, with a quadratic term in I_Σ [38].

The quadratic tail current principle has also been used by Bult and Wallinga in another implementation [49,54], in which a copy of the V-I converter output current is processed by a current squarer ($\{V_\Sigma,I_\Delta\}$ circuit, $I_\Delta \rightarrow I_\Sigma$), to produce the desired quadratic term. Furthermore, Inoue et al proposed to use a strongly asymmetrical differential pair as a squarer for this purpose [82] (one transistors acts as voltage buffer, the other as SVCCS). Kim et al proposed a triode/saturation MOST combination producing the desired square-law term [99]. Other squarers with resistors and MOSTs are possible [119,122,123] and were used by Kimura in a transconductor [119,122].

Somewhat aside it is noted that the quadratic tail current principle can also be used to cancel 3rd order distortion in differential pairs with other device characteristics than the SVCCS, with another proportionality constant for the quadratic term. However, an important problem of the technique is to guarantee that the quadratic term has the optimum magnitude over temperature- and IC-processing variations.

8.2.7 Switched Variable Transconductance Techniques

As motivated in the introduction, this thesis concentrates on continuously electronically variable VCCS circuits. On the other hand, several interesting circuits based on switched techniques have been proposed. Since these can also be used to implement VCCS graphs, some references will be cited here. Transconductors with switchable conversion resistors have for instance been proposed in [108,127]. Furthermore a transconductor with fixed transconductance can be followed by a variable current-gain circuit. Examples of switched current-gain circuits can be found in [59,83,100,104].

A recently proposed interesting V-I conversion technique relies on passive resistors for linearity, but also allows for tuning by means of "soft-switched" triode MOSTs [129, 130]. The switching is soft in the sense that it is done in such a way that the triode MOSTs only weakly degrade the linearity. An advantage of this technique is that it is tolerant to changes in MOST device characteristics, as resistors mainly determine the transfer characteristic.

8.2.8 Summary of V-I Converter Classification

In the previous sections, it was shown that many published transconductor circuits can be classified as 2VCCS circuits. Table 8-1 gives an overview of the results.

Class	References	Functional Kernel Device	Input	Output
$\{V_P\}$	[43,45]	Passive Triode (LVCCS)	V_P	I_P
$\{V_P,V_\Sigma\}$	[54,88,106, 49]	Saturated MOST (SVCCS)	V_P	I_Δ
$\{V_P,V_\Delta\}$	[40,54,63,71,86, 105,128] [43,45]	Saturated MOST (SVCCS) Passive Triode (LVCCS)	V_P	I_Δ
$\{V_\Sigma,V_\Delta\}$	[38,40,58,73,91,62, 69,89,99,107,50,72,81] [68,7] [41,55,67,70,78,]	Saturated MOST (SVCCS) (or $\{V_\Sigma,I_\Delta\}$ pair as SVCCS) Mismatched SVCCSs Active Triode (LVCCS)	V_Δ V_Δ V_Δ	I_Δ I_Δ I_Δ
$\{V_\Sigma,I_\Delta\}$	[40, 47, 50, 72, 81, 86, 91] [85]	Saturated MOST (SVCCS) Krumenacher's LVIC [51]	V_Σ	I_P
$\{V_\Delta,I_\Sigma\}$	[39,48,many others] [79] [38,49,59,82]	Saturated MOST (SVCCS) Backgate driven MOST Saturated MOST (SVCCS) I_Σ-term quadratic to V_Δ	V_Δ V_Δ V_Δ	I_Δ I_Δ I_Δ
-	[54,63,64]	4 SVCCS (2 x $\{V_P,V_\Delta\}$)	V_Δ	I_Δ
-	[51,66]	Triode + Saturated MOST	-	-

Table 8-1: Summary of the classification of Transconductor circuits.

8.3 Variable-Gain Amplifiers

In the previous section transconductors or V-I converters were discussed. In combination with an I-V converter they can be used as a voltage amplifier (V-I followed by I-V) or current amplifier (I-V followed by V-I). A resistor can be used as I-V converter or a passive

triode MOST (electronically variable g_{ds}). Alternatively, an I-V converter can be implemented using a V-I converter, with exchanged input and output signal.

Some examples of voltage and current amplifier will now be discussed to illustrate that they can be considered as combinations of 2VCCS circuits. The examples mainly relate to previous work of the author of this thesis relating to *CMOS current gain-cells*. As Gilbert's bipolar Gain-cell [35], the CMOS cells are large-signal current-difference amplifiers with variable gain. In contrast to the bipolar cells, where signal voltages and currents are nonlinearly related, the CMOS gain cells encompass linear I-V and V-I conversions. A circuit with the same basic structure as Gilbert's gain-cell, but with MOSTs operating as SVCCSs, is shown in Figure 8-13 [61,57]. The underlying principle is the same as in Figure 8-11 and requires the input current to have the algebraic form:

$$I_{in1,2} = I_{in0}\left(1 \pm \frac{\left(I_{in1} - I_{in2}\right)}{4I_{in0}}\right)^2 \tag{8.2}$$

where I_{in0} is the quiescence component of I_{in1} and I_{in2}.

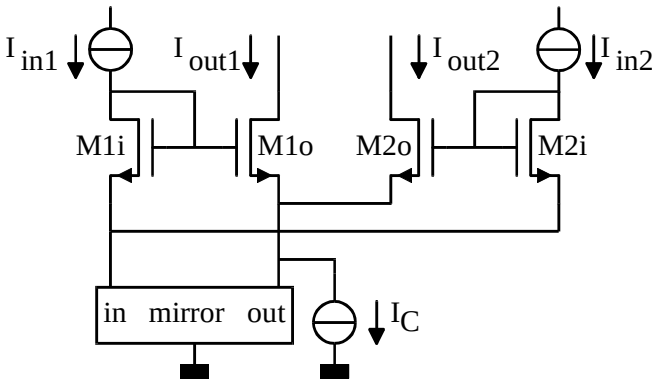


Figure 8-13: A current-gain cell consisting of a linear I-V converter (Mi1,Mi2, if eqn. 8.2 is satisfied) and a linear V-I converter (M1o and M2o) [61].

The input transistors M1i and M2i constitute a $\{I_\Sigma, I_\Delta\}$ circuit ($I_\Delta \rightarrow V_\Delta$) acting as linear I-V converter due to the quadratic component in I_Σ. Such a quadratic I_Σ current is delivered by many $\{V_\Sigma, V_\Delta\}$ and $\{V_P, V_\Sigma\}$ V-I converters based on SVCCSs. The output transistors M1o and M2o constitute a $\{V_\Delta, I_\Sigma\}$ circuit, operating as linear V-I converter ($V_\Delta \rightarrow I_\Delta$), provided that their tail currrent has a suitable quadratic component. This term is available in the input current according to eqn. 8.2 and is copied to the output transistors by the current mirror in Figure 8-13. An additional bias current I_C, that acts as a gain-control current is added to the mirror current. The resulting differential current gain becomes [61]:

$$A_i = \frac{I_{out1} - I_{out2}}{I_{in1} - I_{in2}} = \frac{k_o}{k_i}\sqrt{1 + \frac{I_C}{2I_{in0}}} \tag{8.3}$$

where it is assumed that the current mirror gain is equal to k_0/k_i, and k_i and k_0 are the k-parameters of the input and output transistors. Thus the gain does only depend on a *ratio of k-parameters* (geometic ratio) and *currents*, which is *independent on temperature and IC-processing*. An equivalent voltage biased circuit is also possible [61]. Furthermore, the bandwidth of the circuits remains constant while their gain is varied, implying an increase

of gain-bandwidth product with increasing gain. This property results from the fact that the gate-source capacitance of a MOST is almost bias independent (in contrast to C_{BE} of a bipolar transistor, which increases roughly linear with the bias current resulting in a constant gain-bandwidth product).

The specific required form of the input current limits the use of the above described gain-cell. Furthermore, a cascade of these cells has the same gain-control range then a single cell [77]. In order to solve these problems, alternative cells have been proposed that can handle balanced bi-directional input currents [77,102,111]. Some of these use complementary circuits [77,111], e.g. the circuit of Figure 8-14.

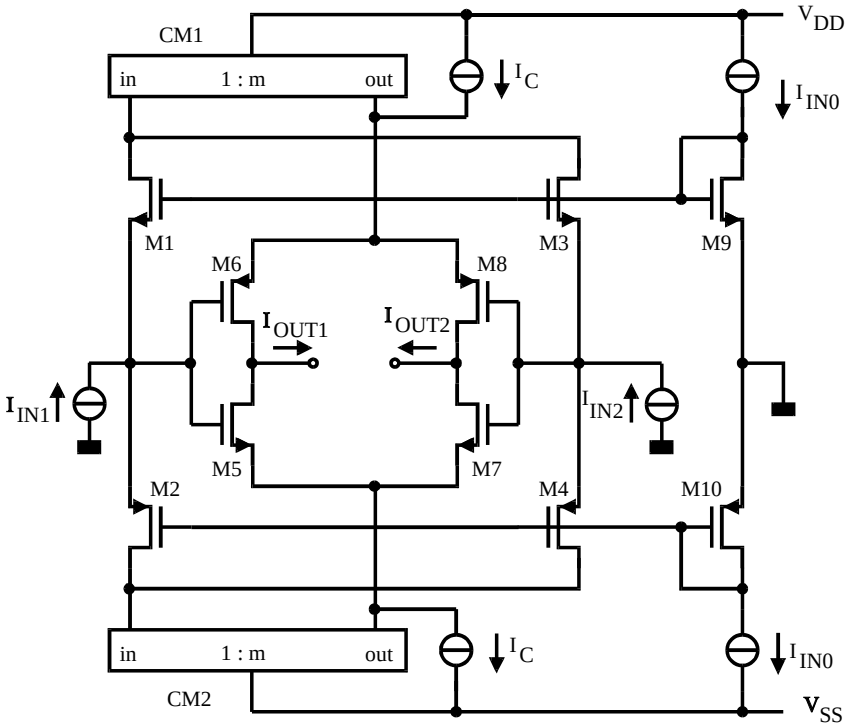


Figure 8-14: Complementary Current Biased Current-Gain Cell [111].

In this circuit, transistors M1-M2 and M3-M4 constitute $\{V_\Sigma,I_\Delta\}$ I-V converter circuits ($I_\Delta \rightarrow V_P$) biased at constant V_Σ by M9-M10 and the bias sources I_{IN0}. If $k_N=k_P$ the relation between I_Δ and V_P (the input voltage) is linear. If $k_N \neq k_P$ some second order distortion occurs, which is however largely cancelled in the balanced structure. Transistors M5-M8 constitute a linear V-I converter, using $\{V_\Delta,I_\Sigma\}$ pairs of SVCCSs with quadratic I_Σ. It can be shown that the desired quadratic term is present in the sum of the currents of the I-V converter transistors [111]. It is copied to the output transistors by 2 current mirrors. Thus the gain-cell has a transfer function similar to that of eqn. 8.2, but with plain bi-directional input currents. Because of the complementary structure, the bias current flows from V_{DD} to V_{SS}, while the input and output currents are bias-free signal currents. This allows the cells to be cascaded easily. A gain-cell with similar input stage, but with voltage biased CMOS inverters as output V-I converters as in Figure 8-9 is also possible [77].

Wang proposed 2 gain-cells with $\{V_\Sigma,I_\Delta\}$ I-V converters, however with 2 equal NMOST SVCCSs instead of complementary MOSTs [102]. A gain-control bias-current is injected at the input, which shows a linear input resistance. As a result, a large gain-variation is

achieved by a relatively small change of bias current (linear gain-control instead of a square-root dependence via I_{IN0} in Figure 8-14).

Apart from current gain-cells, voltage gain-cells can also be constructed using the above described V-I and I-V subcircuits. An example of a variable-gain amplifier with passive resistors as output I-V converter is shown in Figure 8-15 [121]. The upper cross-coupled differential pairs are often used as the core of a multiplier [132,136,140]. They can be classified as $\{V_\Delta,I_\Sigma\}$ SVCCS pairs, combined in a $\{V_P,V_\Delta\}$ configuration ($V_P \rightarrow I_\Delta$, $V_\Delta=0$). The lower pair controls the transconductance of the upper stages and thus the gain. The circuit has a large input range with acceptable distortion at low gain. Moreover it appears to have a phase shift that is almost independent of the gain. This property was exploited to implement a AM suppression circuit with a low AM-PM conversion [123]. It was concluded that the circuit of Figure 8-15 can exhibit a phase shift variation of less than 0.5 degrees at 40MHz over 20dB gain range (2µ BICMOS process).

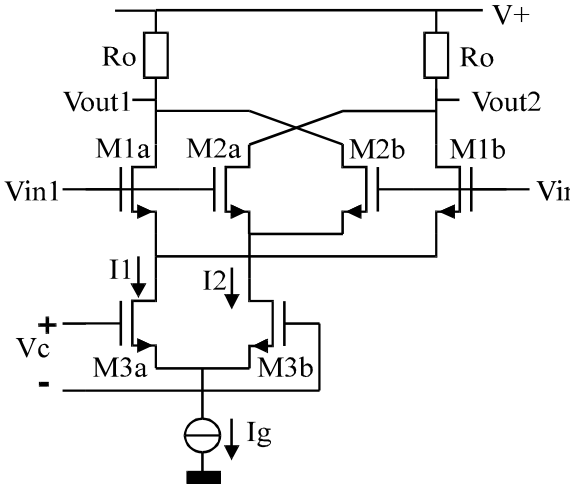


Figure 8-15: MOS variable voltage-gain amplifier with constant phase shift [123].

8.4 Comparison of V-I Kernels with 2 Matched MOSTs

8.4.1 Introduction

As discussed in the previous sections, many papers on MOS transconductor circuits exist. However few papers consistently compare different approaches. As published results relate to different applications of transconductors implemented in different IC-processes, it is hard to asses the relative merits of different V-I conversion techniques. Such a comparison is burdened by many differences in circuit implementation. However, if only the V-I conversion kernel is considered, a comparison is possible. By this simplification an estimate for the achievable performance of classes of transconductors can be found. This will now be shown for an important class of V-I kernels, consisting of 2 matched MOSTs operating as VCCSs[1]. The aim is to identify essentially different approaches, and assess

1 Cascoding is needed, especially for triode MOSTs, but is not included in first order analysis.

their relative merits with respect to dynamic range. This will be done for different operating regions of the MOST.

8.4.2 Systematic Generation of V-I Kernels

All V-I converter Kernels consisting of 2 (MOST-) VCCSs and independent sources will now be generated systematically to find the possible different approaches. As the input voltage V_{in} needs to be an independent variable, only the classes with at least 1 forced voltage need to be considered. Table 8-2 presents these classes.

Class	V_{in}	1st order coeff. Ia,Ib	2nd order coeff. Ia,Ib	3rd order coeff. Ia,Ib
$\{V_P,V_\Sigma\}$	**V_P**	**g_{1a}, $-g_{1b}$**	**g_{2a}, g_{2b}**	**g_{3a}, $-g_{3b}$**
	V_Σ	0, g_{1b}	0, g_{2b}	0, g_{3b}
$\{V_P,V_\Delta\}$	**V_P**	**g_{1a}, g_{1b}**	**g_{2a}, g_{2b}**	**g_{3a}, g_{3b}**
	V_Δ	0, g_{1b}	0, g_{2b}	0, g_{3b}
$\{V_\Sigma,V_\Delta\}$	V_Σ V_Δ	$g_{1a}/2$, $g_{1b}/2$ $g_{1a}/2$,$-g_{1b}/2$	$g_{2a}/4$, $g_{2b}/4$ $g_{2a}/4$, $g_{2b}/4$	$g_{3a}/8$, $g_{3b}/8$ $g_{3a}/8$,$-g_{3b}/8$
$\{V_\Sigma,I_P\}$	V_Σ	0, g_{1b}	0, g_{2b}	0, g_{3b}
$\{V_\Delta,I_P\}$	V_Δ	0, $-g_{1b}$	0, $-g_{2b}$	0, $-g_{3b}$
$\{V_P,I_\Sigma\}$	V_P	g_{1a},$-g_{1a}$	g_{2a}, $-g_{2a}$	g_{3a}, $-g_{3a}$
$\{V_P,I_\Delta\}$	V_P	g_{1a}, g_{1a}	g_{2a}, g_{2a}	g_{3a}, g_{3a}
$\{V_\Sigma,I_\Sigma\}$	V_Σ	*	*	*
$\{V_\Sigma,I_\Delta\}$ @	**V_Σ**	**$g_1/2$, $g_1/2$**	**$g_2/4$, $g_2/4$**	**$g_3/8$, $g_3/8$**
$\{V_\Delta,I_\Sigma\}$ @	**V_Δ**	**$g_1/2$, $-g_1/2$**	**0 , 0**	$\pm\left(\frac{g_3}{8}-\frac{g_2^2}{4g_1}\right)$
$\{V_\Delta,I_\Delta\}$	V_Δ	*	*	*

Table 8-2: Overview of the 11 forcible sets of Kirchhoff relations with at least one voltage relation. The 4 classes with different behaviour are indicated in bold (@= equal g-coefficients; *=not always a unique solution).

The first column shows the set of forced Kirchhoff relations, and the second lists the independent voltage that is used as input. It appears that 3 classes with 2 voltage relations exist ({V,V} sets), each subdivided in 2 cases (2 possible input variables), while 8 classes with a voltage and a current exist ({V,I} sets).

The non-linearity for the classes of V-I Kernels has been analysed symbolically, and Table 8-2 lists the coefficients of the 1st, 2nd and 3rd order terms of I_a and I_b. Taking a single VCCS as reference, we can select cases with essentially different behaviour for further examination. For 6 cases, the coefficients appear to be equal to those of the constituting VCCS (g1, g2, g3), which could have been achieved with just 1 VCCS. For 2 classes ($\{V_\Sigma,I_\Sigma\}$ and $\{V_\Delta,I_\Delta\}$), a unique solution does not always exist. As the author is not aware of any practical circuits based on these classes, these cases are dropped. However, the remaining 6 cases differ essentially from a single VCCS. In fact 4 different types of distortion coefficients are found (printed in bold):

1. $\{V_P,V_\Sigma\}$: constant V_Σ and V_P as input ("balancing"): the 2nd order terms of I_a and I_b have the same sign, while the 1st and 3rd order terms have different signs. Consequently, 2nd order distortion is cancelled, if I_a and I_b are subtracted and $g_{2a}=g_{2b}$ (for matched MOSTs: $V_P=V_\Sigma/2$). Since the 1st and 3rd order terms are both doubled due to subtraction, HD3 remains the same, independent of the VCCS-characteristic. The same behaviour is found for case $\{V_\Sigma,V_\Delta\}$ with V_Δ as input: the cases are equivalent if $V_P=V_\Sigma/2+V_\Delta/2$, which is the usual case (HD2 cancelling).
2. $\{V_P,V_\Delta\}$: constant V_Δ and V_P as input: I_a and I_b have different g-coefficients if the bias-point of $VCCS_a$ and $VCCS_b$ is different. If I_Δ is used as output, the differences of corresponding g-coefficients of $VCCS_a$ and $VCCS_b$ is of concern. As a result, the overall G_m-range is extended at the low end. If $\Delta g_2/\Delta g_1<g_2/g_1$ or $\Delta g_3/\Delta g_1<g_3/g_1$, the linearity is improved. Whether this happens, depends strongly on device characteristics. The behaviour for the $\{V_P,V_\Delta\}$ class is equal to that for case $\{V_\Sigma,V_\Delta\}$, yet now with V_Σ as signal input, provided that $V_P=V_\Sigma/2+V_\Delta/2$.
3. $\{V_\Sigma,I_\Delta\}$: constant I_Δ (usually 0) and V_Σ as input: since the input voltage is divided over two equal devices, the input voltage can be 2 times larger for the same distortion (this holds for both HD2 and HD3). This effect is independent of the device characteristic.
4. $\{V_\Delta,I_\Sigma\}$: constant I_Σ with V_Δ as input: the 2nd order terms are zero for equal biased MOSTs. The 3rd order term now also depends on the 2nd-order term (g_2 dependence). The net result depends on the VCCS characteristic, especially on the sign of the 3rd-order term.

8.4.3 A figure of merit: NDR/I_{SS}

The different V-I Kernels found in the previous section will now be compared with respect to dynamic range DR. To this end, a figure of merit is defined that is closely related to DR/Power: the ratio between *Normalised* Dynamic Range (NDR) and Supply Current (I_{SS}): NDR/I_{SS}. The NDR definition is introduced for easy scaling with application dependent distortion HD3 and noise bandwidth NBW. A (fictitious) normalised condition of HD3=100% and NBW=1Hz is chosen. The accent on third order distortion is motivated by its importance in many applications, as second order distortion is often cancelled by means of balancing (see constant V_Σ case). Scaling with distortion requirements is easy, assuming that HD3 is proportional to V_{in}^2, as is commonly done when defining a 3rd order intercept voltage V_{IP3}. HD3 is then given by:

$$\mathrm{HD3} \approx \frac{g_3}{4g_1}\hat{V}_{in}^2 = \left(\frac{\hat{V}_{in}}{V_{IP3}}\right)^2 \tag{8.4}$$

DR is related in a simple way to NDR, HD3 and NBW:

$$\mathrm{DR} = \frac{\mathrm{NDR}}{\mathrm{NBW}}\mathrm{HD3} \tag{8.5}$$

Dynamic range can be improved by MOS device scaling: doubling device widths quadruples signal power and doubles noise power. Thus dynamic range is doubled at the

cost of doubled current consumption. By dividing NDR by I_{SS} a scaling independent figure of merit is found. Using the above definitions, NDR/I_{SS} becomes:

$$\frac{NDR}{I_{SS}} = \frac{S}{N \cdot I_{SS}}\bigg|_{\substack{HD3=100\% \\ NBW=1Hz}} = \frac{\frac{1}{2} G_m V_{IP3}^2}{4 \cdot k \cdot T \cdot NEF \cdot I_{SS}} \tag{8.6}$$

8.4.4 NDR/I_{SS} Comparison

The NDR/I_{SS} for the 4 different V-I kernels found in section 8.4.2 will now be analysed. Figure 8-16 shows examples of circuit implementations. The 4 kernels will be indicated with no. 1-4 (in figures) or the names given in Table 8-3. The NDR/I_{SS} that will be found can be considered as the *best achievable performance*, since practical circuits contain additional components, that add noise, without improving signal power.

Class	V_{in}	I_{out}	no.	Name
$\{V_P, V_\Sigma\}$	V_P	I_Δ	1 (L1, S1, E1)	"Constant V_Σ"
$\{V_P, V_\Delta\}$	V_P	I_Δ	2 (L2, S2, E2)	"Constant V_Δ"
$\{V_\Delta, I_\Sigma\}$	V_Δ	$I_\Delta/2$	3 (L3, S3, E3)	"Constant I_Σ"
$\{V_\Sigma, I_\Delta\}$	V_Σ	I_P	4 (L4, S4, E4)	"Constant I_Δ"

Table 8-3: The 4 different V-I Kernels for which NDR/I_{SS} will be compared.

Symbolic analysis software (MAPLE) was used to find expressions for NDR/I_{SS}. The results have been verified by simulations. The basic formulas and the method used will be described. In order to be able to calculate NDR/I_{SS} according to 8.6, expressions for G_m, V_{IP3}, NEF and I_{SS} are needed. These expressions depend on the I(V) characteristic of the MOST-VCCS. To cover the regions that are commonly used, 3 different MOST I(V) models are considered as shown in Table 8-4: the LVCCSθ-model (strong inversion, non-saturation, cases **L1-L4**), the LVCCSθ-model (strong inversion, saturation, **S1-S4**) and the EVCCS-model (weak inversion, **E1-E4**). Field dependent mobility is included in the first two models, since it is the main cause of non-linearity in transconductors.

Equations for NEF and NDR/I_{SS} for the 3 models are given in Table 8-4. Using these expressions, and the derivatives of I(V) with respect to V, the supply current, G_m and intercept voltage V_{IP3} can be found (see also eqn. 8.4). NEF for the cases of constant V_Σ, I_Σ and I_Δ, is equal to the value for a single VCCS, since G_m changes with the same factor then the noise current variance. However, for constant V_Δ, it becomes:

$$NEF_{\{V_P, V_\Delta\}} = \frac{g_{1a} \cdot NEF_a + g_{1b} \cdot NEF_b}{|g_{1a} - g_{1b}|} \tag{8.7}$$

In this relation we see that NEF becomes much larger than 1 for small value of g_{1a}-g_{1b}. This happens since the noise remains roughly constant, while the overall transconductance decreases.

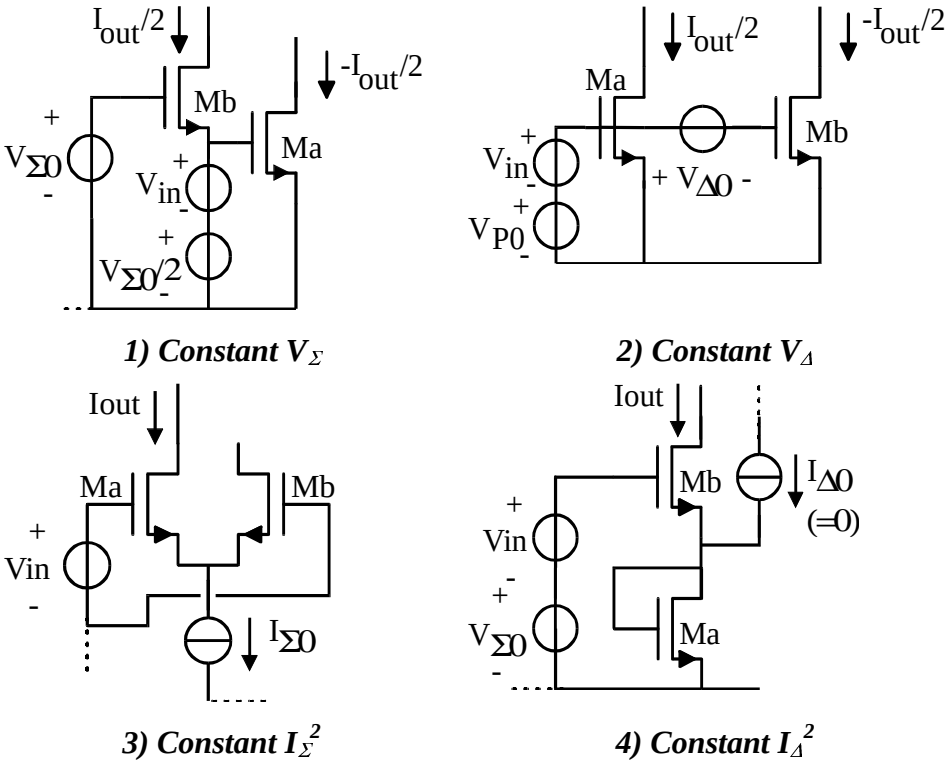


Figure 8-16: Example circuits for the 4 V-I Kernel classes shown in Table 8-3.

	I(V)	**NEF**	**NDR/I_{SS}**
S1-S4 (SVCCSθ)	$k\frac{(V-V_T)^2}{1+\theta(V-V_T)}$	2/3	$\approx\frac{3+6\theta(V-V_T)}{k_BT\theta}$
L1-L4 (LVCCSθ)	$\frac{2k\left((V-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right)}{1+\theta(V-V_T)}$	$\frac{V-V_T}{V_{DS}}-\frac{1}{3}$	$\approx\frac{V_{DS}}{2k_BT(V-V_T)^2\cdot\theta^2}$
E1-E4 (EVCCS)	$I_E\exp^{V/V_E}$	1/2	$\approx\frac{6\cdot V_E}{k_BT}$

Table 8-4: I(V), NEF and NDR/I_{SS} of 3 MOST-VCCS models.

The 4 different V-I Kernels will now be compared using realistic device parameters, derived for MOSTs with W/L=10 in a 1μCMOS process (see Table 8-5). Two values of θ will be considered: $0.1V^{-1}$ for very long channel devices (only mobility reduction due to vertical field) and $0.5V^{-1}$ for minimum channel length devices (also reduced mobility due to lateral field). As is commonly done, the biasing of M_a and M_b is chosen equal and is swept over the range mentioned in Table 8-5, except for M_a for case 2 (constant V_Δ) which is fixed at the maximum bias value. The ratio NDR/I_{SS} as a function of G_m is shown in Figure 8-17 for the EVCCS-model, and in Figure 8-18 and Figure 8-19 for the LVCCSθ- and SVCCSθ-case for low and high θ. As G_m is proportional to W, while NDR/I_{SS} is independent of W-scaling, all curves shift horizontally with W (at the cost of current).

L1-L4	**S1-S4**	**E1-E4**

2 As the VCCS are connected in series, only 1 circulating output current is available.

k = 0.5E-3 A/V	k = 0.5E-3 A/V	V_E = 40 mV
θ = 0.1 or 0.5 V^{-1}	θ = 0.1 or 0.5 V^{-1}	I_E = 1E-15 A
V_{DS} = 0.1..1 V V-V_T = 1 V	V-V_T = 0.1..1 V (V_T = 0.7 V)	V=.45..0.65V

Table 8-5: Numerical values used for MOST parameters (Long and short channel device with W/L=10 in 1 µCMOS process)

The following observations can be made:

- The EVCCS-model renders much lower NDR/I_{SS} than the LVCCSθ- and SVCCSθ-cases. Furthermore, a higher value of θ degrades NDR/I_{SS}, especially for the LVCCSθ-model. This can be understood looking at the NDR/I_{SS} expression in Table 8-4 (θ^{-1} and θ^{-2} dependence). An exception is the S3 case, which is rather insensitive for θ (NDR/I_{SS} even slightly increases for higher θ).

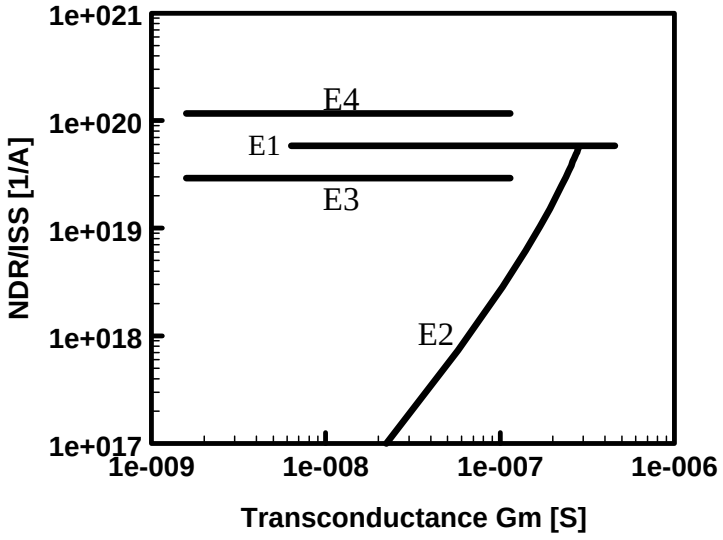


Figure 8-17: NDR/I_{SS} as a function of G_m for the E-model.

- The constant V_Σ case corresponds to a single VCCS apart from a factor 2 increase in G_m. Its main advantage is cancellation of 2nd order distortion.
- Overall, the constant V_Σ and constant I_Δ case with an SVCCSθ-model (S4- and S1-curves) render the best NDR/I_{SS} (high and rather constant), especially for high θ.
- The constant V_Δ cases have an increased G_m-range due to the current subtraction. However, NDR/I_{SS} is drastically degraded for low G_m. For small θ, case S2 has an improved V_{IP3}, which leads to a high NDR/I_{SS}, however only for high G_m.
- The constant I_Δ cases (curves 4) have 4 times lower G_m and 2 times higher NDR/I_{SS} than the constant V_Σ cases (curves 1). However, stacking of devices costs voltage headroom.
- The constant I_Σ cases (curves 3) have a higher V_{IP3} than the constant V_Σ cases, for the LVCCSθ- and EVCCS-model. However, as G_m/I_{SS} is reduced by a factor 4, no NDR/I_{SS} advantage results.

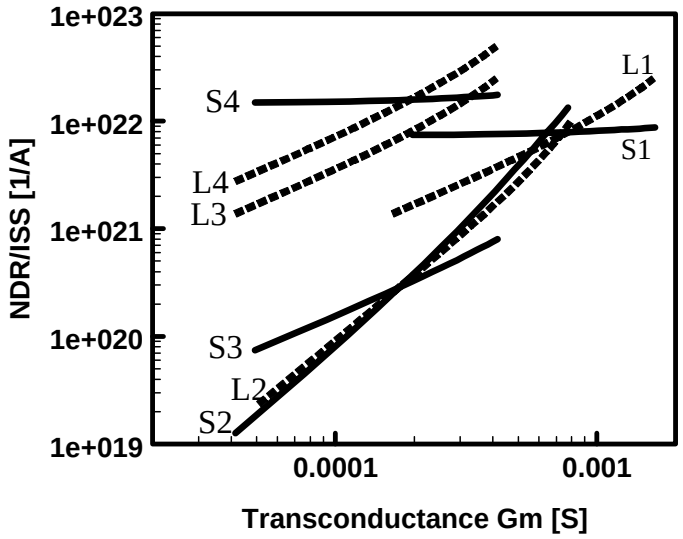


Figure 8-18: NDR/ISS as a function of Gm for the LVCCSθ- and SVCCSθ-model and low θ=0.1 V-1.

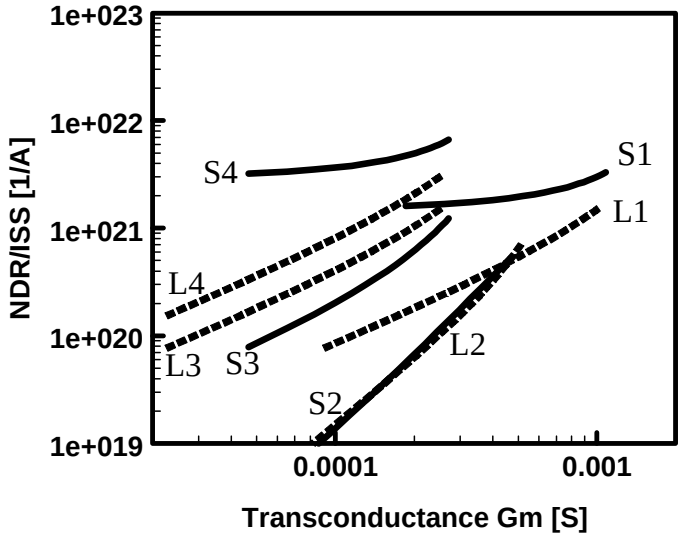


Figure 8-19: NDR/I_{SS} as a function of G_m for the LVCCSθ- and SVCCSθ-model and high θ = 0.5 V^{-1}.

8.5 Design Case Study: AGC-Stage: Part II

In chapter 4, several AGC amplifiers have been synthesised systematically from VCCS graphs and compared by means of numerical circuit simulations. The classification and analysis techniques developed in the previous chapters will now be applied to these AGC circuits, to show how they can be of help to designers. However, it is not claimed that a complete design trajectory of VCCS circuits is readily available. Furthermore, a definite choice and a complete implementation of an AGC circuit on IC-level is beyond the scope of this thesis. The aim of the rest of this section is twofold. First, it will be shown in section 8.5.1 how the design equations are derived. Second, the usefulness of the results will be discussed in section 8.5.2 and 8.5.3.

8.5.1 Description of the Analysis Procedure

The analysis proceeds along the following lines:

1. Classify the AGC circuits using the classification system of chapter 5.
2. Model the VCCSs that are used, (in this case a differential pair) with respect to transconductance, non-linearity and noise, as a function of biasing.
3. Derive expressions for the gain, noise factor, supply current and third order distortion of the AGC amplifiers.

This analysis has largely been automated in a MAPLE program, using the systematic methods discussed in the previous chapters. The results were stored in a data structure, so that the analysis of a particular circuit reduces to the selection of a group of expressions and the substitution of VCCS specific data. Figure 8-20 illustrates the function of the program from a users point of view.

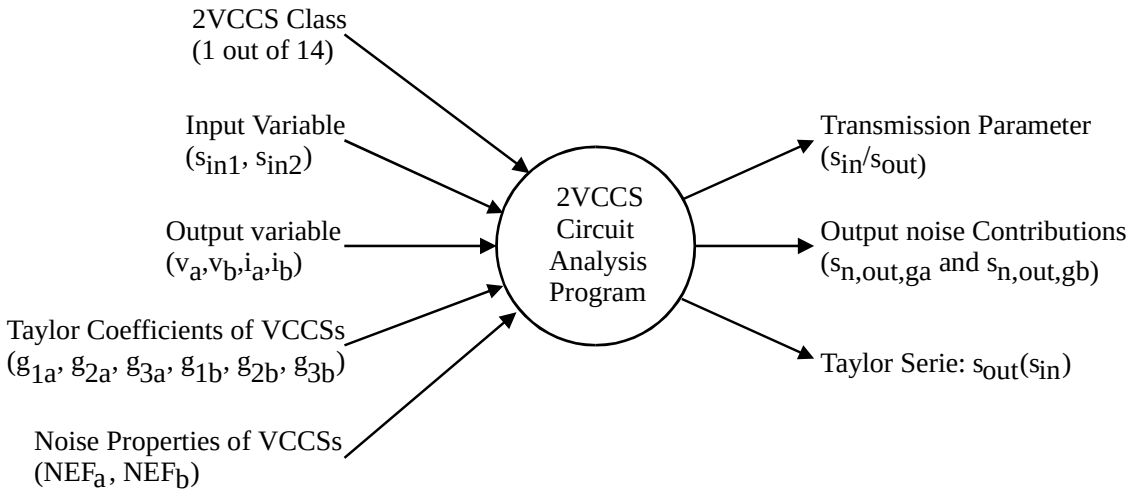


Figure 8-20: Input and output of the 2VCCS Circuit Analysis Program

The selection of output is done by means of the class of the circuit and its input and output variables. The VCCS specific data that are required are the Taylor coefficients and Noise Excess Factor NEF (as a function of the biasing variables). The output of the program is a transmission parameter s_{in}/s_{out}, the output noise contribution of $VCCS_a$ and $VCCS_b$ and the Taylor series $s_{out}(s_{in})$. AGC amplifier case n will now be analysed as an (arbitrary) example and is discussed in detail to illustrate the analysis procedure.

Classification of the AGC amplifiers

The classification of the 2VCCS transactor graphs of Figure 4-17 can be done drawing the VCCS graphs for the transactor in its A-, B-, C- and D-determined mode, as shown in Figure 8-21 for AGC amplifier case n, with 4 non-zero transmission parameters.

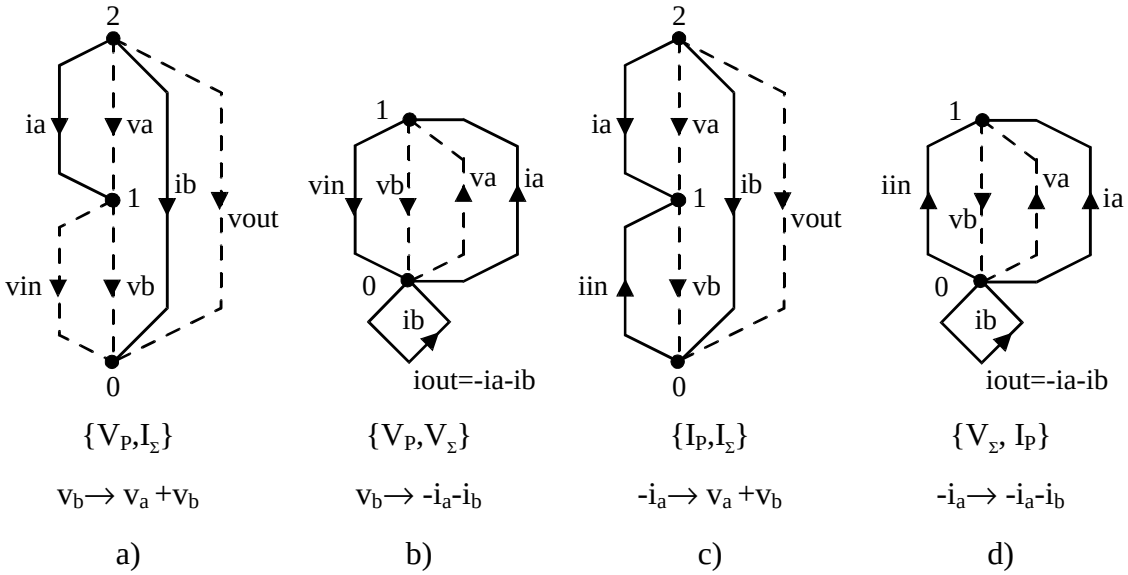


Figure 8-21: Graphs for the 2VCCS transactor used in AGC amplifier case n: a) A-determined; b) B-determined; c) C-determined; d) D-determined.

Looking at these graphs the Kirchhoff relations that are forced are easily identified. For the A-determined case of Figure 8-21a these relations are:

$$v_{in} = v_b \tag{8.8}$$

$$i_a + i_b = 0 \tag{8.9}$$

$$v_{out} = v_a + v_b \tag{8.10}$$

Since a primary voltage (v_b) is forced and a sum of currents, the circuit is classified as a $\{V_P,I_\Sigma\}$ circuit. Its input variable is v_b and its output voltage is v_a+v_b, as shown below the graph in Figure 8-21a. A similar procedure renders the classification data for the B-, C- and D-determined graphs in Figure 8-21. These data are listed in Table 8-6 along with those of the other AGC transactor graphs of Figure 4-17. Note that the data relate to the 2VCCS circuit hart of the AGC stages, and not to possible resistors R_{in} and R_l, that are added to the input or output.

Model the VCCS: Taylor Series and NEF

In chapter 4, differential pairs with equal MOSTs, each biased at half of the tail current, were used to implement VCCSs in the AGC amplifier designs. To model the non-linear transfer characteristic and noise of a differential pair, as a function of its tail current (transconductance control variable), a model for the MOST must be chosen. The SVCCSθ model will be used for this purpose. The biasing point of the MOST in a differential pair depends on its tail current: it is equal to half of that value for zero differential bias voltage. The non-linear behaviour in this bias point is modelled by means of a third order Taylor series (standard MAPLE routine), which renders coefficients g_{1a}, g_{2a}, g_{3a}, g_{1b}, g_{2b}, g_{3b}, r_{1a}, r_{2a}, r_{3a}, r_{1b}, r_{2b}, r_{3b}. Since the differential pair itself is a $\{V_\Delta,I_\Sigma\}$ 2VCCS circuit, its Taylor series is easily derived from the Taylor coefficient of the constituting VCCSs by means of the program of Figure 8-19. For noise analysis NEF has to be specified: NEF=2/3 was used for this purpose (equal to NEF in the simulation model).

Case ident.	Class	Input Variable	Control Variable	Output Variable	$VCCS_a$ mult,sgn	$VCCS_b$ mult,sgn
a	B: $\{V_P,V_\Delta\}$	v_a	$v_\Delta = 0$	$-i_\Sigma$	1,1	1,1
b	B: $\{V_P,V_\Delta\}$	v_a	$v_\Delta = 0$	$-i_\Delta$	2,0	0.9,-1
c-f	B: $\{V_\Sigma, I_\Delta\}$	v_Σ	$i_\Delta = 0$	$\pm i_a$	1,1	1,1
g	A: $\{V_P, I_\Sigma\}$ B: $\{V_P\}$	v_a v_a	$i_\Sigma = 0$ -	v_b $-i_a$	1,1	1/8 ,-1
h	A: $\{V_P, I_\Sigma\}$ B: $\{V_P, V_\Delta\}$	v_a v_a	$i_\Sigma = 0$ $v_\Delta = 0$	$v_{in} - v_b$ i_Σ	1,1	¼,-1
i	B: $\{V_P\}$ C: $\{I_P\}$	v_b i_a	- -	i_b v_a	¼,-1	1,0
j	B: $\{V_P,V_\Delta\}$ D: $\{V_\Delta, I_P\}$	v_a i_a	$v_\Delta = 0$ $v_\Delta = 0$	$-i_b$ $-i_b$	1,0	1,1
k	B: $\{V_P,V_\Delta\}$ D: $\{V_\Delta, I_P\}$	v_a i_a	$v_\Delta=0$ $v_\Delta=0$	i_Σ i_Σ	1,0	1,1
l	A: $\{V_P,I_\Sigma\}$ B: $\{V_P,V_\Delta\}$ C: $\{I_P,I_\Sigma\}$ D: $\{V_\Delta, I_P\}$	v_a v_a i_a i_a	$i_\Sigma = 0$ $v_\Delta = 0$ $i_\Sigma = 0$ $v_\Delta = 0$	$v_{in} - v_b$ i_Σ $v_a - v_b$ i_Σ	1,0	½,-1
m	A: $\{V_P,I_\Delta\}$ B: $\{V_P\}$ C: $\{I_P,I_\Delta\}$ D: $\{I_P\}$	v_a v_a i_a i_a	$i_\Delta = 0$ - $i_\Delta = 0$ -	v_b i_a v_b i_a	1,0	¼,-1
n	A: $\{V_P,I_\Sigma\}$ B: $\{V_P,V_\Sigma\}$ C: $\{I_P,I_\Sigma\}$ D: $\{V_\Sigma, I_P\}$	v_b v_b $-i_a$ $-i_a$	$i_\Sigma = 0$ $v_\Sigma = 0$ $i_\Sigma = 0$ $v_\Sigma = 0$	$v_a + v_b$ $-i_a - i_b$ $v_a + v_b$ $-i_a - i_b$	1/6,-1	1,0

Table 8-6: Classification of the 2VCCS transactor graphs of Figure 4-17, used in 14 AGC amplifiers of Figure 4-20.

Using the definitions of a_c, pwr and sgn from chapter 4, the transconductance of a differential pair can be expressed as:

$$g_{1_dp} \approx kV_{GT} = mult \cdot k_{nom} V_{GT,nom} \left(a_c\right)^{pwr \cdot sgn} \tag{8.11}$$

where mult is a device scaling parameter (proportional to W/L, mult=1 corresponding to $k=k_{nom}$). The values of sgn and mult are listed in the last 2 columns in Table 8-6.

Deriving Performance Expressions

The expressions for the gain can easily be calculated from transmission parameters A, B, C and D using eqn. 2.15. The transmission parameters for a graph are available from the graph analysis program result in Appendix A. Alternatively, these can be selected from the 2VCCS analysis program output, or by hand using Table 5-7 through Table 5-9. An example of this procedure was given in section 5.6. For case n, the resulting voltage gain expression is:

$$A_{v_n} = \frac{g_{1a} - g_{1b}}{g_{1a}\left(1 + g_{1b}R_s\right)} \tag{8.12}$$

Substitution of eqn. 8.11 and $mult_a$=1/6, sgn_a=-1, $mult_b$=1, sgn_b=0 and $g_{1b}R_s$=1 (to satisfy $Z_{in}=1/R_s$) results in:

$$A_{v_n} = \frac{1}{2} - 3\frac{V_{GTnom}}{V_{GTa}} = \frac{1}{2} - \frac{3}{a_c^{-pwr}} \tag{8.13}$$

From this expression, we see that the gain is inversely proportional to V_{GTa}. For a_c=2 and pwr=-1..1 this results in a gain range of -1 to -5.5.

The analysis of the noise uses the method described in chapter 7 to find the equivalent input noise of a 2VCCS transactor. Furthermore the noise of resistors is taken into account, and transferred to the input using eqns. 7.4 and 7.5. The noise factor F is derived by means of the following expression:

$$F = 1 + \frac{\sum_{i=1}^{nns}\left(v_{neq,in,i} + i_{neq,in,i}R_s\right)^2}{4k_B \cdot T \cdot R_s} \tag{8.14}$$

where $v_{neq,in,i}$ and $i_{neq,in,i}$ are the equivalent input noise voltage and current related to the i-th independent noise source, while nns is the number of independent noise sources (note that v_{neq} and i_{neq} are fully correlated).

The supply current I_{SS} for the AGC amplifier relates directly to V_{GT} of the MOS transistors used in the differential pair. Using the SVCCSθ model for the MOSTs, I_{SS} becomes:

$$I_{SS} = 2 \cdot I_{SVCCS\theta}\left(V = V_T + V_{GTa}\right) + 2 \cdot I_{SVCCS\theta}\left(V = V_T + V_{GTb}\right) \tag{8.15}$$

where the factors 2 stem from the fact that every differential pair contains 2 transistors.

The 2VCCS analysis program pictured in Figure 8-20 renders expression for 2VCCS circuits in transmission parameter test conditions (A-, B-, C- or D-determined transactors). If the transactor is used with finite source and/or load impedances, a mix of the expressions renders the transfer properties. This mix is a linear combination for noise and transfer function analysis, since superposition applies for linear circuits. Unfortunately, this is not valid for non-linearity analysis. The question is now how to account for the effect of impedance R_{in} and R_l on non-linearity. Fortunately, a close look at the AGC amplifier designs brings a solution: the circuits can be considered as cascades of two subcircuits that are each 2VCCS circuits themselves (R_s is also considered as a VCCS). As a first guess, one non-linearity can be considered at a time and the contributions can be added. The validity of this guess can be verified afterwards, e.g. by circuit simulations. For case n the decomposition of the AGC amplifier in two 2VCCS circuits can be understood looking at Figure 8-22.

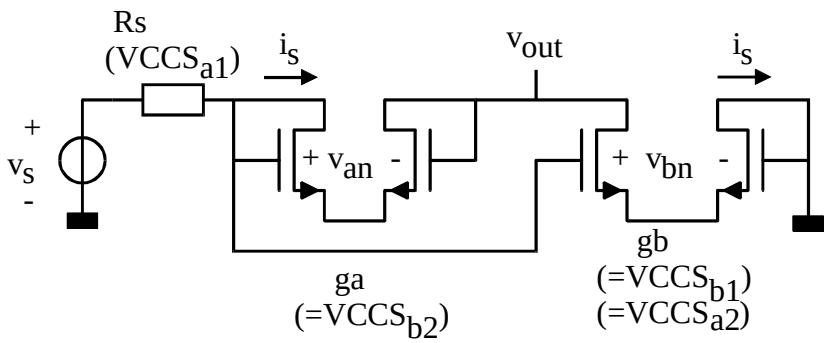


Figure 8-22: AGC amplifier case n, for which design equations are derived.

Id.	Class1	$VCCS_{a1}$	$VCCS_{b1}$	s_{o1}	Class2	$VCCS_{a2}$	$VCCS_{b2}$	s_{o2}
a	$\{\boldsymbol{V_\Sigma}, I_\Delta\}$	1/Rs	1/Ri	v_b	$\{\boldsymbol{V_P}, V_\Delta\}$	$mult_{a_a}=1$ $sgn_{a_a}=1$	$mult_{b_a}=1$ $sgn_{b_a}=1$	$-(i_a+i_b)Rla$ (Rla=2K)
b	$\{\boldsymbol{V_\Sigma}, I_\Delta\}$	1/Rs	1/Ri	v_b	$\{\boldsymbol{V_P}, V_\Delta\}$	$mult_{a_b}=2$ $sgn_{a_b}=0$	$mult_{b_b}=0.9$ $sgn_{b_b}=-1$	$-(i_a-i_b)Rlb$ (Rlb=10K)
c-f	$\{V_\Sigma, I_\Delta\}$	1/Rs	1/Ri	v_b	$\{V_\Sigma, I_\Delta\}$	$mult_{a_c}=1$ $sgn_{a_c}=1$	$mult_{b_c}=1$ $sgn_{b_c}=1$	$-i_a*Rlc$ (Rlc=8K)
g	$\{V_\Sigma, I_\Delta\}$	1/Rs	1/Ri	v_b	$\{V_P, I_\Sigma\}$	$mult_{a_g}=1$ $sgn_{a_g}=1$	$mult_{a_g}= 1/8$ $sgn_{a_g}= -1$	v_b
h	$\{V_\Sigma, I_\Delta\}$	1/Rs	1/Ri	v_b	$\{V_P, I_\Sigma\}$	$mult_{a_h}=1$ $sgn_{a_h}=1$	$mult_{b_h}=1/4$ $sgn_{b_h}=-1$	$v_{in}-v_b$
i	$\{V_\Sigma, I_\Delta\}$	1/Rs	$mult_{b_i}=1$ $sgn_{b_i}=0$	v_b	$\{V_P, I_\Sigma\}$	$mult_{b_i}=1$ $sgn_{b_i}=0$	$mult_{a_i}=1/4$ $sgn_{a_i}=-1$	$-v_b$
j	$\{V_\Sigma, I_\Delta\}$	1/Rs	$mult_{a_j}=1$ $sgn_{a_j}=0$	v_b	$\{V_P, I_\Sigma\}$	$mult_{b_j}=1$ $sgn_{b_j}=1$	1/Rlj (4K)	v_b
k	$\{V_\Sigma, I_\Delta\}$	1/Rs	$mult_{a_k}=1$ $sgn_{a_k}=0$	v_b	$\{V_P, V_\Delta\}$	$mult_{a_k}=1$ $sgn_{a_k}=0$	$mult_{b_k}=1$ $sgn_{b_k}=1$	$(i_a+i_b)*Rlk$ (Rlk=1.3K)
l	$\{V_\Sigma, I_\Delta\}$	1/Rs	$mult_{a_l}=1$ $sgn_{a_l}=0$	v_b	$\{V_P, I_\Delta\}$	$mult_{a_l}=1$ $sgn_{a_l}=0$	$mult_{b_l}=1/2$ $sgn_{b_l}=-1$	$v_{in}+v_b$
m	$\{V_\Sigma, I_\Delta\}$	1/Rs	$mult_{a_m}=1$ $sgn_{a_m}=0$	v_b	$\{V_P, I_\Delta\}$	$mult_{a_m}=1$ $sgn_{a_m}=0$	$mult_{b_m}=1/4$ $sgn_{b_m}=-1$	v_b
n	$\{V_\Sigma, I_\Delta\}$	1/Rs	$mult_{b_n}=1$ $sgn_{b_n}=0$	v_b	$\{V_P, I_\Delta\}$	$mult_{b_n}=1$ $sgn_{b_n}=0$	$mult_{a_n}=1/6$ $sgn_{a_n}=-1$	$v_{in}-v_b$

Table 8-7: Classification data for distortion analysis: the AGC circuits can be considered as a cascade of two 2VCCS circuits, labelled 1 and 2.

The source voltage v_s is forced and renders a current i_s through resistor R_s that flows entirely through differential pair g_b. Although the current also passes g, g_a does not influence its value. Thus the first stage is a $\{V_\Sigma, I_\Delta\}$ circuit consisting of R_s as $VCCS_{a1}$ and g_b as $VCCS_{b1}$ (see Table 8-7, indices 1 refer to the 1st stage). The input variable of stage 1 is $v_\Sigma=v_s$ and the output variable is v_b. The solution for v_b is then used as input for a second 2VCCS circuit, with g_b as $VCCS_{a2}$ and g_a as $VCCS_{b2}$. This circuit can be classified as a $\{V_P, I_\Delta\}$ circuit, with input voltage $v_P=v_b$, $I_\Delta=0$. The final output v_{out} is $v_{a2}-v_{b2}$.

8.5.2 Performance Prediction by Design Equations

The analysis method described in the previous section was used in a MAPLE program for all AGC circuits. Numerical values corresponding to the ones used in simulations were substituted. The resulting values for gain, noise factor, distortion and current are listed in Table 8-8 along with the simulation results of chapter 4. All dimensionless quantities have been expressed in dB for easy interpretation of relative differences.

	$A_{v,sim}$ (dB)	$A_{v,calc}$ (dB)	F_{sim} (dB)	F_{calc} (dB)	$1/HD3_{sim}$ (dB)	$1/HD3_{calc}$ (dB)	$I_{SS,sim}$ (mA)	$I_{SS,calc}$ (mA)
a	1→11	0→12	7→ 4	7 →4	39→74	36→91	0.4 → 11	0.4 → 10
b	1→17	0→18	19→6	24→7	41→74	33→103	6.0→ 2.0	6.0 → 1.2
c-f	1→11	0→12	11→7	13→7	52→74	48→103	0.4→ 11	0.4→ 10
g	2→20	0→25	8→5	10→5	40→39	37→25	0.9→ 5.0	0.8→ 5.0
h	0→16	0→19	6→5	7→5	45→34	43→26	1.6→ 5.5	1.4→ 5.1
i	0→11	0→13	5→2	4→3	67→14	66→25	2.3→ 1.0	2.3→ 1.1
j	1→10	0→12	11→5	9→5	41→80	37→85	1.1→ 6.3	1.2→ 6.0
k	1→5	0→6	4→3	4→3	49→94	45→88	1.1→ 6.3	1.2→ 6.0
l	0→7	0→8	2→1	2→2	80→ 27	72→30	3.7→1.1	3.5 → 1.1
m	1→11	0→13	3→2	5→3	67→17	66→25	2.6→1.1	2.3 →1.1
n	2→14	0→15	5→2	7→3	54→14	49→23	2.0→1.1	1.8 →1.0

Table 8-8: Comparison of the performance prediction of the AGC stage by means of design equations and simulations.

Furthermore Figure 8-23 shows plots of these properties as a function of pwr (see also section 0). The aim of these plots is to show the trends for a coarse visual comparison with the plots of chapter 4. No attempt was made to indicate the individual lines. From the table and figures the following conclusions can be drawn:

- The trends in the simulation results are also found in the results for the macro-model.
- Considering that the expressions are primarily meant to estimate the order of magnitude of performance criteria, the calculated values for gain, noise figure and supply current are in fair agreement (±20%) with the simulation results. For the cases with a large gain-range, the results are somewhat worse but still acceptable. Apparently the rather simple VCCS model grasps the main features of the circuits.
- The distortion estimations are much less accurate. For simulated HD3 values between -30dB and -70dB the estimate is usually within 6dB. Outside this range even higher deviations are found. This is mainly because the simulation model comprises several second order effects not modelled in the SVCCSθ MAPLE model, that dominate at low distortion levels. Furthermore, for high distortion values the intercept point model is no longer valid because of hard-clipping effects. In some cases, e.g. case b, g and h, the distortion is very sensitive to modelling, as (partial) distortion cancellation occurs. Nevertheless, the trends in the simulation and the macro-model results correspond, while even 10dB uncertainty in HD3 is often acceptable in an early design phase.

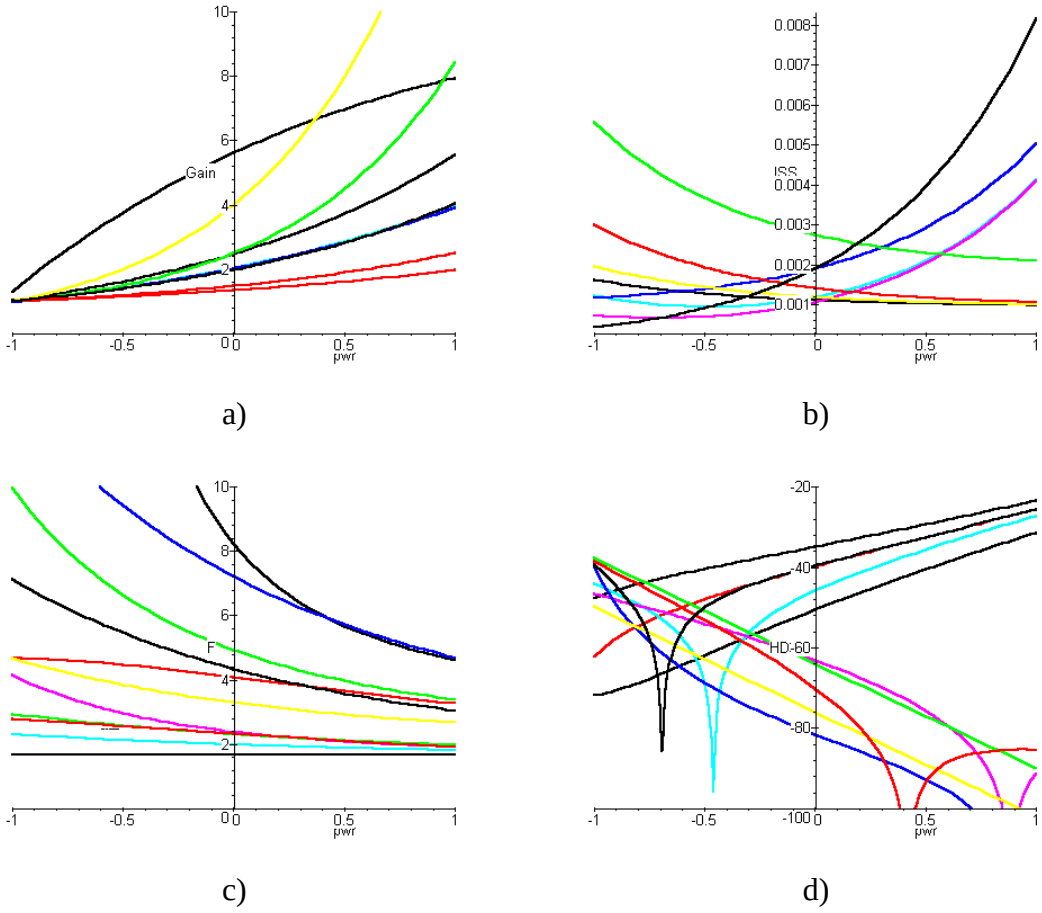


Figure 8-23: Plots calculated with macromodels for the AGC amplifiers as a function of pwr: a) Gain (linear scale); b) I_{SS} (A); c) Noise Factor (linear scale); d) HD3 (dB).

8.5.3 Practical Applications of the Design Equations

The plots of Figure 8-23 allow for a comparison of different design options. Since calculating the plots corresponds to substituting numerical values in analytical design equations, they are calculated in a few seconds, while a circuit simulator would need orders of magnitude more computer power. Hence, a quick and easy exploration of many different design alternatives is possible. Moreover, the design equations are hierarchical: the properties of a transactor are a function of VCCS properties, while these are again a function of MOS transistor properties. Hence, deriving plots for another VCCS implementation merely means substituting another set of VCCS equations. Moreover, the hierarchy makes it possible to distinguishes between properties related to the interconnection of VCCSs and properties of the VCCS themselves.

A set of design equations is also very useful if the performance of a circuit is to be optimised by means of a set of design parameters. Because of the systematic nature of the approach in this thesis, it should be possible to incorporate it in analog CAD tools.

As discussed in chapter 3, a very important advantage of analytical design equations lies in the insight that they can provide to designers, which can render clues for design improvements. An example was given at the end of chapter 7, relating to AGC amplifier

case l: eqn. 7.11 reveals that the noise contribution of $VCCS_a$ cancels for $g_bR_s=1$. The design satisfied this condition, and this leads to the best noise performance (Table 8-8).

As a last example, consider the HD3 plots of the AGC stages shown Figure 8-23d. Broadly speaking (neglecting distortion minima due to specific distortion cancellations), the distortion either decreases (case a, b, c, j and k) or increases with gain (the other cases). A look at the distortion expressions shows that this relates to different dependencies on the input and output voltage amplitude. These differences stem from different connections of the VCCS voltage terminals to the input and output signal of the transactor: transactors with decreasing distortion have VCCSs connected to the input voltage, while for the others at least one terminals is connected to the output. In the AGC application considered, the output voltage swing is constant, while the input voltage swing reduces with gain. Connection to the input, in combination with an increase of V_{GT} with gain, results in a decrease of distortion with gain. Connection to the output (constant amplitude), in combination with a transconductance that is lowered to increase the gain, results in an increased distortion since V_{IP3} of a differential pair reduces rather strongly with decreasing transconductance. Because of the latter reason, a useful design clue might be to use a VCCS with a V_{IP3} that *does not* depend on transconductance (e.g. an LVCCSθ) or does depend less strongly on transconductance (e.g. SVCCSθ). A detailed consideration of these design alternatives is beyond the scope of this thesis.

Thus it has been shown that the classification and analysis techniques developed in the second part of this thesis are helpful during the design of VCCS circuits. Macro-models of VCCS circuits have been derived, that predict several important performance aspects.

8.6 Summary and Conclusions

In this chapter, applications of the theory developed in the second part of this thesis have been exemplified. The most important results are summarised below.

Classification of CMOS Transconductor Circuits

- Almost all published transconductor circuits (ca. 50 publications) can be classified using the classification system proposed in chapter 5. Exceptions are non-separable 4-transistor kernels proposed by Bult [54] and Czarnul [72] and the heavily interwoven circuits using a combination of a triode and saturated MOSTs [51,66].
- The following different classes of circuits were encountered for V-I conversion:
    1. $\{V_P\}$ $(V_P \rightarrow I_P)$
    2. $\{V_P, V_\Sigma\}$ $(V_P \rightarrow I_\Delta)$
    3. $\{V_P, V_\Delta\}$ $(V_P \rightarrow I_\Delta)$
    4. $\{V_\Sigma, I_\Delta\}$ $(V_\Sigma \rightarrow I_P)$
    5. $\{V_\Delta, I_\Sigma\}$ $(V_\Delta \rightarrow I_\Delta)$

Comparison of V-I Kernels with 2 Matched MOSTs

All Transconductor V-I Kernels with 2 matched MOST-VCCSs have been analysed. Four cases with essentially different distortion appear to exist: forcing constant V_Σ,V_Δ, I_Σ or I_Δ. For these cases the achievable dynamic range has been compared for different MOST I(V) characteristics, using NDR/I_{SS} as a figure of merit. The main conclusions are:

- The exponential model renders worst NDR/I_{SS}.
- The approximate square-law model renders the best values, especially for high θ (S1 and S4 curves).
- Constant V_Σ circuits render the same NDR/I_{SS} as a single MOST, yet with additional HD2 cancellation.
- Stacked VCCSs (I_Δ=0) render even 2 times better NDR/I_{SS} values, yet require more voltage headroom.
- Constant Vdif circuits have an increased G_m-range, paid by a drastic reduction of NDR/I_{SS} for low G_m.

AGC Amplifier Design Case Study

Using the systematic analysis methods developed in chapter 5-7, symbolic design equations have been derived for the AGC amplifers synthesised in chapter 4. It was shown that these equations are useful during design because of the following reasons:

- Many different design alternatives can be evaluated quickly by simple substitutions of VCCS specific data. Moreover, because of the hierarchical nature of the VCCS circuit design equations, VCCS specific transactor properties and VCCS independent properties can easily be distinguished.
- Analytical expressions help to gain insight in the operation of a circuit and the requirements for its components.

The estimates based on the macro-model of the AGC amplifiers were compared with simulation results with the following results:

- Small signal gain and noise estimates are within 1-2 dB of the simulation results.
- Distortion estimates are much less accurate and strongly depend on modelling. For HD3 values between -30dB and -70dB the difference compared to simulations was found to be less than roughly 6dB.

9

Symmary & Conclusions

This chapter surveys the contents of this thesis. In section 9.1 a summary of the contents is given, while section 9.2 presents the main conclusions. Original contributions are identified in section 9.3. Finally, in section 9.4 recommendations for further research are given.

9.1 Summary

This thesis deals with “Transconductance based CMOS Circuits”, i.e. circuits with a *transfer function* mainly determined by the *transconductance* of MOS transistors (e.g. transconductance or amplifier stages). Such circuits can have an electronically variable transfer function, as is required in self-correcting or programmable systems (the transconductance can be varied by changing the biasing point). Moreover, transconductance based circuits are simple circuits with often good high-frequency performance. This thesis aims at a *generalisation* and *systematisation* of the *design* of transconductance based circuits. The underlying idea is that many different transistor circuits are different implementations of a very limited number of different principles. Although the thesis focuses on MOST circuits, many results are applicable to other realisations (e.g. bipolar transistors).

For the purpose of *generalisation*, a MOST or a pair of MOSTs is represented as a *Voltage Controlled Current Source* (VCCS). Using a VCCS as a building block, the possibilities to implement linear two-ports are *systematically* explored using linear graphs. Two VCCSs are at least required to implement V-V and I-I transfer functions apart from V-I and I-V transfer functions. *All graphs of two-ports with two VCCSs* are then *generated* and analysed systematically, resulting in 145 graphs of VCCS-circuits with non-zero transfer function. Given a desired two-port behaviour, all suitable graphs can be selected. From each graph, several different transistor implementation can be derived systematically, so that several hundreds of circuits are covered. As an example, an AGC amplifier stage has been designed using the systematic design procedure. It is shown that several alternative designs are possible, which show significant differences in behaviour.

Although many different circuit implementations are possible, only a limited number of different two-port parameter expressions is found. This suggests that there are only a limited number of different ways to establish two-port parameters. It is shown that in circuits with two VCCSs, driven by ideal sources, two independent relations amongst the

VCCS voltages and currents are crucial in this respect. On the assumption that only Kirchhoff relations are allowed (two-ports consisting of only two VCCSs and interconnections), all different possibilities are considered. This leads to the definition of a class of *"2VCCS circuits"* that can be subdivided in 3 main classes and 14 subclasses, based on different sets of two imposable Kirchhoff relations. The classification is useful for circuit synthesis and analysis as it reveals *all basically different ways to exploit two VCCSs*. Moreover, it allows for a *unified analysis* of classes of circuits.

A unified analysis of classes of circuits has been performed for several properties that can be modelled using a VCCS model. This results in hierarchical macro-models for 2VCCS circuits, expressing circuit properties in VCCS properties by means of symbolic equations. The properties that are analysed are the small-signal transfer function, the DC-transfer curve, the (weak) non-linear behaviour, and the noise.

To show their usefulness, the classification and analysis techniques have been applied to CMOS transconductor circuits described in literature. Transconductors from some 50 papers are classified in 5 classes, and analysed. The results provide insight in relations between different circuits, and render an estimate for their maximal achievable dynamic range in relation to supply current. Finally, the classification and analysis techniques are applied to the AGC-amplifier design discussed earlier. It appears that the symbolic macro-models provide a useful first order estimate of the results found using SPICE simulations.

9.2 Conclusions

- For circuit synthesis and first-cut design, a MOST or an elementary combination of MOSTs can often be considered as a Voltage Controlled Current Source (VCCS). The transfer function of circuits designed on this basis is determined by the transconductances of VCCSs (*Transconductance based CMOS Circuits)* (chapter 1, 3).
- Broadly speaking, 3 different types of large-signal I(V) characteristics for MOST-VCCSs are encountered: a Linear (LVCCS), Square-law (SVCCS) and Exponential (EVCCS) function. Since the transconductance of a VCCS depends in general on biasing, the transfer properties of VCCS circuits can be made electronically variable. This is a major reason for their use. Furthermore, VCCS circuits are simple circuits that often have attractive high frequency properties (chapter 1, 3).
- From a viewpoint of optimum information transfer and compatibility with voltage- and current-mode signal processing, 9 types of linear, so called transactors, are desired: two-ports with port impedances that are either very low, very high or well-defined. The transmission two-port parameters of such transactors should either be linear and accurate (useful as is), or electronically tuneable (allowing for self-correction of IC-processing and temperature variations). Alternatively, electronic variability can be used to achieve programmability of transactor transfer properties (chapter 2).
- *All linear transactors consisting of two VCCSs connected to a source and load*, have been generated *using linear graphs*, resulting in 145 different graphs. The transmission parameters of the transactors have been analysed by means of a MAPLE program

(Appendix A). It appears that all desired 9 types of transactors can either be implemented directly or at least approximated by circuits with two VCCSs (chapter 3).

- Given a set of desired transmission parameters, all graphs of transactors with 2 VCCSs implementing this set can be found in Appendix A. These transactors can be realised in numerous different ways, since in principle any transconductor realisation can be used to implement a VCCS in graph. However, depending on the relative orientation of the v- and i- branches in the graph, and depending on their connectivity, the simplest possibility is either a resistor, a MOST or a pair of MOS transistors (chapter 4).
- Although numerous circuit realisations are possible, the number of different realisable transmission parameters is limited by the availability of only two transconductance parameters in so called 2VCCS circuits. These parameters can be found by generating all different sets of two independent Kirchhoff relations amongst the VCCS variables and input variables and an analysis of all possible resulting output variables (chapter 5).
- Based on the different *sets of 2 independent imposable Kirchhoff relations, 2VCCS circuits* driven by two independent voltage and/or current sources can be *classified in 3 main classes and 14 subclasses* (chapter 5).
- All circuits belonging to a class or subclass, can often be analysed in one run. In this way, general expressions for the transfer function, distortion, noise and dynamic range of 2VCCS circuits in a given bias point have been derived. The VCCS design-parameters in these expressions are the transconductance of the two VCCSs (g_a and g_b), the 2nd and 3rd order Taylor coefficients of the I(V) characteristic (g_{2a},g_{2b},g_{3a},g_{3b}), and the Noise Excess Factor (NEF_a and NEF_b) (chapter 5, 6, 7, 8).
- The DC transfer characteristic and bias point of a 2VCCS circuit depends on the I(V) characteristic of the VCCSs and the applied bias voltages and/or currents. Assuming equal VCCSs satisfying the generalised VCCS equations (LVCCS, SVCCS, EVCCS), DC transfer characteristic expressions have been derived for all classes. Furthermore, limits for the useful operating range have been identified, indicating trade-offs between input swing and tuneability of the transfer properties (chapter 6).
- Some 50 published linear V-I converters have been classified in 5 different classes, with essentially different operating principle (chapter 8).
- The dynamic range and supply current of all classes of 2VCCS V-I converter kernels realised with two matched MOSTs has been analysed. The results render an estimation of the maximum achievable dynamic range of the V-I kernels (chapter 8).

9.3 Original Contributions

The following original contributions can be found in this thesis and related publications:

- *All graphs* of linear two-ports with *two VCCSs* connected between a source and load have been generated. This results in 145 graphs of linear transactors with 1 or more non-zero transmission parameters, shown in appendix A (chapter 3)

- A *systematic* procedure for the *generation* of different *transistor circuit* realisations of VCCS graphs has been developed, resulting in several hundreds of circuit topologies for 145 graphs (chapter 4).
- A *classification* system for circuits with two VCCSs based on *sets of two independent Kirchhoff relations* has been proposed (chapter 5).
- *Symbolic expressions* for the DC transfer characteristic, transmission parameters, non-linearity and noise of *all classes* of 1VCCS and 2VCCS circuits in terms of VCCS properties have been derived. *Hierarchical macro-models* for these circuits are thus available (chapter 5-8).
- Many published transactor circuits (±50), especially transconductor circuits, have been classified in a few different classes (±5) and compared with respect to maximum achievable dynamic range.
- Several new circuits and/or circuit applications have been found or explored:
    - A transconductor with a constant bandwidth and its application to a programmable filter [58,90].
    - Current gain-cells with an electronically variable gain, that is insensitive to temperature and IC-processing and have a constant bandwidth [57,61].
    - Complementary gain-cell circuits with attractive cascading properties [76,110].
    - An AM-suppression circuit with a very low AM-PM conversion, based on variable gain [120,122].

9.4 Recommendations for Further Research

- Application of the theory developed in this thesis to more design problems. It is expected that this will lead to new and improved circuit designs.
- The development and implementation of an automated design strategy for the selection, sizing and optimisation of VCCS circuits. The design procedure of chapter 4 can be used as a start.
- Extension of the VCCS circuit generation to more VCCSs. Some well-known basic circuits are not yet covered by the classification, although they can be considered as a combination of VCCSs (e.g. Wilson current mirror). Moreover, transistor circuits with resistive feedback can be considered as VCCS circuits, and generated systematically.
- Research to the high-frequency properties of VCCS circuits. Apart from bandwidth limitations, the frequency dependence of distortion in VCCS circuits might be an important problem (e.g. reactive distortion [54]).

Appendix A

Transmission Parameters of All Transactors with 2 VCCSs

Format: Graph-name (see Figure 3-15), [Definitions of va, vb, vsref], A, B, C, D.

*****

(s)(i+i+l) [va = v2, vb = v2-v1, sref = v2] [A=0, B=(1/gb), C=0, D=0]

(s)(i+i+l) [va = v3-v1, vb = v2-v1, sref = v2] [A=0, B=(1/gb), C=0, D=0]

(s)(i+i+l) [va = -v2+v3, vb = v2-v1, sref = v2] [A=0, B=(1/gb), C=0, D=0]

(s)(i//l)(i) [va = v3, vb = v3-v1, sref = 0] [A=0, B=(-1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = v3, sref = 0] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v1, vb = v3, sref = 0] [A=0, B=(-1/ga), C=0, D=0]

(s)(i//l)(i) [va = v1, vb = -v2+v3, sref = 0] [A=0, B=(-1/ga), C=0, D=0]

(s)(i//l)(i) [va = v1, vb = v3-v1, sref = 0] [A=0, B=(-1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3, vb = v1, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = -v2+v3, vb = v2-v1, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v2-v1, vb = -v2+v3, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = v3, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = -v2+v3, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = v2-v1, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = v1, sref = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v1, vb = v3, sref = v3] [A=0, B=(-1/ga), C=0, D=0]

THE 3 CASES WITH NON-ZERO PARAMETERS D:

(s+i+l)(i) [va = v3-v1, vb = v1] [A=0, B=0, C=0, D=1]

(s+i+l)(i) [va = -v2+v3, vb = v1] [A=0, B=0, C=0, D=1]

(s+i+l)(i) [va = v3, vb = v1] [A=0, B=0, C=0, D=1]

THE 23 CASES WITH NON-ZERO PARAMETERS AB:

(s)(i//i//l) [va = v1, vb = v2, sref = 0] [A=(-gb/ga), B=(-1/ga), C=0, D=0]

(s)(i//i//l) [va = v1, vb = v2-v1, sref = 0] [A=(gb/(-ga+gb)), B=(1/(-ga+gb)), C=0, D=0]

(s)(i//i//l) [va = v2, vb = v2-v1, sref = 0] [A=((ga+gb)/gb), B=(1/gb), C=0, D=0]

(s)(i//i//l) [va = v2-v1, vb = v2-v1, sref = 0] [A=1, B=(1/(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = -v2+v3, vb = v2-v1, sref = 0] [A=1, B=(1/gb/ga*(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = v2-v1, vb = -v2+v3, sref = 0] [A=1, B=(1/gb/ga*(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = v1, vb = -v2+v3, sref = v2] [A=-1, B=(-1/gb/ga*(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = v3-v1, vb = v2, sref = v2] [A=1, B=(1/gb/ga*(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = v2, vb = v3-v1, sref = 0] [A=1, B=(1/gb), C=0, D=0]

(s)(i+i+l) [va = v3-v1, vb = v2, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i+i+l) [va = v3-v1, vb = -v2+v3, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i+i+l) [va = v3-v1, vb = v2-v1, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i+i+l) [va = -v2+v3, vb = v3-v1, sref = 0] [A=1, B=(1/gb), C=0, D=0]

(s)(i+i+l) [va = v2-v1, vb = v3-v1, sref = 0] [A=1, B=(1/gb), C=0, D=0]

(s)(i//l)(i) [va = -v2+v3, vb = v3-v1, sref = 0] [A=1, B=(-1/ga), C=0, D=0]

(s)(i//l)(i) [va = v2-v1, vb = v3, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v2-v1, vb = -v2+v3, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v2-v1, vb = v3-v1, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = -v2+v3, sref = 0] [A=1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v3, vb = v2-v1, sref = v3] [A=1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = -v2+v3, vb = v1, sref = v3] [A=-1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v2-v1, vb = v3, sref = v3] [A=1, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v1, vb = -v2+v3, sref = v3] [A=-1, B=(-1/ga), C=0, D=0]

THE 6 CASES WITH NON-ZERO PARAMETERS AD:

s//(i+i)//l [va = v2, vb = v2] [A=1, B=0, C=0, D=1]

(s//i//l)(i) [va = v2, vb = v2] [A=1, B=0, C=0, D=1]

(s//i//l)(i) [va = v2-v1, vb = v2-v1] [A=1, B=0, C=0, D=1]

(s+i+l)(i) [va = v3-v1, vb = v2-v1] [A=1, B=0, C=0, D=1]

(s+i+l)(i) [va = -v2+v3, vb = v2-v1] [A=1, B=0, C=0, D=1]

(s+i+l)(i) [va = v3, vb = v2-v1] [A=1, B=0, C=0, D=1]

THE 1 CASES WITH NON-ZERO PARAMETERS BC:

(s//i)(i//l) [va = v2, vb = v1, sref = 0] [A=0, B=(-1/gb), C=ga, D=0]

THE 23 CASES WITH NON-ZERO PARAMETERS BD:

s+i+l+i [va = v2, vb = v2-v1] [A=0, B=(-1/gb/ga*(ga+gb)), C=0, D=1]

s+i+l+i [va = v2-v1, vb = v2] [A=0, B=(1/gb/ga*(ga+gb)), C=0, D=1]

s+i+i+l [va = v2-v1, vb = v2] [A=0, B=((-ga+gb)/gb/ga), C=0, D=1]

s+i+i+l [va = v2, vb = v2-v1] [A=0, B=(-(-ga+gb)/gb/ga), C=0, D=1]

s+(i//i)+l [va = v1, vb = v1] [A=0, B=(1/(ga+gb)), C=0, D=1]

s+i+(i//l) [va = v1, vb = v1] [A=0, B=(-1/(ga+gb)), C=0, D=(1/(ga+gb)*ga)]

s//i//(i+l) [va = v1, vb = v1] [A=0, B=(-1/gb), C=0, D=((-ga+gb)/gb)]

(s//i)(i//l) [va = v1, vb = v1, sref = 0] [A=0, B=(-1/gb), C=0, D=(-ga/gb)]

s+i+l+i [va = v1, vb = v2] [A=0, B=(-1/ga), C=0, D=1]

s+i+l+i [va = v1, vb = v3] [A=0, B=(-1/ga), C=0, D=1]

s+i+l+i [va = v1, vb = v2-v1] [A=0, B=(-1/ga), C=0, D=1]

s+i+l+i [va = v1, vb = v3-v1] [A=0, B=(-1/ga), C=0, D=1]

s+i+i+l [va = -v2+v3, vb = v1] [A=0, B=(-1/gb), C=0, D=1]

s+i+i+l [va = v2-v1, vb = v1] [A=0, B=(-1/gb), C=0, D=1]

s+i+i+l [va = v2, vb = v1] [A=0, B=(-1/gb), C=0, D=1]

s+i+i+l [va = v1, vb = -v2+v3] [A=0, B=(-1/ga), C=0, D=1]

s+i+i+l [va = v1, vb = v2-v1] [A=0, B=(-1/ga), C=0, D=1]

s+i+i+l [va = v1, vb = v2] [A=0, B=(-1/ga), C=0, D=1]

(s+i+l)(i) [va = v3-v1, vb = v3] [A=0, B=(1/ga), C=0, D=1]

(s+i+l)(i) [va = v3, vb = v3-v1] [A=0, B=(-1/ga), C=0, D=1]

(s+i+l)(i) [va = v1, vb = v3-v1] [A=0, B=(-1/ga), C=0, D=1]

(s+i+l)(i) [va = v1, vb = -v2+v3] [A=0, B=(-1/ga), C=0, D=1]

(s+i+l)(i) [va = v1, vb = v3] [A=0, B=(-1/ga), C=0, D=1]

THE 3 CASES WITH NON-ZERO PARAMETERS ABC:

s+i+(i//l) [va = v2, vb = v2-v1] [A=((ga+gb)/gb), B=(1/gb), C=(-ga), D=0]

s+i+(i//l) [va = v2, vb = v1] [A=(-ga/gb), B=(-1/gb), C=(-ga), D=0]

(s//i)(i//l) [va = v2, vb = v2-v1, sref = 0] [A=1, B=(1/gb), C=ga, D=0]

THE 24 CASES WITH NON-ZERO PARAMETERS ABD:

s+i+l+i [va = v2, vb = v3-v1] [A=-1, B=(-1/gb/ga*(ga+gb)), C=0, D=1]

s+i+l+i [va = v3, vb = v2-v1] [A=1, B=(-1/gb/ga*(ga+gb)), C=0, D=1]

s+i+l+i [va = v2-v1, vb = v3] [A=1, B=(1/gb/ga*(ga+gb)), C=0, D=1]

s+i+l+i [va = v3-v1, vb = v2] [A=-1, B=(1/gb/ga*(ga+gb)), C=0, D=1]

s+i+i+l [va = -v2+v3, vb = v2-v1] [A=1, B=(1/gb/ga*(ga+gb)), C=0, D=1]

s+i+i+l [va = v2-v1, vb = -v2+v3] [A=1, B=(1/gb/ga*(ga+gb)), C=0, D=1]

s+(i//i)+l [va = v2, vb = v2-v1] [A=((ga+gb)/gb), B=(-1/gb), C=0, D=1]

s+(i//i)+l [va = v2, vb = v1] [A=(-ga/gb), B=(1/gb), C=0, D=1]

s+(i//i)+l [va = v2-v1, vb = v2-v1] [A=1, B=(-1/(ga+gb)), C=0, D=1]

s+(i//i)+l [va = v2-v1, vb = v1] [A=(-1/(-ga+gb)*ga), B=(1/(-ga+gb)), C=0, D=1]

s+i+(i//l) [va = v2-v1, vb = v2-v1] [A=1, B=(1/(ga+gb)), C=0, D=(1/(ga+gb)*ga)]

s//i//(i+l) [va = v2-v1, vb = v2-v1] [A=1, B=(1/gb), C=0, D=((-ga+gb)/gb)]

(s//i)(i//l) [va = v2-v1, vb = v2-v1, sref = 0] [A=1, B=(1/gb), C=0, D=(-ga/gb)]

s+i+i+l [va = -v2+v3, vb = v3-v1] [A=1, B=(1/gb), C=0, D=1]

s+i+i+l [va = v3-v1, vb = -v2+v3] [A=1, B=(1/ga), C=0, D=1]

s+i+i+l [va = v3-v1, vb = v2-v1] [A=1, B=(1/ga), C=0, D=1]

s+i+i+l [va = v3-v1, vb = v2] [A=1, B=(1/ga), C=0, D=1]

s+i+i+l [va = v2-v1, vb = v3-v1] [A=1, B=(1/gb), C=0, D=1]

s+i+i+l [va = v2, vb = v3-v1] [A=1, B=(1/gb), C=0, D=1]

(s+i+l)(i) [va = v3-v1, vb = -v2+v3] [A=1, B=(1/ga), C=0, D=1]

(s+i+l)(i) [va = -v2+v3, vb = v3-v1] [A=1, B=(-1/ga), C=0, D=1]

(s+i+l)(i) [va = v2-v1, vb = v3-v1] [A=1, B=(1/ga), C=0, D=1]

(s+i+l)(i) [va = v2-v1, vb = -v2+v3] [A=1, B=(1/ga), C=0, D=1]

(s+i+l)(i) [va = v2-v1, vb = v3] [A=1, B=(1/ga), C=0, D=1]

THE 9 CASES WITH NON-ZERO PARAMETERS ACD:

s//(i+i)//l [va = v2, vb = v2-v1] [A=1, B=0, C=(-gb*ga/(ga+gb)), D=1]

s//(i+i)//l [va = v2-v1, vb = v2] [A=1, B=0, C=(gb*ga/(ga+gb)), D=1]

s//i//i//l [va = v1, vb = v1] [A=1, B=0, C=(ga+gb), D=1]

s//(i+i)//l [va = v1, vb = v2] [A=1, B=0, C=(-ga), D=1]

s//(i+i)//l [va = v1, vb = v2-v1] [A=1, B=0, C=(-ga), D=1]

(s//i//l)(i) [va = v1, vb = v2] [A=1, B=0, C=ga, D=1]

(s//i//l)(i) [va = v1, vb = v2-v1] [A=1, B=0, C=ga, D=1]

(s//i//l)(i) [va = v2, vb = v2-v1] [A=1, B=0, C=ga, D=1]

(s//i//l)(i) [va = v2-v1, vb = v2] [A=1, B=0, C=(-ga), D=1]

THE 3 CASES WITH NON-ZERO PARAMETERS BCD:

s//i//(i+l) [va = v2, vb = v1] [A=0, B=(-1/gb), C=ga, D=1]

s//i//(i+l) [va = v2-v1, vb = v1] [A=0, B=(-1/gb), C=ga, D=((ga+gb)/gb)]

(s//i)(i//l) [va = v2-v1, vb = v1, sref = 0] [A=0, B=(-1/gb), C=ga, D=(ga/gb)]

THE 7 CASES WITH NON-ZERO PARAMETERS ABCD:

s+i+(i//l) [va = v2-v1, vb = -v1]

[A=ga/(ga+gb), B=1/(ga+gb), C=-ga*gb/(ga+gb), D=ga/(ga+gb)]

s+i+(i//l) [va = v2-v1, vb = v2]

[A=((ga+gb)/ga), B=(1/ga), C=gb, D=1]

s+i+(i//l) [va = -v1, vb = v2-v1]

[A=gb/(ga+gb), B=1/(ga+gb), C=ga*gb/(ga+gb), D=ga/(ga+gb)]

s+i+(i//l) [va = v1, vb = v2] [A=(-gb/ga), B=(-1/ga), C=gb, D=1]

s//i//(i+l) [va = v1, vb = v2-v1] [A=1, B=(1/gb), C=ga, D=((ga+gb)/gb)]

s//i//(i+l) [va = v2, vb = v2-v1] [A=1, B=(1/gb), C=ga, D=1]

(s//i)(i//l) [va = v1, vb = v2-v1, sref = 0] [A=1, B=(1/gb), C=ga, D=(ga/gb)]

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FLOATING INPUT GRAPHS

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THE 9 CASES WITH NON-ZERO PARAMETERS B:

(s)(i//i//l) [va = v3-v1, vb = v3-v1] [A=0, B=(1/(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = v4-v2, vb = v2-v1] [A=0, B=(1/gb/ga*(ga+gb)), C=0, D=0]

(s)(i+i+l) [va = v3-v2, vb = v4-v1] [A=0, B=(1/gb), C=0, D=0]

(s)(i+i+l) [va = v4-v2, vb = v4-v1] [A=0, B=(1/gb), C=0, D=0]

(s)(i+i+l) [va = v2, vb = v4-v1] [A=0, B=(1/gb), C=0, D=0]

(s)(i//l)(i) [va = v3-v1, vb = v4-v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v4-v1, vb = v3] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v4-v1, vb = v3-v1] [A=0, B=(1/ga), C=0, D=0]

(s)(i//l)(i) [va = v4-v1, vb = v3-v2] [A=0, B=(1/ga), C=0, D=0]

THE 1 CASES WITH NON-ZERO PARAMETERS AB:

(s)(i//i//l) [va = v2, vb = v3-v1] [A=(ga/gb), B=(1/gb), C=0, D=0]

THE 1 CASES WITH NON-ZERO PARAMETERS BC:

(s//i)(i//l) [va = v2, vb = v3-v1] [A=0, B=(1/gb), C=ga, D=0]

THE 1 CASES WITH NON-ZERO PARAMETERS BD:

(s//i)(i//l) [va = v3-v1, vb = v3-v1] [A=0, B=(1/gb), C=0, D=(-ga/gb)]

References

Analog CMOS circuits: overview papers

[1] P. R. Gray, B. A. Wooley, R. W. Broderson, "Analog MOS integrated circuits", New York, IEEE Press, 1980.

[2] D. J. Allstot, W. C. Back, JR., "Technological design considerations for monolithic MOS switched-capacitor filtering systems", Proc. IEEE, vol. 71, pp. 167-186, august 1983.

[3] E. A. Vittoz, "The design of high-performance analog circuits on digital CMOS chips", IEEE J. Solid-State Circuits, vol. SC-20, pp.657-665, June 1985.

[4] E. Habekotte, B. Hoefflinger, H. Klein, M. A. Beunder, "State of the art in the analog CMOS circuit design", Proc. IEEE, vol.75, pp. 816-828, June 1987.

[5] Y. P. Tsividis, "Analog MOS integrated circuits - certain new ideas, trends, and obstacles", IEEE J. Solid-State Circuits, Vol. SC-22, pp. 317-321, June 1987.

[6] P. R. Gray, B. A. Wooley, R. W.Broderson, "Analog MOS integrated circuits, II", New York, IEEE Press, 1989.

[7] C. Toumanzou, F. J. Lidgey and D. G. Haigh, "Analogue IC design: the current-mode approach", London, Peter Peregrinus Ltd., 1990.

[8] Y. P. Tsividis, "R&D in analog circuits: possibilities and needed support", Proceedings of the ESSCIRC '93, pp.1-14, Copenhagen Danmark, 21-23 September 1992.

[9] Y.P. Tsividis, J.O. Voorman, "Integrated Continuous-Time Filters", New York, IEEE Press, 1993.

[10] E. A. Vittoz, "Low-Power Design: Ways to Approach the Limits", ISSCC'94 Digest of technical papers, pp.14-18, 1994.

[11] E. A. Vittoz, "Analog VLSI Signal Processing: Why, Where, and How?", Analog Integrated Circuits and Signal Processing, vol. 6, pp. 27-44, 1994.

[12] M. W. Hauser, R. G. Meyer, W. D. Mack, "Variable-Gain Techniques: Translinear or Not?", Proceedings of the Workshop on Advances in Analog Circuit Design, Lausanne, Switzerland, April 2-4, 1996.

[13] M. W. Hauser, E. A. M. Klumperink, R. G. Meyer, W. D. Mack, "Variable-Gain, Variable-Transconductance, and Multiplication Techniques: A Survey", In W. Sansen et al, editors, Analog Circuit Design, Dordrecht: Kluwer Academic Publishers, 1997.

Linear Transactor Design Theory

[14] B. D. H. Tellegen, "On nullators and norators", IEEE Transactions on Circuit Theory, Vol. CT-13, pp. 466-469, 1966.

[15] E. M. Cherry and D.E. Hooper, "Amplifying Devices and Low-pass Amplifier Design", Wiley, New York, 1968.

[16] K. C. Smith, A. Sedra, "The Current Conveyor - A New Circuit Building Block", Proceedings of the IEEE (Letters), Vol. 56, pp. 1368-1369, August 1968.

[17] A. Sedra, K. C. Smith, "A Second-Generation Current Conveyor and Its Applications", IEEE Transactions on Circuit Theory, Vol. CT-17, pp. 132-134, February 1970.

[18] M. Bialko and R. W. Newcomb, "Generation of all finite linear circuits using the integrated DVCCS", IEEE Transactions on Circuit Theory, pp.733-736, November 1971.

[19] J. H. Huijsing, "Integrated circuits for accurate linear analogue electric signal processing", Ph.D. Thesis, Delft University Press, 1981.

[20] P. R. Gray, R. G. Meyer, "MOS operational amplifier design - a tutorial overview", IEEE J. of Solid-State Circuits, vol. SC-17, pp. 969-982, December 1982.

[21] E. H. Nordholt, "Design of high-performance negative-feedback amplifiers", Amsterdam, Elsevier Scientific Publishing Company, 1983.

[22] P. R. Gray and R. G. Meyer, "Analysis and design of analog integrated circuits", second edition, New York, John Wiley & Sons, 1984.

[23] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: a tutorial", IEEE Circuits and Device Mag., 2, pp. 20-32, 1985.

[24] J. Davidse, "Analogue electronic circuit design", Prentice Hall International, New York, 1991.

[25] D. G. Haigh, C. A. Losada, A. E. Parker and D. R. Webster, "Systematic Approach for the Development and Design of Analogue Communication Circuits", ECCTD '93, Selected Topics in Circuits and Systems, Amsterdam, Elsevier Scientific Publishing Company, 1993.

[26] J. H. Huijsing, "Design and Application of the Operational Floating Amplifier (OFA): The MOST Universal Operational Amplifier", Analog Integrated Circuits and Signal Processing, Vol. 4, pp. 115-129, 1993.

[27] W. A. Serdijn, "The Design of Low-Voltage Low-Power Analog Integrated Circuits and their Applications in Hearing Instruments", Ph.D. Thesis, ISBN 90-6275-955-6, Delft University Press, Delft, 1994.

MOS Modeling

[28] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation", IEEE J. Solid-State Circuits, Vol. SC-12, pp.224-231, 1977.

[29] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2, Memorandum No. UCB/ERL M80/7, Electronics Research Laboratory, University of Berkeley, 1980.

[30] R. S. Muller, T. I. Kamins, "Device Electronics for Integrated Circuits", Wiley, New York, 1986.

[31] S. L. Garverick, C. G. Sodini, "A simple model for scaled MOS transistors that includes field-dependent mobility", IEEE J. Solid-state Circuits, SC-22, pp.111-114, February 1987.

[32] Y. P. Tsividis, "Operation and modeling of the MOS transistor", New York, McGraw-Hill Book Company, 1987.

[33] H. Wallinga, K. Bult, "Design and analysis of CMOS analog signal processing circuits by means of a graphical MOST model", IEEE J. Solid-State Circuits, Vol. SC-24, no.3, pp. 672-680, June 1989.

[34] G. Groenewold, W.J. Lubbers, "Systematic Distortion Analysis for MOSFET Integrators with Use of a New MOSFET Model", IEEE Transactions on Circuits and Systems-II, vol. 41, no. 9, pp. 569-580, September 1994.

Linear Transactor Circuits

[35] B. Gilbert, "A new wide-band amplifier technique", IEEE J. Solid-State Circuits, Vol. SC-3, pp. 353-373, December 1968.

[36] B. J. Hosticka, "Improvement of the Gain of MOS Amplifiers", IEEE J. Solid-State Circuits, vol. SC-14, pp. 1111-1114, 1979.

[37] P.B. Denyer et al, "A monolithic adaptive filter", IEEE J. Solid-State Circuits, vol. SC-18, pp.291-296, June 1983.

[38] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements", IEEE Transactions on Circuits and Systems, Vol. 31, No. 10, pp. 891-894, October 1984.

[39] H. Khorramabadi and P. R. Gray, "High-frequency CMOS continuous-time filters", IEEE Journal of Solid-State Circuits, Vol. SC-19, pp. 939-948, December 1984.

[40] R. R. Torrance, T. R. Viswanathan, and J. V. Hanson, "CMOS Voltage to Current Transducers", IEEE Transactions on Circuits and Systems, Vol. CAS-32, No. 11, pp. 1097-1104, November 1985.

[41] J. L. Pennock, CMOS triode transconductor for continuous-time active integrated filters", Electronics Letters, Vol. 21, pp.817-818, August 1985.

[42] T. R. Viswanathan, "CMOS Transconductance Element", Proceedings of the IEEE, Vol. 74, No.1, pp. 222-224, Januari 1986.

[43] Z. Czarnul, Y. Tsividis, "MOS transconductors and integrators with high linearity", Electronics Letters, Vol. 22, pp. 245-246, February 1986.

[44] Y. P. Tsividis, M. Banu and J. M. Khoury, "Continuous-time MOSFET-C filters in VLSI", IEEE J. Solid State Circuits, Vol. SC-21, pp. 15-29, February 1986.

[45] Z. Czarnul, Y. Tsividis, "MOS tunable transconductor", Electronics Letters, Vol. 22, pp. 721-722, June 1986.

[46] Z. Czarnul, "Novel MOS Resistive Circuit for Synthesis of Fully Integrated Continuous-Time Filters", IEEE Trans. on Circuits and Systems, Vol. CAS-33, No.7, pp. 718-721, July 1986.

[47] C. S. Park and R. Schaumann, "A high-frequency CMOS linear transconductance element", IEEE Transactions on Circuits and Systems, Vol. 33, No. 11, pp. 1132-1138, November 1986.

[48] S. L. Garverick, C. G. Sodini, "Large signal linearity of scaled MOS transistors", IEEE Journal of Solid-state Circuits, Vol. 22, No. 2, pp. 282-286, April 1987.

[49] K. Bult , H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of a MOS transistor in saturation", IEEE Journal of Solid-State Circuits, Vol. 22, No. 3, pp. 357-365, June 1987.

[50] E. Seevinck and R. F. Wassenaar, "A Versatile CMOS Linear Transconductor/Square-law Function Circuit", IEEE Journal of Solid-State Circuits, Vol. 22, No. 3, pp. 366-377, June 1987.

[51] F. Krummenachter, N. Joehl, "A 4-MHz CMOS Continous-Time Filter with On-Chip Automatic Tuning", IEEE Journal of Solid-State Circuits, Vol. 23, no. 3, pp.750-758, June 1988.

[52] K. Bult and H. Wallinga, "A CMOS analog continuous-time delay line with adaptive delay-time control", IEEE J. Solid State Circuits, SC-23, pp. 759-766, June 1988.

[53] E. A. M. Klumperink, E. Seevinck, “Linear-gain amplifier arangement”, Patent Application Number 8802631, The Netherlands, October 26, 1988.

[54] K. Bult, "Analog CMOS square-law circuits", PH.D. dissertation, University of Twente, Enschede, The Netherlands, 1988.

[55] S. L. Wong, "Novel drain-biased transconductance building blocks for continuous-time filter applications", Electronics Letters, Vol. 25, pp. 100-101, January 1989.

[56] B. Nauta and E. Seevinck, "Linear CMOS transconductance element for VHF filters", Electronics Letters, Vol. 25, No.7, pp. 448-450, March 1989.

[57] E. A. M. Klumperink, E. Seevinck, “Linear-gain amplifier arangement”, Patent Application Number 78102418, Taiwan, March 28, 1989.

[58] E.A.M. Klumperink, E. v.d.Zwan, E. Seevinck, "CMOS linear transconductor circuit with constant Bandwidth", Electronics Letters, Vol.25, No.10, pp. 675-676, May 1989.

[59] W. J. Adams, A. Nedungadi, R. L. Geiger, “Design of a Programmable OTA with Multi-Decade Transconductance Adjustment”, 1989 IEEE International Symposium on Circuits and Systems, pp. 663-666, Portland USA, May 8-11, 1989.

[60] E. A. M. Klumperink, E. Seevinck, “Linear-gain amplifier arangement”, Patent Application Number 418414, USA, October 6, 1989.

[61] E. A. M. Klumperink and E. Seevinck, "MOS current gain cells with electronically variable gain and constant bandwidth", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1465-1467, October 1989.

[62] S. Noceti Filho, M. C. Schneider, R. N. G. Robert, "New CMOS ota for fully integrated continuous-time circuit applications", Electronics Letters, Vol. 25, No. 24, pp. 24-26, November 1989.

[63] Z. Wang, "Novel linearisation technique for implementing large-signal MOS tunable transconductors", Electronics Letters, Vol. 26, No. 2, pp. 138-139, January 1990.

[64] Z. Wang and W. Guggenbühl, "A Voltage-Controllable Linear MOS Transconductor using Bias Offset Technique", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pp.135-138, February 1990.

[65] E. Säckinger, W. Guggenbühl, "A High-Swing, High-Impedance MOS Cascode Circuit", IEEE Journal of Solid-State Circuits, Vol. 25, pp.289-297, 1990.

[66] P. M. Van Peteghem, F. G. L. Rice and S. Lee, "Design of a very linear CMOS transconductance input stage for continous-time filters", IEEE J. Solid State Circuits, pp. 497-501, April 1990.

[67] U. Gatti, F. Maloberti and G. Torelli, "A novel CMOS linear transconductance cell for continous-time filters", 1990 IEEE International Symposium on Circuits and Systems, pp. 1173-1176, New Orleans, USA, May 1-3, 1990.

[68] P. Wu, R. Schaumann, and S. Szczepanski, "A CMOS OTA with Improved linearity based on current addition", 1990 IEEE International Symposium on Circuits and Systems, pp. 2296-2299, New Orleans, USA, May 1-3, 1990.

[69] G. Wilson and P. K. Chan, "Low-distortion CMOS transconductor", Electronics Letters, Vol. 26, No. 11, pp. 720-722, May 1990.

[70] B. Stefanelli and A. Kaiser, "CMOS triode transconductor with high dynamic range", Electronics Letters, Vol. 26, pp. 880-881, June 1990.

[71] Z. Czarnul and N. Fujii, "Highly-linear transconductor cell realised by double MOS transistor differential pairs", Electronics Letters, Vol. 26, No. 31, pp. 1819-1821, October 1990.

[72] Z. Czarnul, S. Takagi, "Design of Linear Tuneable CMOS Differential Transconductor Cells", Electronics Letters, Vol. 26, No. 21, pp.1809-1811, October 1990.

[73] S. P. Singh, J. V. Hanson, J. Vlach, "Simple High-Frequency CMOS Transconductor", IEE Proceedings-G, Vol. 137, No. 6, pp.470-474, December 1990.

[74] S. T. Dupuie and M. Ismail, "High Frequency CMOS Transconductors", in "Analogue IC design: the current-mode approach", Edited by C. Toumazou et al, London, Peter Peregrinus Lts., 1990.

[75] K. Bult, G. Geelen, "The CMOS gain boosting Technique", Analog Integrated Circuits and Signal Processing, Vol. 1, pp. 119-135, 1991.

[76] G. Wilson, P.K. Chan, "Saturation-mode CMOS Transconductor with Enhanced Tunability and Distortion", Electronics Letters, Vol. 27, No. 1, pp. 27-29, January 1991.

[77] E. A. M. Klumperink and H. J. Janssen, "Complementary CMOS current gain cell", Electronics Letters, Vol. 27, No. 1, pp. 38-39, January 1991.

[78] E. A. M. Klumperink, "Gate-drain Capacitance Compensation Technique for Triode MOS Transconductors", Electronics Letters, Vol. 27, No.2, pp. 113-115, Januari 1991.

[79] W. Kang, W. H. Lee, W. J. Han, S. W. Kim, "Characteristics of a CMOS Differential Input-Stage using a Source-Coupled Backgate Pair", Journal of the Korean Institute of Telematics and Electronics, Vol. 28a, No. 1, pp. 40-45, Januari 1991.

[80] Z. Wang, "Novel electronically-controlled floating resistors using MOS transistors operating in saturation", Electronics Letters, Vol. 27, pp. 188-189, January 1991.

[81] S. Szczepanski, R. Schaumann and P. Wu, "Linear transconductor based on crosscoupled CMOS pairs", Electronics Letters, Vol. 27, No. 9, pp. 783-785, April 1991.

[82] T. Inoue, F. Ueno, Y. Aramaki, O. Matsumoto, M. Suefuji, “A Design of CMOS OTA’s using Simple Linearizing Techniques and their Application to High-Frequency Contrinuous-Time Filters”, 1991 IEEE International Symposium on Circuits and Systems, pp.1741-1744, Singapore, June 11-14, 1991.

[83] W. J. Adams and J. Ramirez-Angulo, "Extended transconductance adjustment/ linearization technique", Electronics Letters, Vol. 27, No. 10, pp. 842-844, May 1991.

[84] B. Nauta, E. A. M. Klumperink, and W. Kruiskamp, "A CMOS triode transconductor", 1991 IEEE International Symposium on Circuits and Systems, pp. 2232-2235, Singapore, June 11-14, 1991.

[85] J. Silva-Martinez, M. S. J. Steyaert, W. M. C. Sansen, "A Large-Signal Very Low-Distortion Transconductor for High-Frequency Contrinuous-Time Filters", IEEE Journal of Solid-State Circuits, Vol. SC-26, No. 7, July 1991.

[86] P. Wu, R. Schaumann, “Tunable Operational Transconductance Amplifier with Extremely High Linearity over Very Large Input Range”, Electronics Letters, Vol. 27, No.14, pp.1254-1255, July 1991.

[87] H. Tanimoto, M. Koyama, Y. Yoshida, "Realization of a 1-V Active Filter Using a Linearization Technique Employing Plurality of Emitter-Coupled Pairs", IEEE Journal of Solid State Circuits, Vol. SC-26, No.7, July 1991.

[88] M. C. H. Cheng and C. Toumazou, "Linear composite MOSFETs (COMFETs)", Electronics Letters, Vol. 27, No. 20, pp. 1802-1804, September 1991.

[89] J. Sevenhans, M. Van Paemel, "Novel CMOS Linear OTA Using Feedback Control on Common Source Node", Electronics Letters, Vol. 27, No. 20, pp. 1873-1875, September 1991.

[90] J. Ramirez-Angulo, M. Deyong and W.J. Adams, "Applications of composite BICMOS transistors", Electronics Letters, Vol. 27, pp. 2236-2238, November 1991.

[91] E. J. van der Zwan, E. A. M. Klumperink, and E. Seevinck, "A CMOS OTA for HF filters with programmable transfer function", IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, pp. 1720-1724, November 1991.

[92] G. Wilson and P. K. Chan, "Comparison of four CMOS transconductors for fully integrated analogue filter applications", IEE Proceeding-G, Vol. 138, pp. 683-688, December 1991.

[93] Z. Wang, "Current-mode CMOS integrated circuits for analog computation and signal processing: a tutorial", Analog Integrated Circutis and Signal Processing, Vol. 1, pp. 287-295, December 1991.

[94] A. Guzinski, T. Kuley, "New Fully-Balanced OTA Structure", Electronics Letters, Vol. 28, No. 5, pp.498-499, Februari 1992.

[95] S. Szczepanski, J. Jakusz, A. Czarniak, "Differential Pair Transconductor Linearisation via Electronically Controlled Current-mode Cells", Electronics Letters, Vol. 28, No.12, pp.1093-1095, June 1992.

[96] R. Gomez, A. A. Abidi, "A 50-MHz CMOS Variable Gain Amplifier for Magnetic Data Storage Systems", IEEE Journal of Solid-State Circuits, Vol. SC-27, No. 6, pp. 935-939, June 1992.

[97] J. Hauptmann, F. Dielacher, R. Steiner, C. C. Enz, F. Krummenacher, “A Low-Noise Amplifier with Automatic Gain Control and Anticlipping Control in CMOS Technology”, IEEE J. Solid-State Circuits, vol. SC-27, no. 7, pp.974-981, July 1992.

[98] J. Silva-Martinez, M. S. J. Steyaert, W. Sansen, "Design Techniques for High-Performance Full-CMOS OTA-RC Continuous-Time Filters", IEEE Journal of Solid-State Circuits, Vol. SC-27, No. 7, pp. 993-1000, July 1992.

[99] C.S. Kim, Y.H. Kim, S.B. Park, “New Cmos Linear Transconductor”, Electronics Letters, Vol. 28, no. 21, pp. 1962-1964, october 1992.

[100] K. Bult, G. J. G. M. Geelen, "An inherently linear and compact MOST-only current division technique", IEEE Journal of Solid-State Circuits, Vol. 27, no. 12. pg. 1730-1735, december 1992.

[101] R. Raut, “A Novel VCT for Analog IC Applications”, IEEE Transactions on Circuits and Systems-II: Analog and Digtal Signal Processing, Vol. 39, No.12, pp. 882-883, December 1992.

[102] Z. Wang, “Two CMOS large current-gain cells with linearly variable gain and constant bandwidth”, IEEE Transactions on CAS I: Fundamental Theory and Applications, Vol. CAS-39, No. 12, pp. 1021-1024, December 1992.

[103] K. Bult, “The CMOS Gain-Boosting Technique”, Proceedings of the 1992 Workshop on Advances in Analog Circuit Design, pp.81-121, 1992.

[104] E. A. Vittoz, X. Arreguit, "Linear Networks based on Transistors”, Electronics Letters, Vol. 29, no. 3, pp. 297-298, February 1993.

[105] S. C. Huang, M. Ismail, "Linear Tunable COMFET Transconductor", Electronics Letters, Vol. 29, No. 5, pp.459-461, March 1993.

[106] M.C.H. Cheng and C. Toumazou, "Linear Composite MOSFET: Theory, Design, and Applications", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 40, pp. 297-306, May 1993.

[107] S. Szczepanski, A. Wyszynski, R. Schaumann, "Highly Linear Voltage-Controlled CMOS Transconductors", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. CAS-40, No. 4, April 1993.

[108] Durham, A. M., Redman-White, W., "Very high linearity tunable OTA in 5 V CMOS”, IEE Proceedings-G, Vol. 140, no. 3, pp. 207-210, June 1993.

[109] M. F. Li, X. Chen, Y.C. Lim, "Linearity Improvement of CMOS Transconductors for Low Supply Applications", Electronics Letters, Vol. 29, No. 12, pp. 1106-1107, June 1993.

[110] R. J. Wiegerink, “A CMOS Wideband Linear Current Attenuator with Electronically Variable Gain”, 1993 IEEE International Symposium on Circuits and Systems, pp. 962-965, Chicago, USA, May 3-6, 1993.

[111] E. A. M. Klumperink, “Cascadable CMOS current gain cell with gain insensitive phase shift”, Electronics Letters, Vol. 29, No. 23, pp. 2027-2028, November 1993.

[112] B. Nauta, “Analog Cmos Filters for Very High Frequencies”, Kluwer Academic Publishers, ISBN 0-7923-9272-8, 1993.

[113] A. L. Coban, P. E. Allen, "Low-voltage CMOS Transconductance Cell Based on Parallel Operation of Triode and Saturated Transconductors", Electronics Letters, Vol. 30, No. 14, pp.1124-1126, July 1994.

[114] E. A. M. Klumperink, C. H. J. Mensink, P. M. Stroet, Comment on “Low-voltage CMOS transductance cell based on parallel operation of triode and saturation transconductors”, Electronics Letters, Vol. 30, pp. 1824-1825, October 1994.

[115] C. Galup-Montoro, M.C. Schneider, "Series-Parallel Association of FET's for High Gain and High Frequency Applications", IEEE Journal of Solid-State Circuits, Vol. SC-29, pp.1094-1101, 1994.

[116] G. W. den Besten, R. F. Wassenaar, R. J. Wiegerink, "Linear CMOS V-I Conversion Structure with Tunable Transconductance", ICECS '94, Cairo, Egypt, December 19-22 1994.

[117] P. M. Furth, A. G. Andreou, "Linearised Differential Transconductors in Subthreshold CMOS", Electronics Letters, Vol. 31, No. 7, pp. 545-546, March 1995.

[118] I. E. Opris, G. T. A. Kovacs, "Large-Signal Subthreshold CMOS Transconductance Amplifier", Electronics Letters, Vol. 31, No. 9, pp. 718-720, April 1995.

[119] K. Kimura, “A Unified Analysis of Adaptively Biased Emitter- and Source-Coupled Pairs for Linear Bipolar and MOS Transconductance Elements”, IEICE Trans. Fundamentals, Vol. E78-A, No. 4, pp. 485-497, April 1995.

[120] J. J. F. Rijns, "CMOS Low-Distortion High-Frequency Variable-Gain Amplifier", Proceedings of the ESSCIRC '95, Lilli 19-21 September, 1995.

[121] E.A.M. Klumperink, C.T. Klein, B. Rüggeberg, A.J.M. v. Tuijl, “AM Suppression with Small AM-PM Conversion by Means of Variable Gain”, Proceedings of the ESSCIRC ‘95, pp. 214-217, Lille, 19-21 September 1995.

[122] K. Kimura, “A Linear CMOS Transconductance Element of an Adaptively Biased Source-Coupled Differential Pair Using a Quadritail”, IEICE Trans. Fundamentals, Vol. E79-A, No. 2, pp. 184-189, February 1996.

[123] E. A. M. Klumperink, C.T. Klein, B. Rüggeberg, A. J. M. v. Tuijl, “AM Suppression with low AM-PM conversion with the aid of a variable-gain Amplifier”, IEEE Journal of Solid-State Circuits, Vol. 31, No. 5, pp. 625-633, May 1996.

[124] C. H. J. Mensink, B. Nauta, "Tuneable Degenerated Differential Pair", European Patent, No. 96201256.3, May 1996.

[125] C. H. J. Mensink, E. A. M. Klumperink, B. Nauta, "On the Reduction of the Third Order Distortion in a CMOS Triode Transconductor", 1996 IEEE International Symposium on Circuits and Systems, Vol. 1, pg. 223-226, May 1996.

[126] C. H. J. Mensink, B. Nauta, "CMOS Tuneable Linear Current Divider", Electronics Letters, Vol. 32, No. 10, pp. 889-890, May 1996.

[127] J. J. F. Rijns, "CMOS Low-Distortion High-Frequency Variable-Gain Amplifier", IEEE Journal of Solid-State Circuits, Vol. SC-31, no. 7, pp. 1029-1034, July 1996.

[128] S. Szczepanski, R. Schaumann, B. Pankiewicz, “A CMOS Transconductance Element with Improved DC Gain and Wide Bandwidth for VHF Applications”, Analog Integrated Circuits and Signal Processing, Vol. 10, pp. 143-156, 1996.

[129] C. H. J. Mensink, B. Nauta, H. Wallinga, "A 5.5 MHz CMOS Low-pass Filter Using a "Soft-Switched" Transconductor", Proceedings of the ESSCIRC ‘96, pp. 84-87, Neufchâtel, 17-19 September 1996.

[130] C. H. J. Mensink, "Analogue Transconductors for Sub-micron CMOS Technology", Ph.D Thesis, University of Twente, ISBN 90-9009612-4, 1996.

[131] R. F. Wassenaar, "Analysis of Analog C-MOS Circuits", Ph.D. Thesis, University of Twente, Enschede, ISBN 90-9009960-3, 1996.

Multipliers and Other Non-Linear Circuits

[132] I. Házman, "Four-quadrant multiplier using M.O.S.F.E.T. differential amplifiers", Electronics Letters, Vol. 8, No. 3, pp. 63-65, 1972.

[133] O. A. Seriki and R. W. Newcomb, "Direct coupled MOS squaring circuit", IEEE J. Solid-State Circuits, Vol. SC-14, No.4, pp. 766-768, August 1979.

[134] D. C. Soo, R. G. Meyer, "A Four-quadrant NMOS Analog Multiplier", IEEE Journal of Solid-state Circuits, Vol. 17, No.6, pp.1174-1178, December 1982.

[135] Z. Hong and H. Melchior, "Analogue four-quadrant CMOS multiplier with resistors", Electronics Letters, Vol. 21, No. 12, pp. 531-532, June 1985.

[136] J. N. Babanezhad and G. C. Temes, "A 20-V four-quadrant CMOS analog multiplier", IEEE Journal of Solid-State Circuits, Vol. 20, No. 6, pp. 1158-1168, December 1985.

[137] Bang-Sup Song, “CMOS RF Circuits for Data Communications Applications”, IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 2, pp. 310-317, April 1986.

[138] K. Bult and H. Wallinga, "Four-quadrant analog multiplier", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 3, pp. 430-435, June 1986.

[139] S. L. Wong, N. Kalyanasundaram, and C. A. T. Salama, "Wide dynamic range four-quadrant CMOS analog multiplier using linearized transconductance stages", IEEE J. Solid-State Circuits, Vol. SC-21, No. 6, pp. 1120-1122, December 1986.

[140] S. Qin, R. L. Geiger, "An ±5-V CMOS Analog Multiplier", IEEE Journal of Solid-State Circuits, Vol. 22, No. 6, pp. 1143-1146, December 1987.

[141] J.W. Fattaruso, R.G. Meyer, "MOS Analog Function Synthesis", IEEE J. Solid-State Circuits, Vol. SC-22, pp.1056-1063, 1987.

[142] J. S. Peña- Finol and and J. A. Connelly, "A MOS four-quadrant analog multiplier using the quarter-square technique", IEEE J. Solid-State Circuits, Vol. 22, No. 6, pp. 1064-1073, December 1987.

[143] H. Song and C. Kim, "An MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers", IEEE J. Solid-State Circuits, Vol. 25, No. 3, pp. 841-848, June 1990.

[144] P. J. Langlois, "Comment on "A CMOS four-quadrant multiplier": effects of threshold voltage", IEEE Journal of Solid-State Circuits, Vol. 25, No. 6, pp. 1595-1597, December 1990.

[145] E. Seevinck and R. J. Wiegerink, "Generalized translinear circuit principle", IEEE J. Solid-State Circuits, Vol. SC-26, No.8, pp.1098-1102, August 1991.

[146] Z. Wang, "A CMOS Four-Quadrant Analog Multiplier with Single-Ended Voltage Output and Improved Temperature Performance", IEEE Journal of Solide-State Circuits, Vol. SC-26, No. 9, pp. 1293-1301, September 1991.

[147] R. J. Wiegerink, "Analysis and Synthesis of MOS translinear circuits", Kluwer Academic Publishers, 1993.

[148] K. Kimura, “An MOS Four-Quadrant Analog Multiplier Based on the Multitail Technique Using a Quadritail Cell as a Multiplier Core”, IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 42, No. 8, pp. 448-454, August 1995.

Miscelaneous

[149] S. Seshu and M. B. Reed, "Linear Graphs and Electrical Networks", Addison-Wesely Publishing Company Inc., London, 1961.

[150] C. A. Desoer and E. E. Kuh, "Basic Circuit Theory", McGraw-Hill Book Co., New York, 1966.

[151] R. W. Newcomb, "Linear Multiport Synthesis", Mc Graw-Hill, New York, 1966.

[152] D. A. Bell, “Information Theory and its Engineering Applications”, Sir Isaac Pitman & Sons Ltd., London, 1968.

[153] N. Balabanian, T. A Bickart and S. Seshu, "Electrical Network Theory", John Wiley & Sons, Inc., New York, 1969.

[154] G. A. Korn and T. M. Korn, "Electron Analog and Hybrid Computers", MacGraw-Hill, 2nd edition, New York, 1972.

[155] F. Harary, M.P. Palmer, "Graphical Enumeration", Academic Press, New York, 1973.

[156] P. W. Li, M. J. Chin, P. R. Gray, and R. Castello, “A ratio-independent algorithmic analog-to-digital conversion technique”, IEEE Journal of Solid-State Circuits, vol. SC-19, pp. 828-836, 1984.

[157] J. B. Hughes, N. C. Bird, I. C. Macbeth, “Switched Currents - A New Technique for Analogue Sampled-Data Signal Processing”, 1989 IEEE Symposium on Circuits and Systems, pp. 1584-1587, 1989.

[158] M. J. M. Pelgrom, A. C. J. Duinmaijer, A. P. G. Welbers, “Matching Properties of MOS Transistors”, IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1433-1440, October 1989.

[159] G. G. E. Gielen, H. C. C. Walscharts, W. M. C. Sansen, “ISAAC: A Symbolic Simulator for Analog Integrated Circuits”, IEEE Journal of Solid-State Circuits, vol. SC-24, no. 6, pp. 1587-1597, December 1989.

[160] R. Bowman, "Analog Integrated Circuit Design Conceptualization", in "Introduction to Analog VLSI Design Automation", editors. M. Ismail and J. Franca, Boston/Dordrecht/London: Kluwer Academic Publishers, 1990.

[161] B. W. Char, K. O. Geddes, G. H. Gonnet, B. L. Leong, M. B. Monagan, S. M. Watt, “Maple V Language Reference Manual”, Springer-Verlag, New York, 1991.

[162] P. E. de Haan, S. v. d. Elshout, E. A. M. Klumperink, K. Bult, “Analysis of a Current Mode Most-Only-D-A Converter”, Proceeding of the ESSCIRC ‘94, pp. 188-191, Ulm, 22-24 September 1994.

[163] C. Toumazou, C. A. Makris, "Analog IC Design Automation: Part I - Automated Circuit Generation: New Concepts and Methods", IEEE Trans. on CAD of Integrated Circuits and Systems, Vol. 14, No. 2, pp. 218-238, February 1995.

[164] A. J. Annema, “Feed-Forward Neural Networks: Vector Decomposition Analysis, Modelling and Analog Implementation”, Norwell MA: Kluwer Academic Publishers, 1995.

References

Veel transistor basiscircuits hebben een overdracht die in hoofdzaak bepaald wordt door de transconductantie van transistoren (bv. transconductors en versterkertrappen). Zulke *"Transconductance Based Circuits"* zijn het onderwerp van dit proefschrift. Deze schakelingen kunnen een elektronisch regelbare overdracht hebben, zoals nodig in zelf-corrigerende of programmeerbare systemen, doordat de transconductantie van een transistor te variëren is via het instelpunt. Bovendien gaat het om eenvoudige schakelingen met vaak goede hoogfrequenteigenschappen.

Dit proefschrift richt zich op het generaliseren en systematiseren van het ontwerpproces. De achterliggende gedachte is dat veel transistorcircuits te zien zijn als verschillende uitvoeringsvormen van een zeer beperkt aantal principes. De belangrijkste onderwerpen die aan bod komen zijn de *systematische generatie van circuit topologiën*, en de *klassifikatie en analyse* van de resulterende circuits. Hoewel het proefschrift zich richt op MOST circuits, zijn vele resultaten ook bruikbaar voor andere implementaties (bv. bipolaire transistoren). Om tot generalisatie te komen, wordt een MOS transistor of transistorpaar gemodelleerd als een spanningsgestuurde stroombron (VCCS (Voltage Controlled Current Source)). Daarbij wordt de grootsignaal $I_D(V_{GS})$ karakteristiek, afhankelijk van het werkingsgebied van de MOST, in eerste orde benadering gemodelleerd als een lineaire (LVCCS), kwadratische (SVCCS) of exponentiële (EVCCS) funktie. Zonodig worden daaraan tweede-orde effekten toegevoegd.

Na een motivatie en historisch overzicht in hoofdstuk 1, worden in hoofdstuk 2 de eisen onderzocht die gesteld kunnen worden aan lineaire transactors (tweepoorten met een overdrachtsfunktie ongelijk aan nul). Dit wordt gedaan vanuit vier gezichtpunten: de aanpassing van een transactor aan de signaalbron en belasting, de gewenste overdrachtsfunktie, de geschiktheid voor zelf-corrigerende en programmeerbare systemen en de compatibiliteit met spannings- en stroomsignalen. Het blijkt dat de negen transactors met poortimpedanties die ofwel zeer laag, zeer hoog of lineair en nauwkeurig zijn, bij uitstek geschikt zijn. De transmissie tweepoort parameters van deze transactors dienen ofwel nauwkeurig ofwel elektronisch varieerbaar te zijn.

Vervolgens worden in hoofdstuk 3 de mogelijkheden onderzocht om de gewenste transactors met VCCSen te implementeren. Daarvoor blijken minimaal twee VCCSen nodig te zijn om naast V-I en I-V overdrachten ook V-V en I-I overdrachten mogelijk te maken. Met behulp van lineaire grafen worden dan alle topologiën van transactors met twee VCCSen gegenereerd. Vervolgens worden deze met een computerprogramma geanalyseerd qua transmissie parameters, hetgeen leidt tot 145 grafen van transactors met een overdracht ongelijk aan nul (Appendix A). Het blijkt dat de negen bij uitstek bruikbare typen transactors ofwel direkt geïmplementeerd kunnen worden, ofwel benaderd kunnen worden door grote transconductantiewaarden te kiezen. Hun transmissie parameters zijn een funktie van de twee transconductanties van de VCCSen.

In hoofdstuk 4 wordt beschreven hoe iedere VCCS in principe op meerdere manieren geïmplementeerd kan worden. Daardoor kunnen vele honderden verschillende transistor topologiën afgeleid worden uit de 145 grafen. De eenvoudigst mogelijke implementatie hangt af van de aanwezigheid van gemeenschappelijk knooppunten voor de spannings- en stroom-tak van een VCCS in een graaf, en de tak-oriëntatie, en is ofwel een weerstand, een MOST of een MOST-paar. Vanuit een gespecificeerd tweepoort gedrag kunnen nu systematisch circuit topologiën gegenereerd worden. Als voorbeeld worden versterkertrappen gesynthetiseerd voor een IF AGC-versterkertrap t.b.v. een TV-ontvanger. Alternatieve ontwerpen blijken grote verschillen in gedrag te vertonen.

Hoewel er vele verschillende circuits mogelijk zijn, is het aantal verschillende transmissie parameter uitdrukkingen beperkt. In hoofdstuk 5 wordt aangetoond dat dit komt doordat er slechts een beperkt aantal mogelijkheden is om twee VCCSen te gebruiken, waarbij twee mathematische relaties tussen de spanningen en stromen van de VCCSen een cruciale rol spelen. Onder de aanname dat alleen Kirchhoff relaties mogelijk zijn (transactors enkel bestaand uit twee VCCSen en verbindingen), worden alle mogelijkheden in kaart gebracht. Sommige van de circuits met twee VCCSen kunnen beschouwd worden als twee onafhankelijke circuits met ieder één VCCS ("1VCCS circuits"). In andere gevallen is dat niet mogelijk ("2VCCS circuits"). De 1VCCS circuits kunnen in 2 klassen worden ingedeeld. De 2VCCS circuits kunnen onderverdeeld worden in 3 hoofdklassen en 14 subklassen, gebaseerd op verschillende sets van twee oplegbare Kirchhoff relaties. De *klassifikatie* is nuttig voor circuit synthese en analyse, omdat ze een *overzicht* geeft van alle *wezenlijk verschillende mogelijkheden* om twee VCCSen te gebruiken. Bovendien maakt ze het mogelijk om in *één analyse* een *complete klasse* van circuits te analyseren.

De analyse van klassen van circuits wordt in de hoofdstukken 6 t/m 8 uitgevoerd voor gedragsaspekten die via een VCCS-model beschreven kunnen worden. Dit resulteert in hiërarchische macro-modellen voor 2VCCS circuits. Het kleinsignaalgedrag wordt per hoofdklasse uitgedrukt in VCCS-transconductantie waarden, met behulp van een set van symbolische vergelijkingen. Verder worden per subklasse grootsignaalvergelijkingen afgeleid voor de LVCCS, SVCCS en EVCCS modellen in termen van I(V) model parameters. Hiermee kan het instelpunt, het stroomverbruik, het regelbereik en de instuurgrenzen afgeschat worden. Verder wordt het zwak niet-lineaire gedrag uitgedrukt in termen van 1^e, 2^e en 3^e orde Taylor coefficiënten van de I(V) karakteristiek van de VCCSen. Tenslotte worden symbolische expressies voor het ruisgedrag afgeleid, uitgedrukt in de transconductantie en Noise excess factor (NEF) van de VCCS.

In hoofdstuk 8 worden ca. 50 CMOS transconductor circuits uit de literatuur geklassificeerd in 5 klassen van 2VCCS circuits. Daarna wordt de funktionele kern van V-I converters met twee gematchte MOSTen onder de loep genomen. Het blijkt dat er 4 gevallen met wezenlijk verschillend gedrag bestaan, waarvoor formules worden afgeleid voor de transconductanctie, het dynamisch bereik en de voedingsstroom. De analyse geeft inzicht in de relatieve merites van verschillende circuits en in hun maximaal haalbare dynamisch bereik. Tenslotte worden de klassifikatie en analyse technieken toegepast op de in hoofdstuk 4 beschreven versterkertrap ontwerpen. Het blijkt dat de macro-modellen een redelijk eerste orde afschatting geven van de simulatieresultaten.

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Curriculum Vitae & List of Publications

Curriculum vitae

Eric A.M. Klumperink was born on april 4th, 1960 in Lichtenvoorde, The Netherlands. In 1978 he received his VWO diploma from the "Marianum Scholengemeenschap" in Groenlo. In 1982 he got his HTS-diploma from the HTS in Enschede. He was then involved in several short industrial projects in hardware and software design. In 1984 he joined the IC-technology and Electronics (ICE-) group of the Electrical Engineering department at Twente University. He was mainy engaged in the design and characterisation of CMOS semi-custom arrays and in the education of students in analog CMOS circuit design. Since 1990, he is also involved in analog CMOS circuit research at the MESA Research institute at Twente University. His primary interest is in the area of basic analog signal processing blocks like V-I converters and amplifier circuits and their applications.

List of Publications

[1] E.A.M. Klumperink, E. v.d.Zwan, E. Seevinck, "CMOS linear transconductor circuit with constant Bandwidth", Electronics Letters, Vol.25, No.10, pp. 675-676, May 1989.

[2] E. A. M. Klumperink and E. Seevinck, "MOS current gain cells with electronically variable gain and constant bandwidth", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1465-1467, October 1989.

[3] E. A. M. Klumperink, E. v. d. Zwan, E. Seevinck, “CMOS V-I converter with independently variable transconductance and bandwidth”, Proceedings of the 2nd Symposium on design methodology, Dalfsen, pp. 209-209, 1990.

[4] E. A. M. Klumperink and H. J. Janssen, "Complementary CMOS current gain cell", Electronics Letters, Vol. 27, No. 1, pp. 38-39, January 1991.

[5] E. A. M. Klumperink, "Gate-drain Capacitance Compensation Technique for Triode MOS Transconductors", Electronics Letters, Vol. 27, No.2, pp. 113-115, Januari 1991.

[6] E. J. van der Zwan, E. A. M. Klumperink, and E. Seevinck, "A CMOS OTA for HF filters with programmable transfer function", IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, pp. 1720-1724, November 1991.

[7] B. Nauta, E. A. M. Klumperink, and W. Kruiskamp, "A CMOS triode transconductor", Proceedings of the ISCAS '91, pp. 2232-2235, June 1991.

[8] P. E. de Haan, E. A. M. Klumperink, M. G. v. Leeuwen, H. Wallinga, “Extending a CMOS Digital Sea-Of-Gates Array towards Mixed Signal Applications", Proceedings of the IEEE/PRORISC Workshop on Circuits, Systems and Signal Processing, pp. 57-62 Houthalen, Belgium, 24/3/1993.

[9] E. A. M. Klumperink, “Cascadable CMOS current gain cell with gain insensitive phase shift”, Electronics Letters, Vol. 29, No. 23, pp. 2027-2028, November 1993.

[10] P. E. de Haan, S. v. d. Elshout, E. A. M. Klumperink, K. Bult, “Analysis of a Current Mode Most-Only-D-A Converter”, Proceedings of the ESSCIRC, pp. 188-191, 1994.

[11] E.A.M.Klumperink, C.H.J. Mensink, P. M. Stroet, Comment on “Low-voltage CMOS transductance cell based on parallel operation of triode and saturation transconductors”, Electronics Letters, 30, pp. 1824-1825, 1994.

[12] P. E. de Haan, E. A. M. Klumperink, M. G. v. Leeuwen, H. Wallinga, "DC Modeling of Composite MOS Transistors", Proceeding of the ESSDERC '95, pp. 801-804, The Hague, 25/9/1995.

[13] E. A. M. Klumperink, C. T. Klein, B. Rüggeberg, A. J. M. v. Tuijl, “AM Suppression with Small AM-PM Conversion by Means of Variable Gain”, Proceedings of the ESSCIRC ‘95, Lille, 19-21 September, 1995.

[14] E. A. M. Klumperink, C.T. Klein, B. Rüggeberg, A. J. M. v. Tuijl, “AM Suppression with low AM-PM conversion with the aid of a variable-gain Amplifier”, IEEE Journal of Solid-State Circuits, Vol. 31, No. 5, pp. 625-633, May 1996.

[15] C. H. J. Mensink, E. A. M. Klumperink, B. Nauta, "On the Reduction of the Third Order Distortion in a CMOS Triode Transconductor", 1996 IEEE International Symposium on Circuits and Systems, Vol. 1, pg. 223-226, 1996.

[16] M. W. Hauser, E. A. M. Klumperink, R. G. Meyer, W. D. Mack, "Variable-Gain, Variable-Transconductance, and Multiplication Techniques: A Survey", In W. Sansen et al, editors, Analog Circuit Design, Dordrecht: Kluwer Academic Publishers, 1997.

Patents

[17] E. A. M. Klumperink, E. Seevinck, “Linear-gain amplifier arangement”
Patent Application Number 8802631, The Netherlands, October 26, 1988
Patent Application Number 78102418, Taiwan, March 28, 1989
Patent Application Number 418414, USA, October 6, 1989.