2009 International Microwave Symposium

Workshop
WSB

# Recent Advances in Low Jitter CMOS Clock Generation Stimulated by FoM Definitions

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# Outline

- Introduction
- Admittance Level Scaling
- FoM for Oscillator Phase Noise
- Relaxation Oscillator Design
- FoM for Absolute Jitter
- Multi-Phase Clock Generator Design
- FoM for PLL Jitter
- Sub-Sampling PLL Design
- Conclusions

# Introduction: Why FoMs?

Why define a Figure of Merit (FoM)?

- Compare relative merits

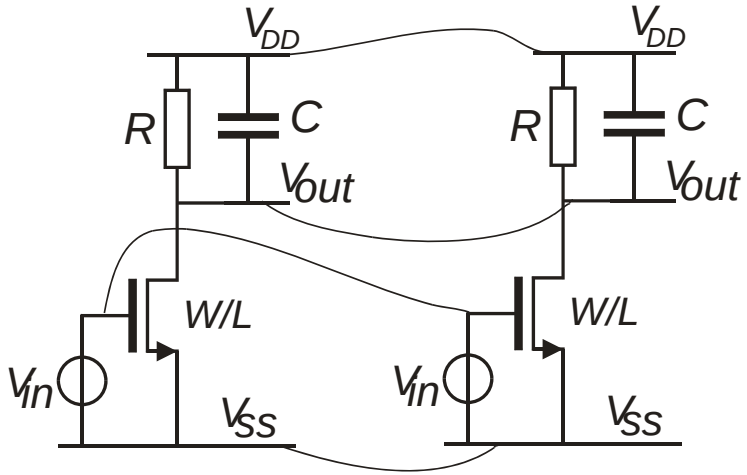
… most beautiful ….?

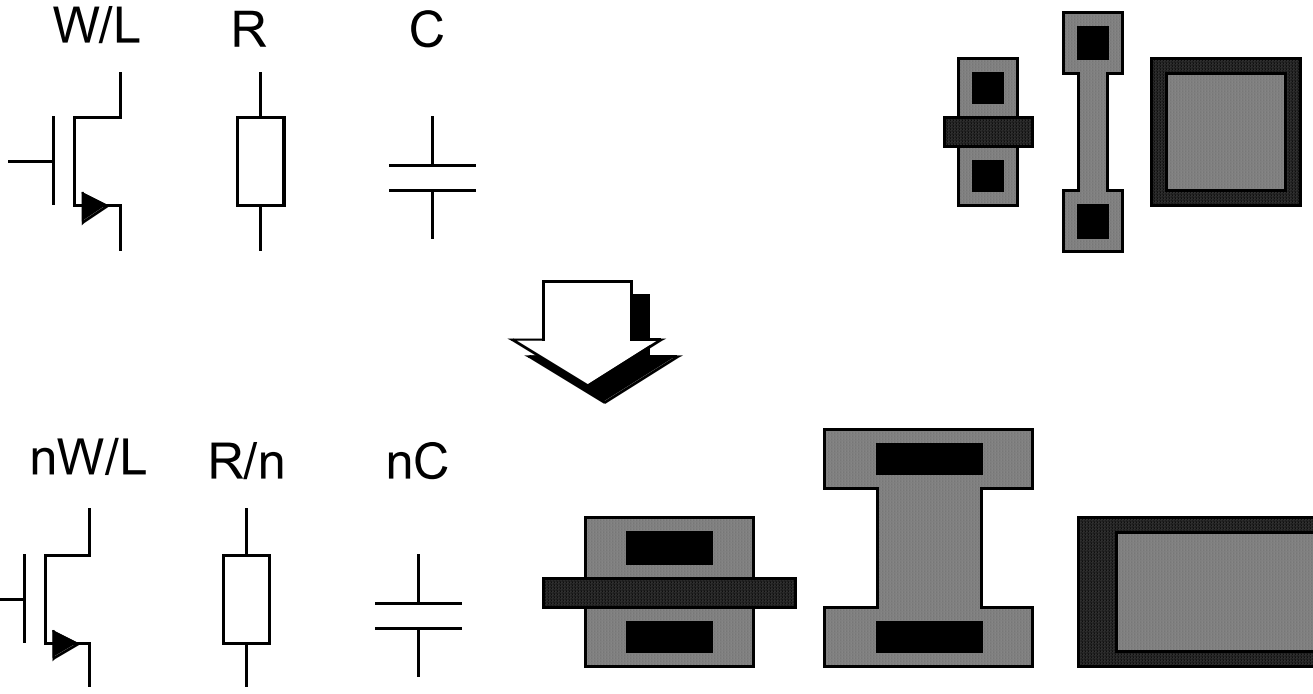
Challenge in defining FoMs: “fair”

- Fundamental basis?
- Help designers to approach fundamental limits

# Admittance Level Scaling

Design recipe to lower noise:



# Admittance Level Scaling

- Results:
- $\sigma_v^2$ /n
- Power x n
- Area x n

remarks:

- same voltage, currents x n
- poles/zeros not affected
- Bias-voltage related properties don't change

SNR improved x n, at cost of n x Power

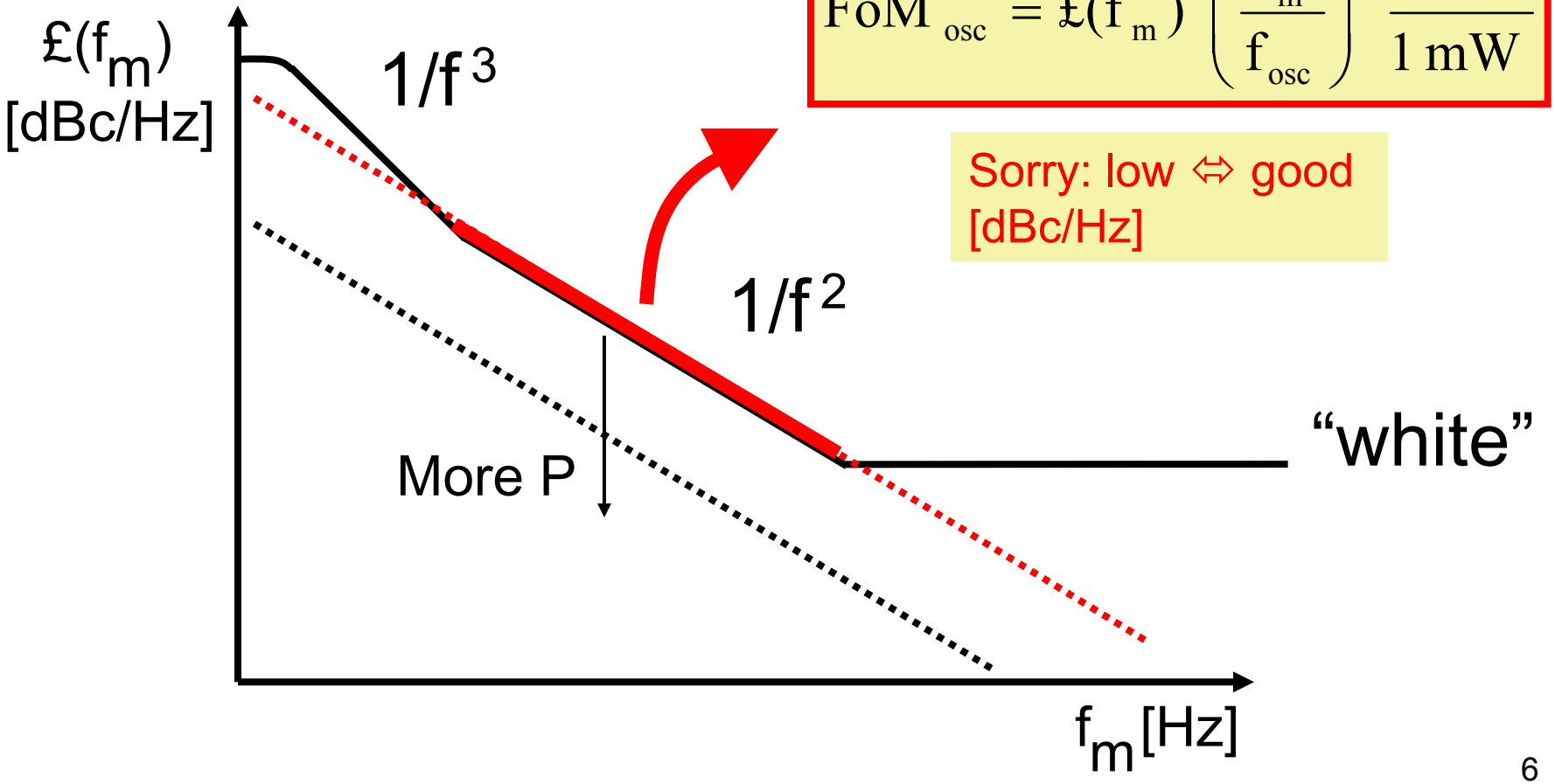
More fair comparison: FoM = SNR / P

# Oscillator Phase-noise and FoM

SNR for Oscillator ⇔ $1/\pounds(f_m)$

$$FoM_{osc} = \pounds(f_m)\left(\frac{f_m}{f_{osc}}\right)^2 \frac{P}{1\,mW}$$

Sorry: low ⇔ good [dBc/Hz]



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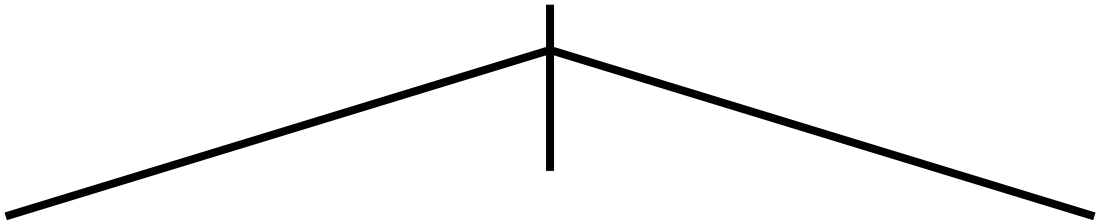
# RC Oscillators



## Ring Oscillators

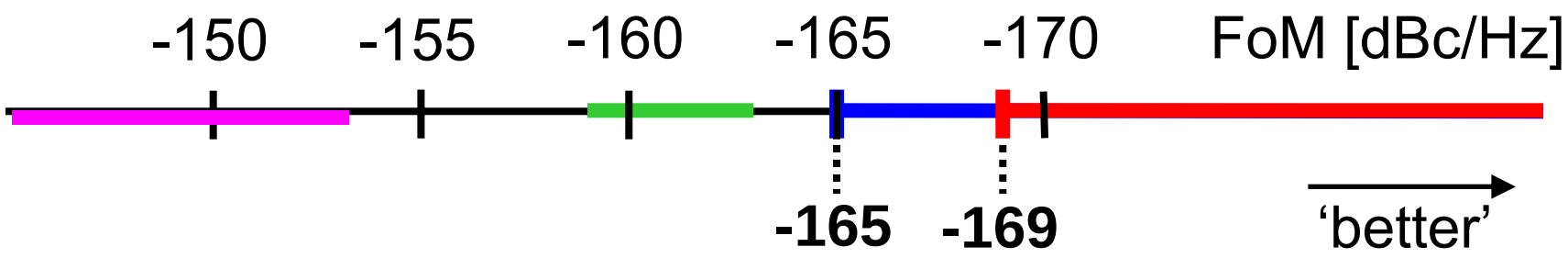
+ small area
+ large tuning range

…

## Relaxation Oscillators

+ small area
+ large tuning range
+ linear tuning
- **poor phase-noise performance**

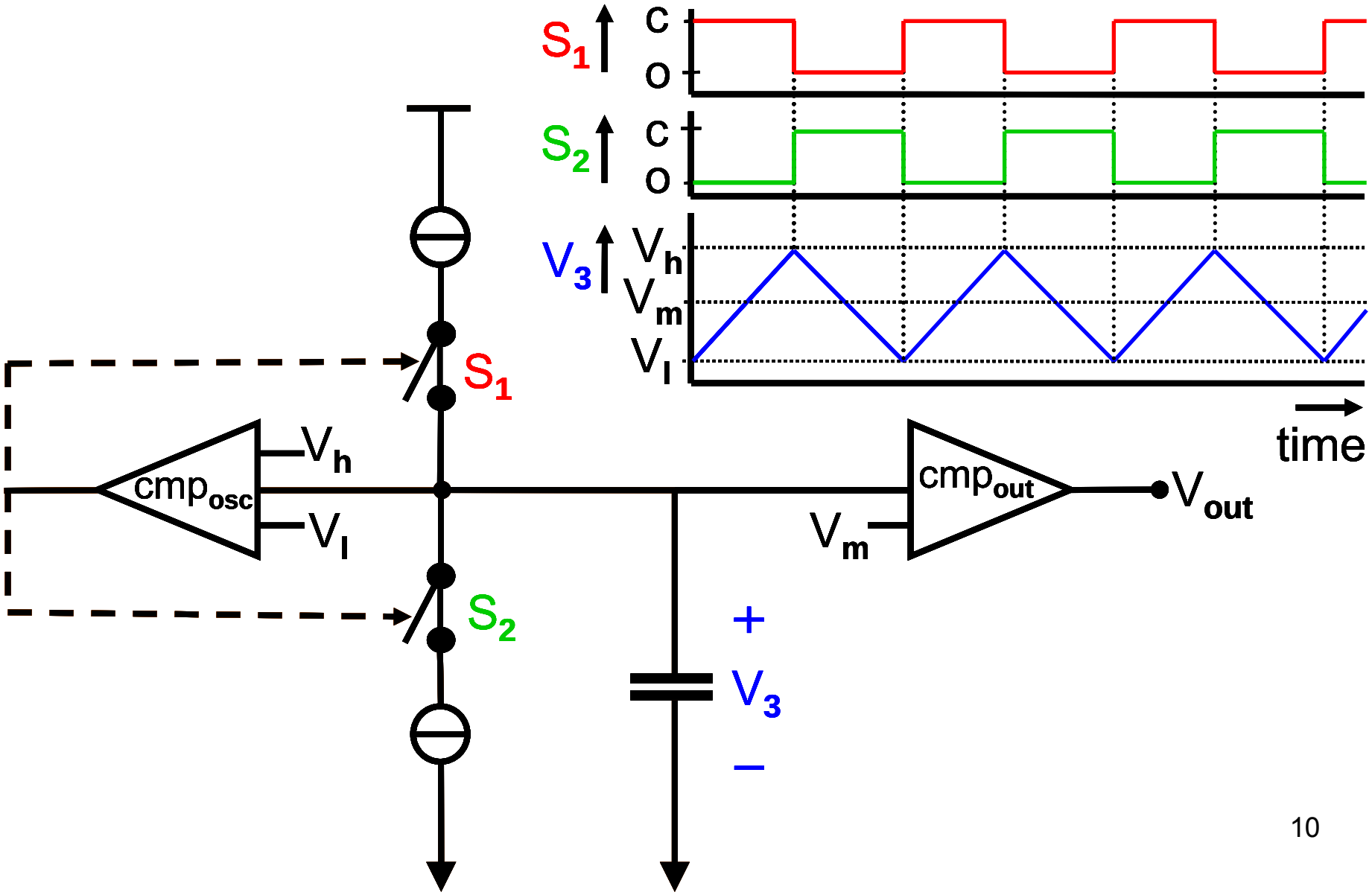
# Typical Figures of Merit




- theoretical limit relaxation oscillators
- theoretical limit ring oscillators
- practical ring oscillators
- practical relaxation oscillators

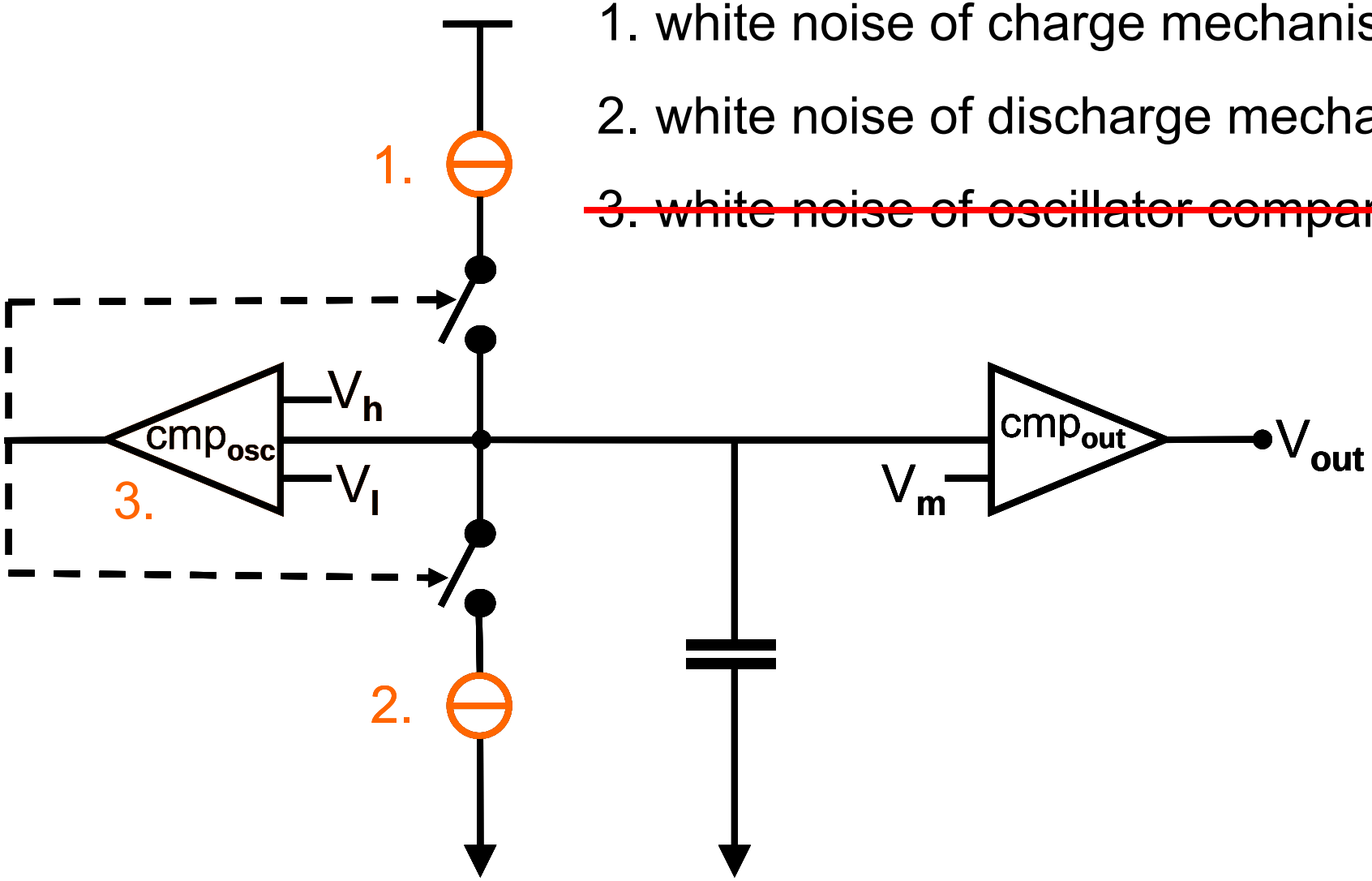
[Navid, JSSC05] @ 290K

# Typical Relaxation Oscillator

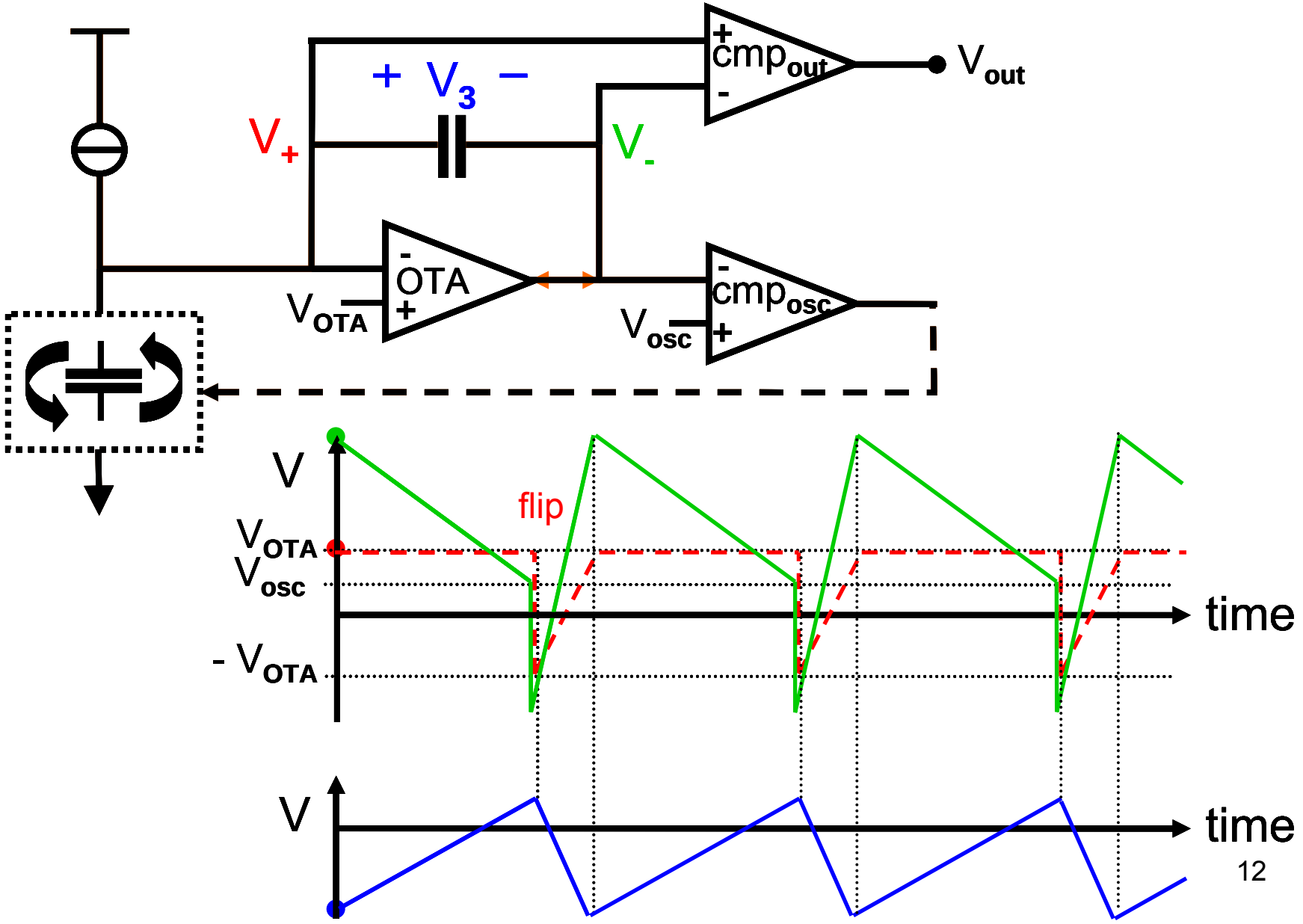


# Sources of $1/f^2$ Phase-noise

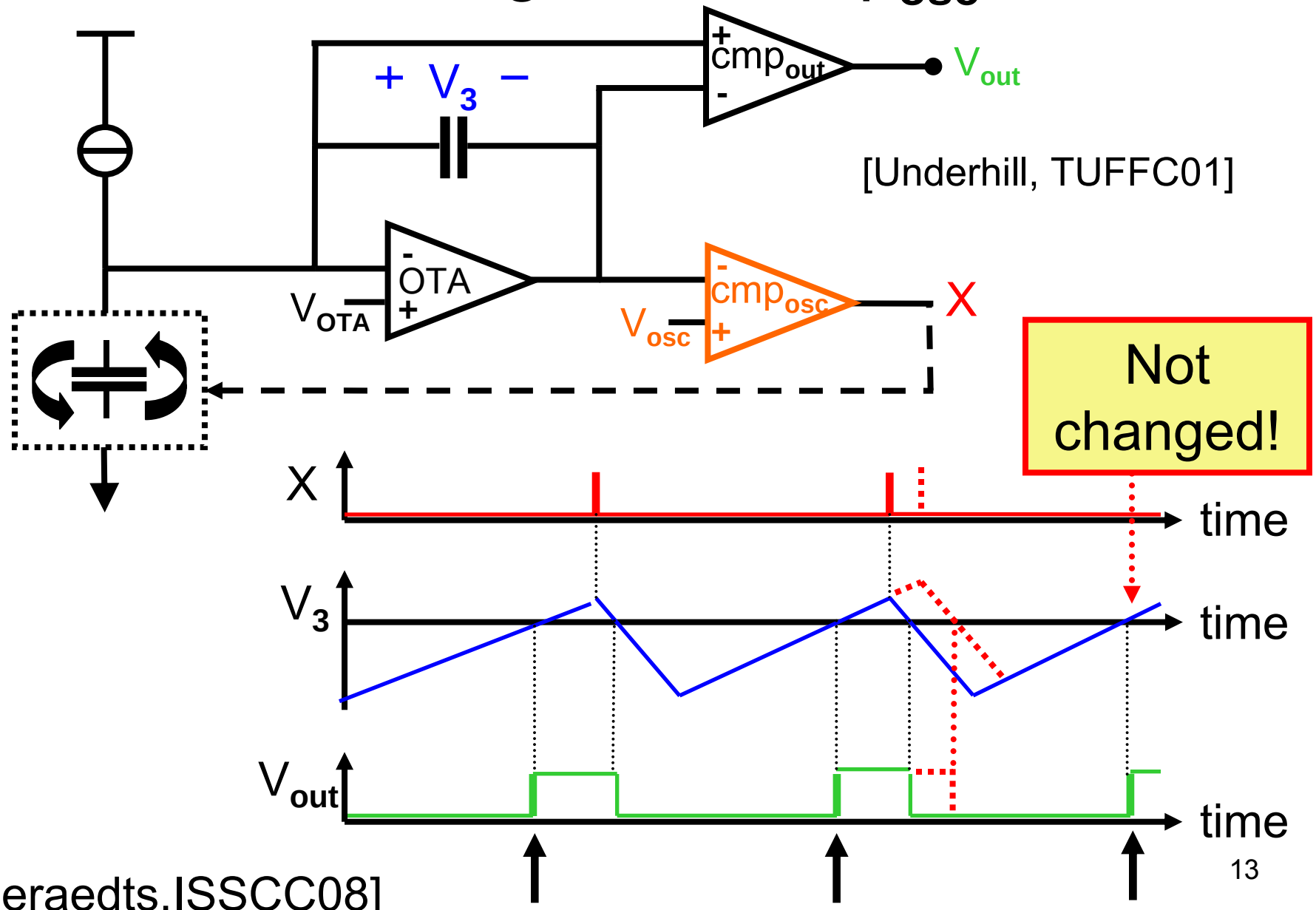
1. white noise of charge mechanism
2. white noise of discharge mechanism
~~3. white noise of oscillator comparator~~



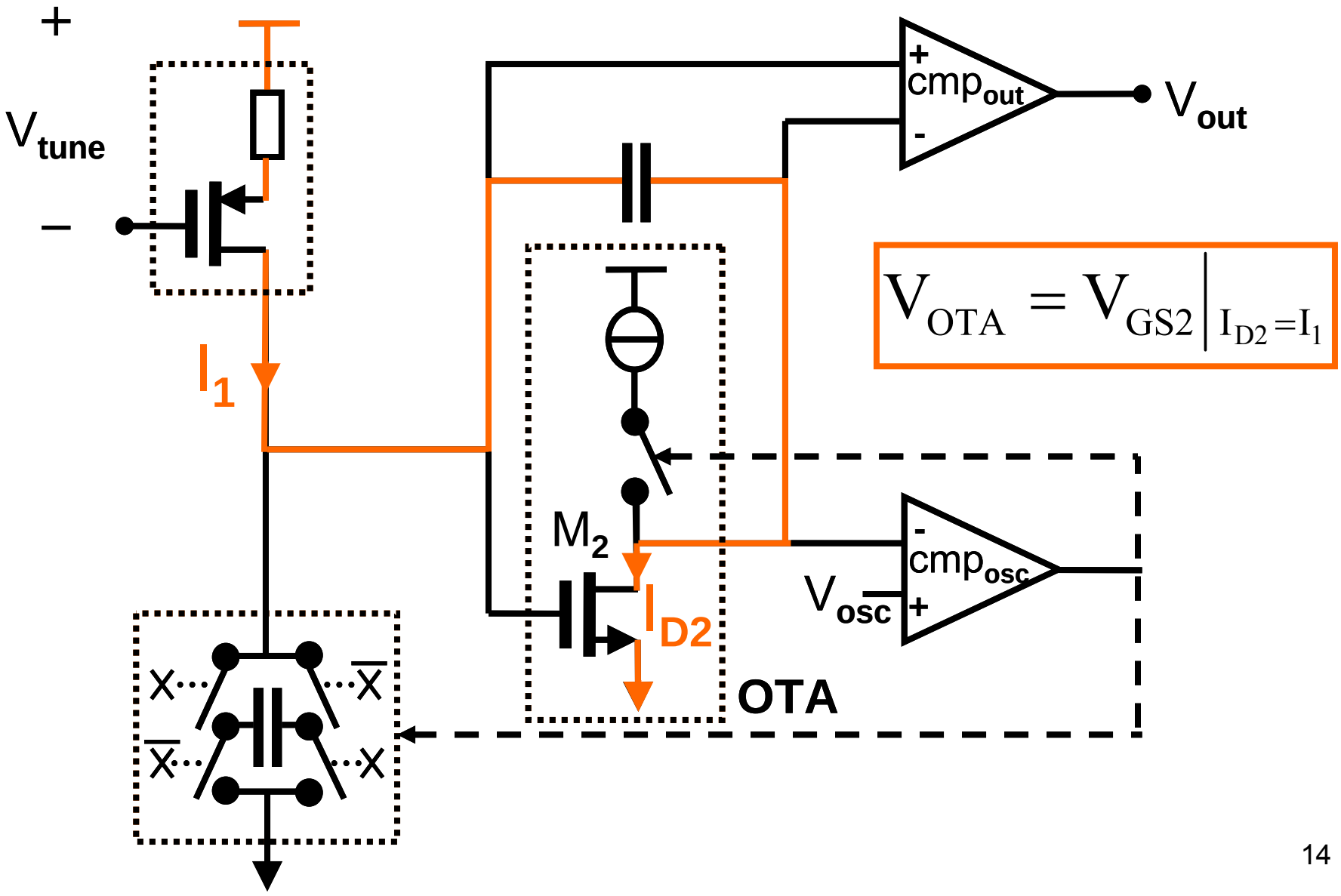
# Improved Relaxation Oscillator



# Filtering Noise $cmp_{osc}$



# Actual Implementation

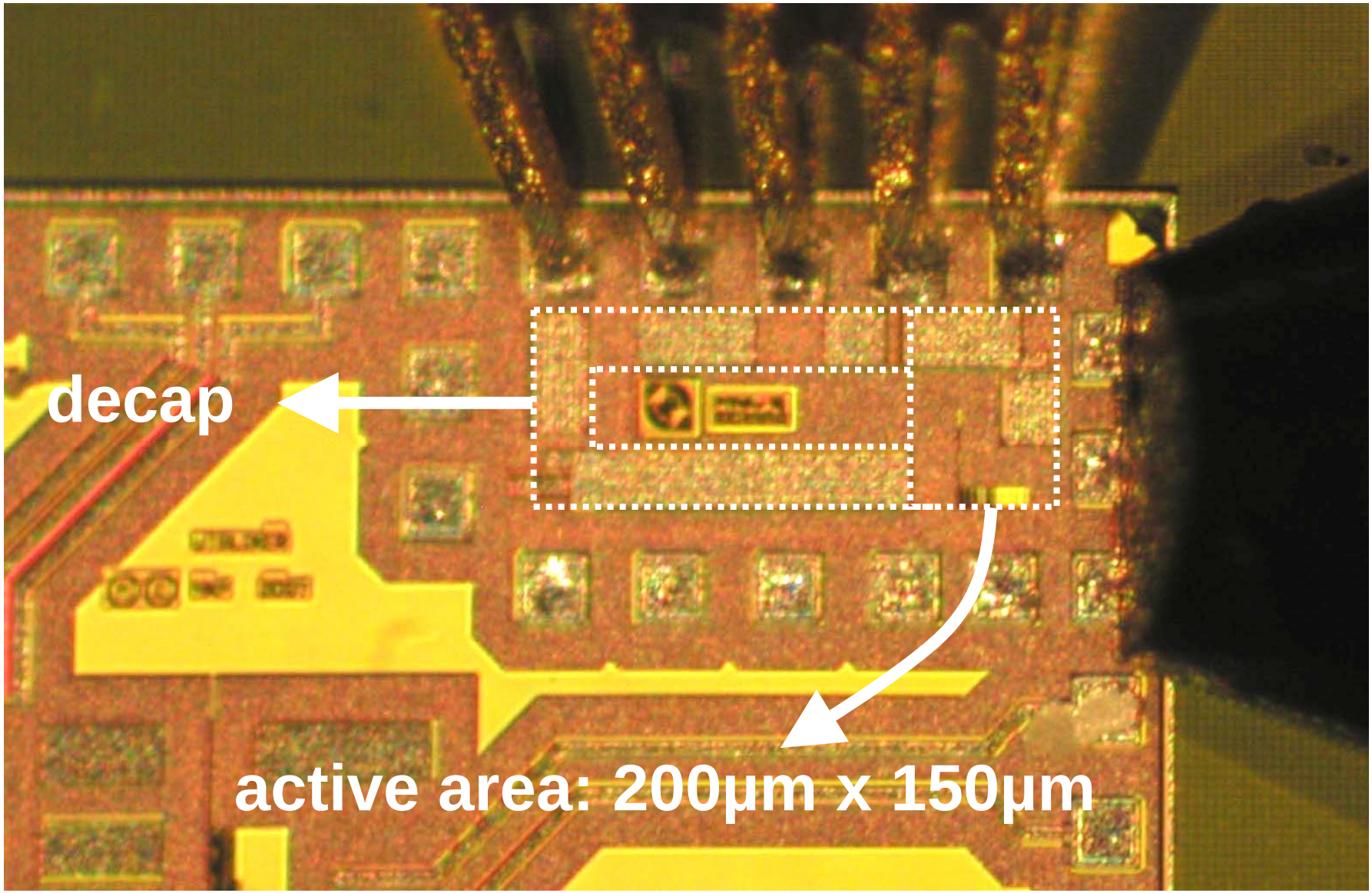


# First-order Design Choices

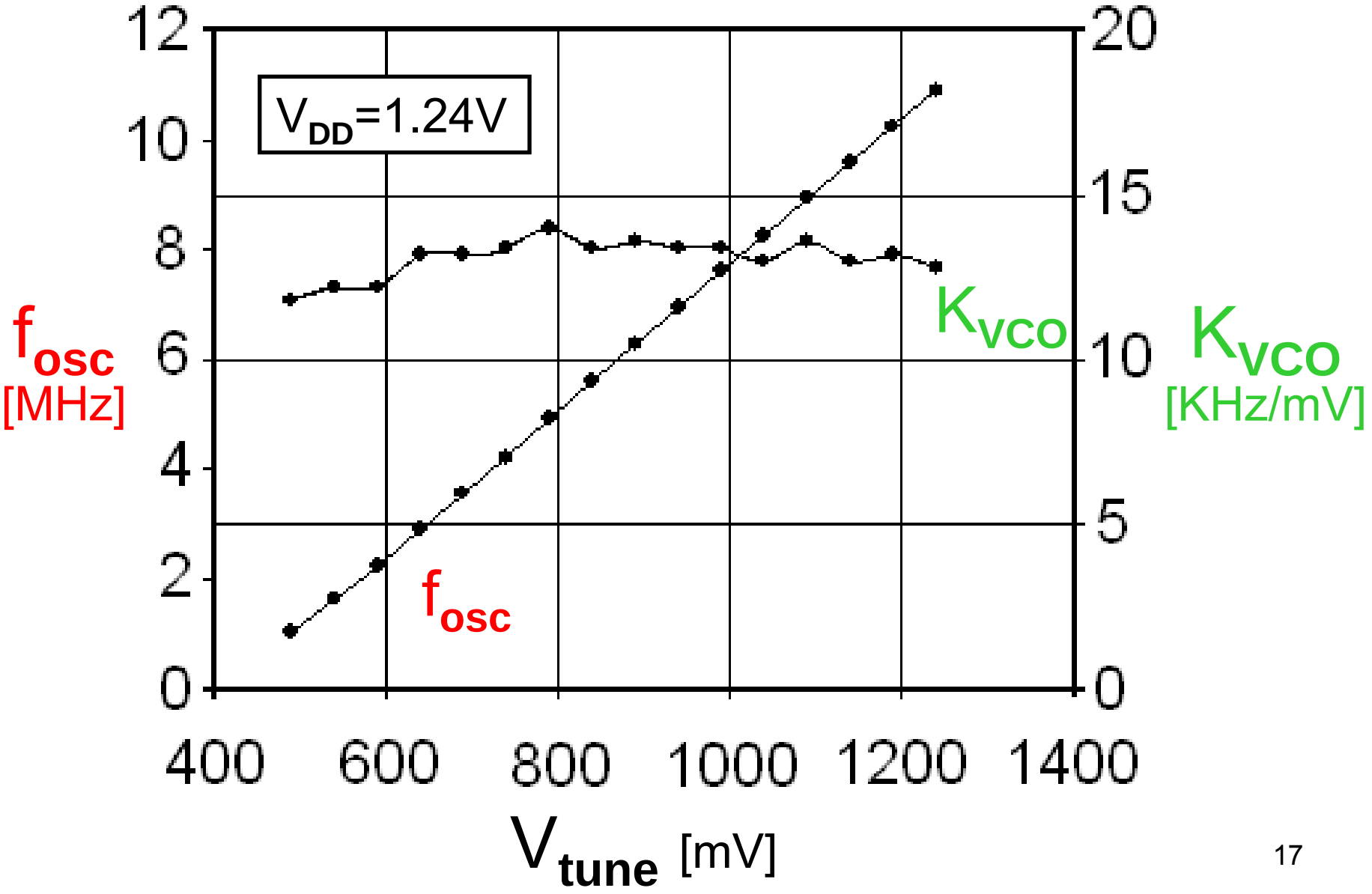
- process: standard 65nm CMOS ($V_{DD}$ = 1.2V)
- voltages: $\Delta V_1 = \Delta V_2 = \Delta V_3 = 2V_{DD}/3$
- currents: $I_1 = I_2/4 = 25\mu A$
- capacitors: $C_1 = C_2 = 2.5pF$

$\Leftrightarrow f_{osc} \approx 12.5MHz$

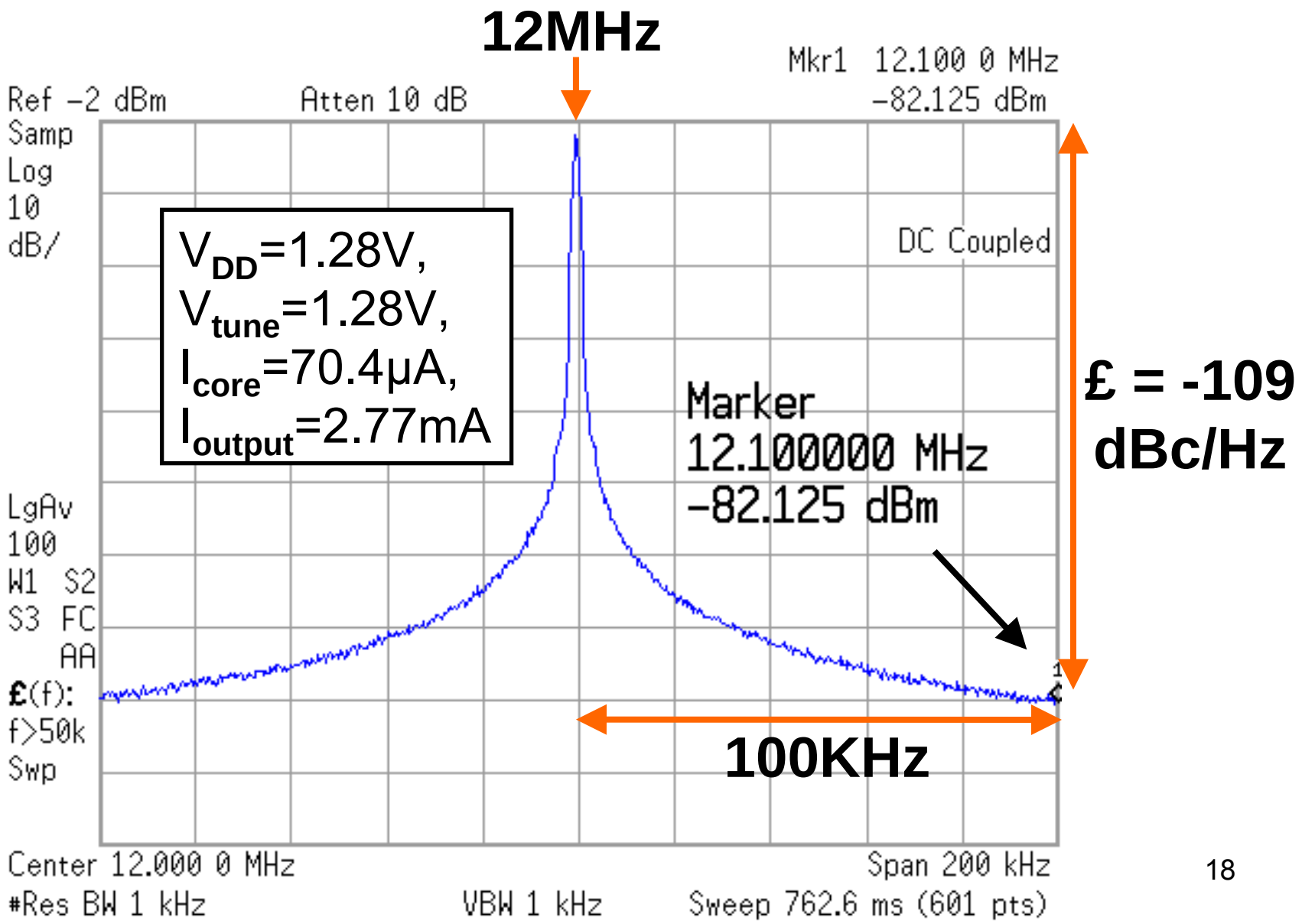
# Micrograph



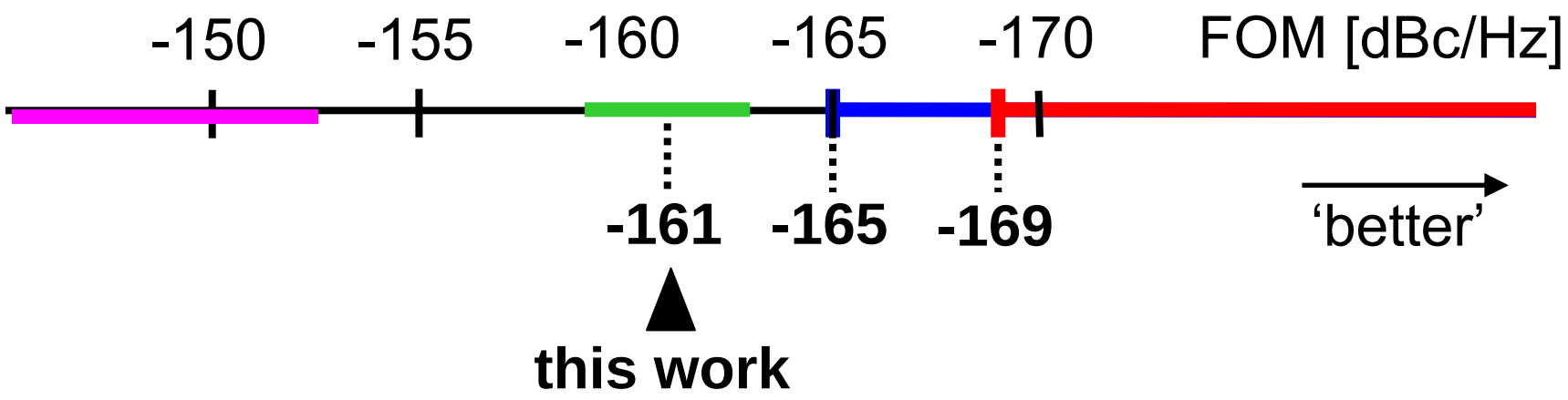
# Measured Tuning Range



# Measured Phase-noise



# Typical Figures of Merit




theoretical limit relaxation oscillators

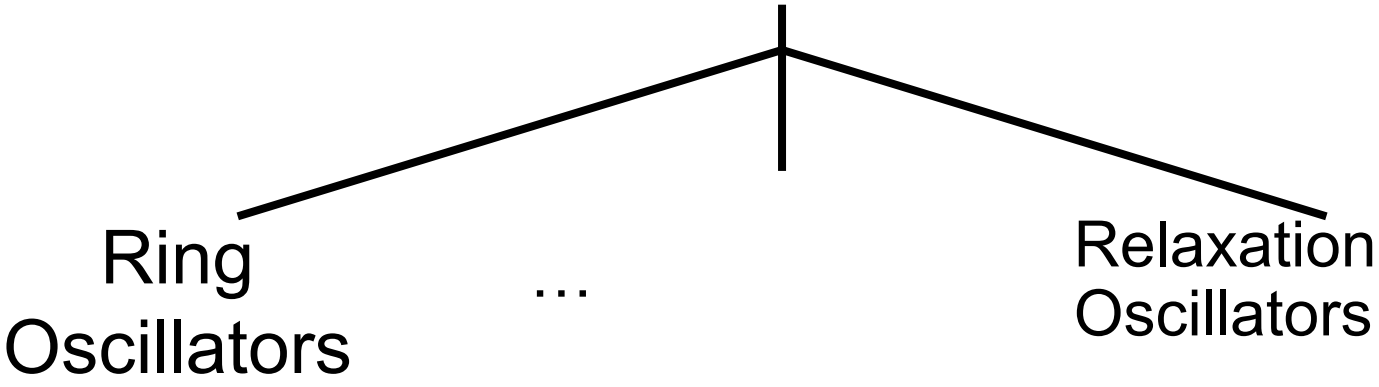
theoretical limit ring oscillators

practical ring oscillators

practical relaxation oscillators

[Navid, JSSC05] @ 290K

# RC Oscillators




+ small area
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+ linear tuning
- **poor phase-noise**

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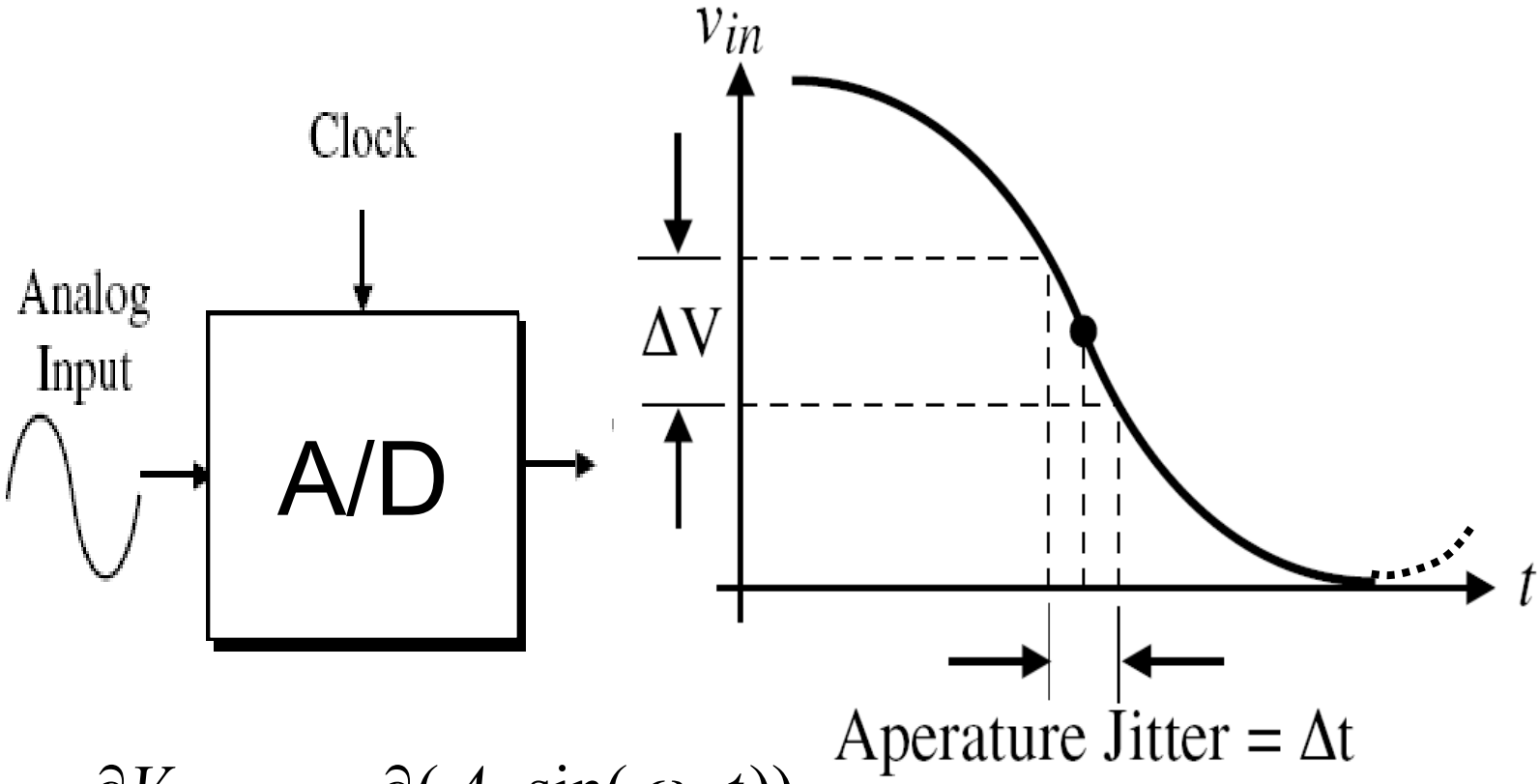
# (Absolute) jitter and sampling error



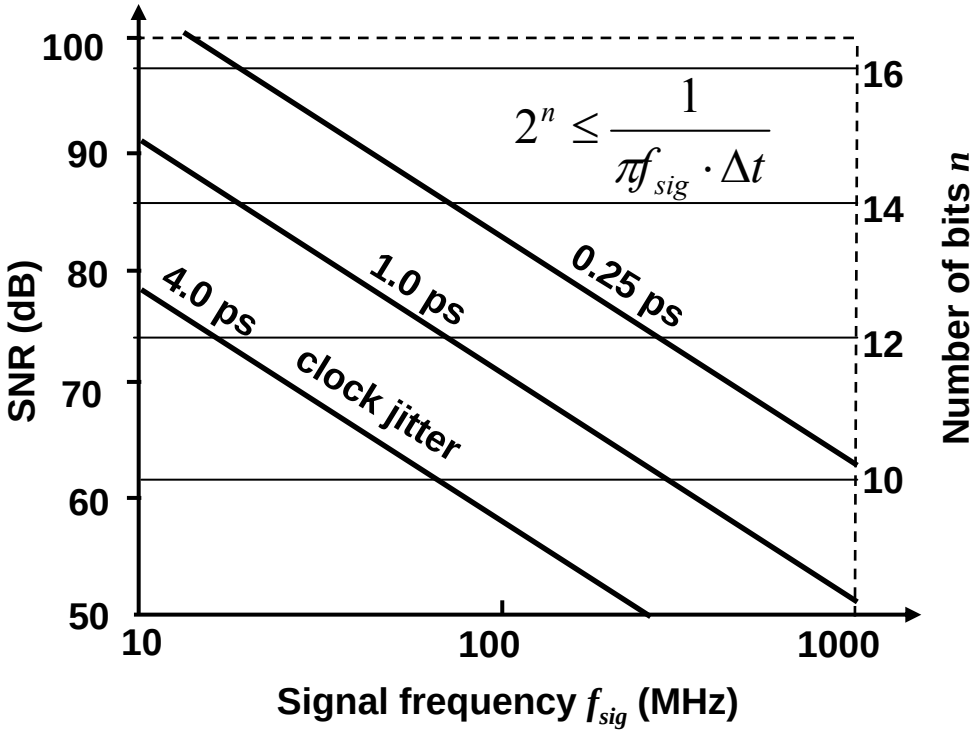

$$\Delta V = \frac{\partial V_{in}}{\partial t}\Delta t = \frac{\partial(A \cdot \sin(\omega \cdot t))}{\partial t}\Delta t = A \cdot \omega \cdot \Delta t \cdot \cos(\omega \cdot t)$$

Maximum Voltage sampling error around zero crossing:

Must usually be smaller then LSB => absolute jitter requirement

# FoM for Jitter

Long term absolute jitter relevant for ADC: $\sigma_t$




Jitter Variance scales with admittance, so:

$$FoM_{abs.jitter} = \sigma_t^2 \cdot P$$

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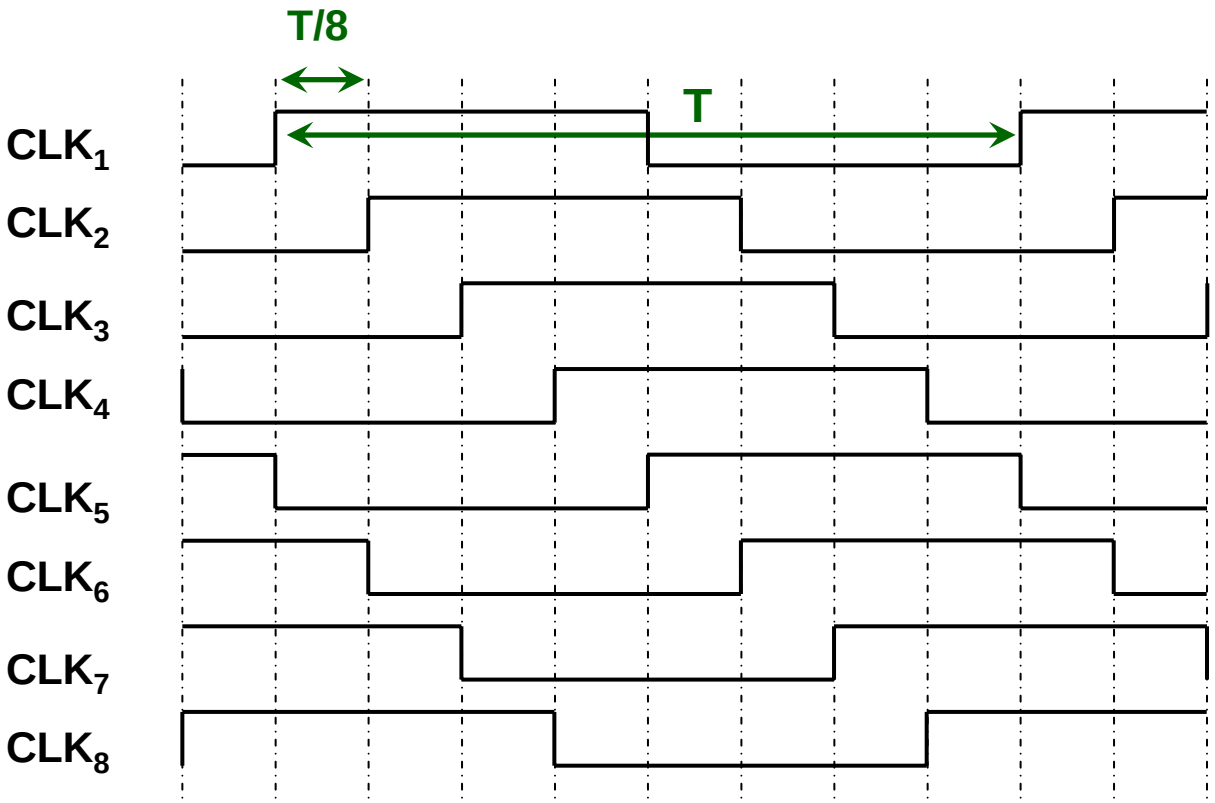
# What and Why of Multi-phase Clocks

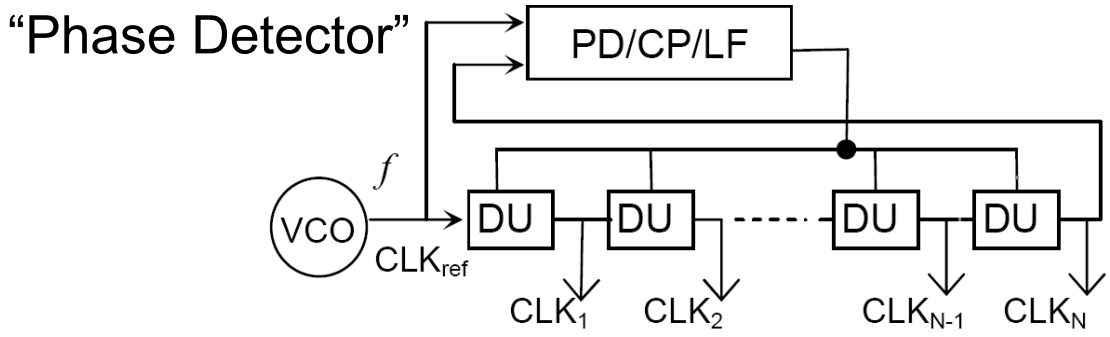



Example applications:

- Multi-phase harmonic rejection mixers (sofware radio)
- Fast Time-interleave A/D Converters
- High-speed serial datacommunication links

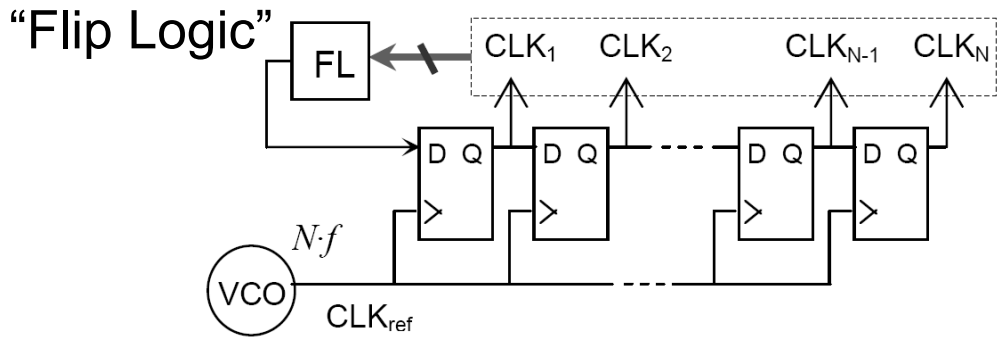
# How Create Multi-phase Clocks?

- Delay Locked Loop




**Controlled Delay Units (DU)**

- Shift Register acting as Divider:

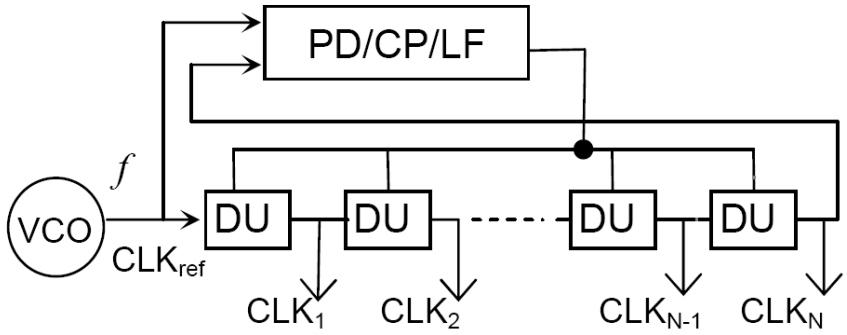



**Clocked D-FlipFlops (DFF)**

Which has better performance (in $FoM_{abs.Jitter}$)?

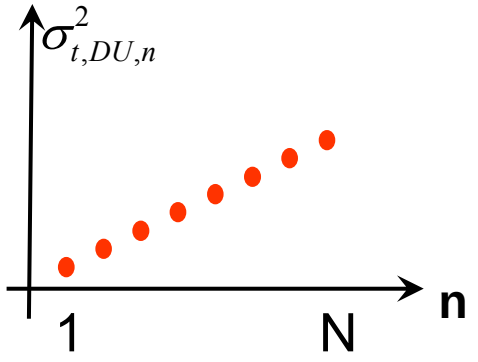
# DLL Output Jitter

- **Jitter Sources (thermal noise)**
  - **Voltage Controlled Oscillator (VCO)**
  - **Delay Units**
  - **Phase control loop**




- **DLL output jitter is lowest for low bandwidth**
  - **Control loop jitter negligible, VCO and DU jitter almost un-controlled**
  - **(Independent) jitter contributions of cascaded DUs accumulate:**

$$\sigma^2_{t,DU,n} = n\sigma^2_{t,DU}$$

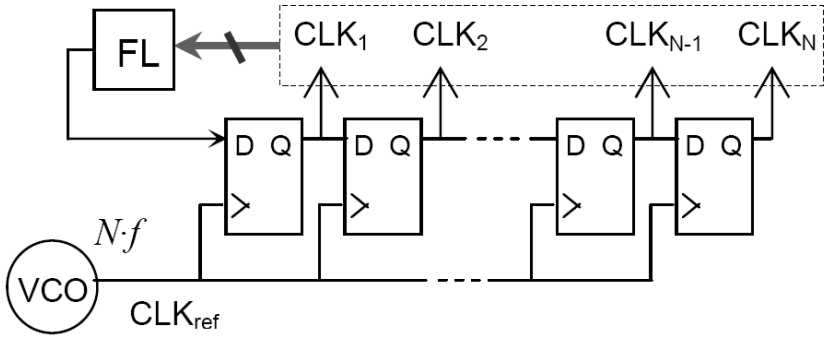



  - **Average jitter variance (all phases contribute errors):**

$$\sigma^2_{t,avgN,DLL} = \frac{\sum_{n=1}^{N} \sigma^2_{t,DU,n}}{N} = \frac{1+N}{2}\sigma^2_{t,DU}$$

# Shift Register (SR) Output Jitter

- Jitter Sources
  - VCO
  - D-flipflop chain
  - Flip Logic doesn't add jitter

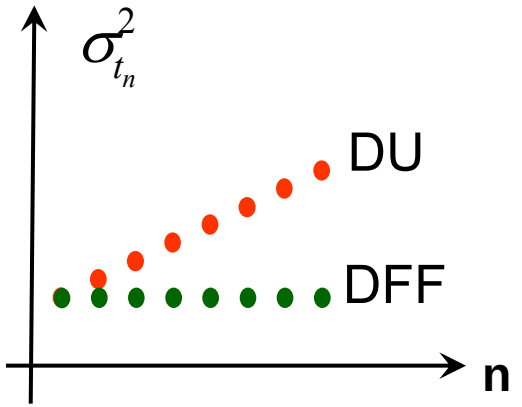



- SR is an open-loop system for jitter
  - VCO and DFF chain jitter un-controlled

- No jitter accumulation between DFFs (simply select & pass one $CLK_{ref}$ edge)

$$\sigma^2_{t,DFF,n} = \sigma^2_{t,DFF}$$

$$\sigma^2_{t,DFF,avgN} = \sigma^2_{t,DFF}$$



# Compare VCO Phase Noise/Jitter

VCO Performance evaluated via FOM:

$$\mathrm{FoM_{osc}} = 10\log(\mathrm{L}(\mathrm{f_m})) + 10\log\left(\frac{\mathrm{f_m^2}}{\mathrm{f_{OSC}^2}}\frac{\mathrm{P_{DC}}}{1\mathrm{mW}}\right)$$

- At DLL output:

$$\mathcal{L}_{\mathrm{DLL}}(\mathrm{f_m}) = \frac{10^{\mathrm{FoM_{osc}}/10}}{\mathrm{P_{DC}}/1\mathrm{mW}} \cdot \frac{\mathrm{f_{OSC}^2}}{\mathrm{f_m^2}}$$

- At SR (divide-by-N) output

$$\mathcal{L}_{\mathrm{SR}}(\mathrm{f_m}) = \frac{10^{\mathrm{FoM_{osc}}/10}}{\mathrm{P_{DC}}/1\mathrm{mW}} \cdot \frac{(\mathrm{N}\cdot\mathrm{f_{OSC}})^2}{\mathrm{f_m^2}} \times \frac{1}{\mathrm{N^2}} = \mathcal{L}_{DLL}(f_m)$$

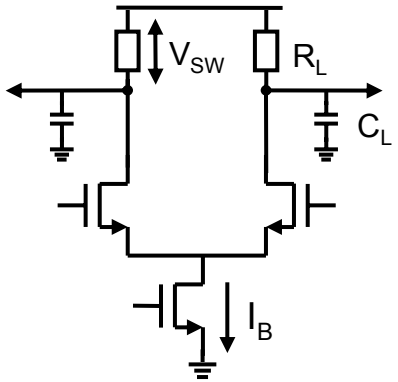
For same VCO FOM and power: same transferred phase noise (jitter)

- LC VCO: inductor Q higher and area smaller at high $f_{OSC}$
- Shift Register also more flexible and “more digital”

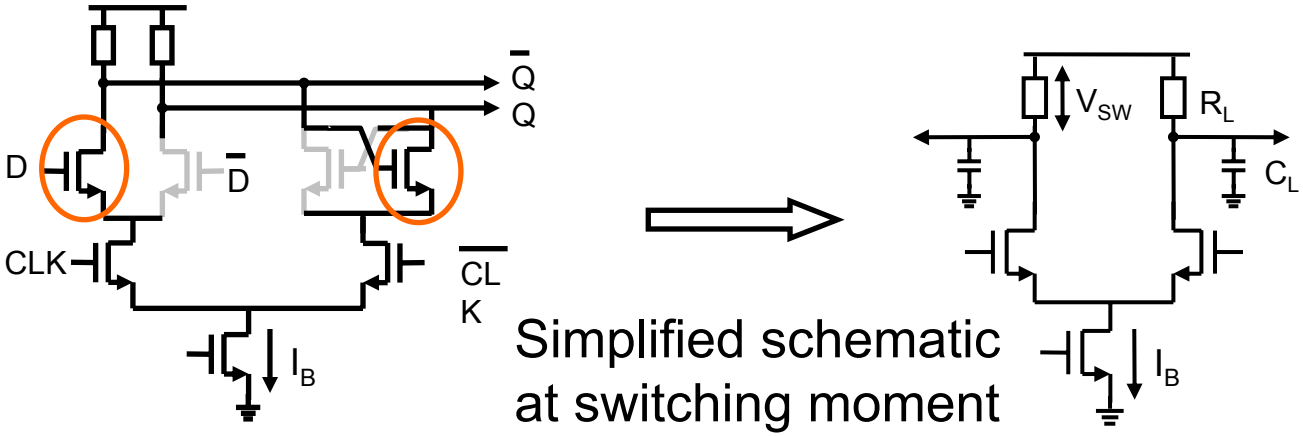
# Compare Generated Jitter

- Assume Current Mode Logic (CML) circuits
  - Good supply noise rejection
  - Low generation of delta-I noise
- CML delay unit

$$t_d \approx \ln 2 \cdot R_L C_L = \ln 2 \cdot \frac{V_{SW}}{I_B} C_L$$




- CML DFF part determining jitter:



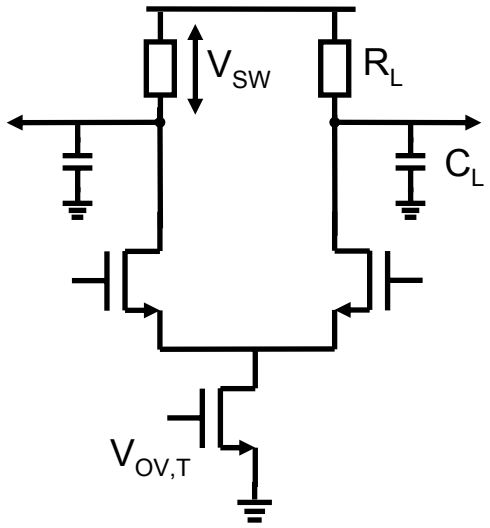

Simplified schematic at switching moment

# DU Noise Jitter Analysis

- Delay unit jitter due to thermal noise

$$\sigma_t^2 = \{2(1+\gamma+\gamma_T \frac{\alpha \cdot V_{SW}}{2V_{OV,T}})\} \times \frac{\kappa T/C_L}{(I_B/C_L)^2}$$

[Levantino,JSSC05]




- Tradeoff jitter ⇔ power

- FoM based on admittance scaling:

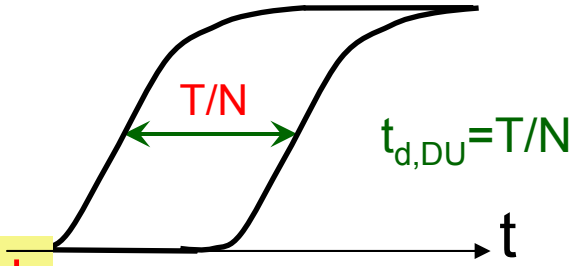
$$\sigma_t^2 \cdot P_{dis} = \{(1+\gamma+\gamma_T \frac{\alpha \cdot V_{SW}}{2V_{OV,T}}) \frac{2\kappa T}{\ln 2 V_{SW}}\} \times \frac{t_d}{I_B} \times \frac{V_{DD} I_B}{1mW} \approx c \times t_d$$

Power efficient low jitter: Minimize $t_d$!!

# DU and Latch Delay

- DLL based:

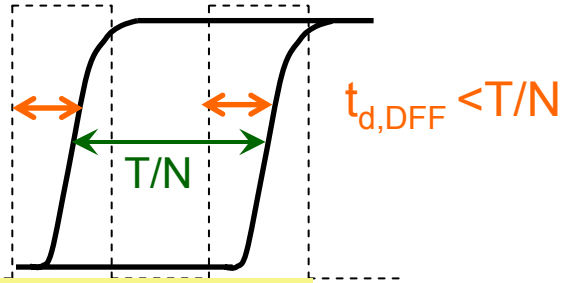
$$t_{d,DU} = \frac{T}{N} = \frac{1}{N \cdot f}$$




Delay is functionally fixed to T/N

- SR based:

$$t_{d,DFF} + t_{su} < \frac{T}{N}$$




Delay can be small reducing jitter!!

Conclusions:
- Choose Shift Register and keep latch delay small
- Similar conclusion for threshold voltage-mismatch
- Benefit strongest at low clock frequency

[1] Gao, TCASII08

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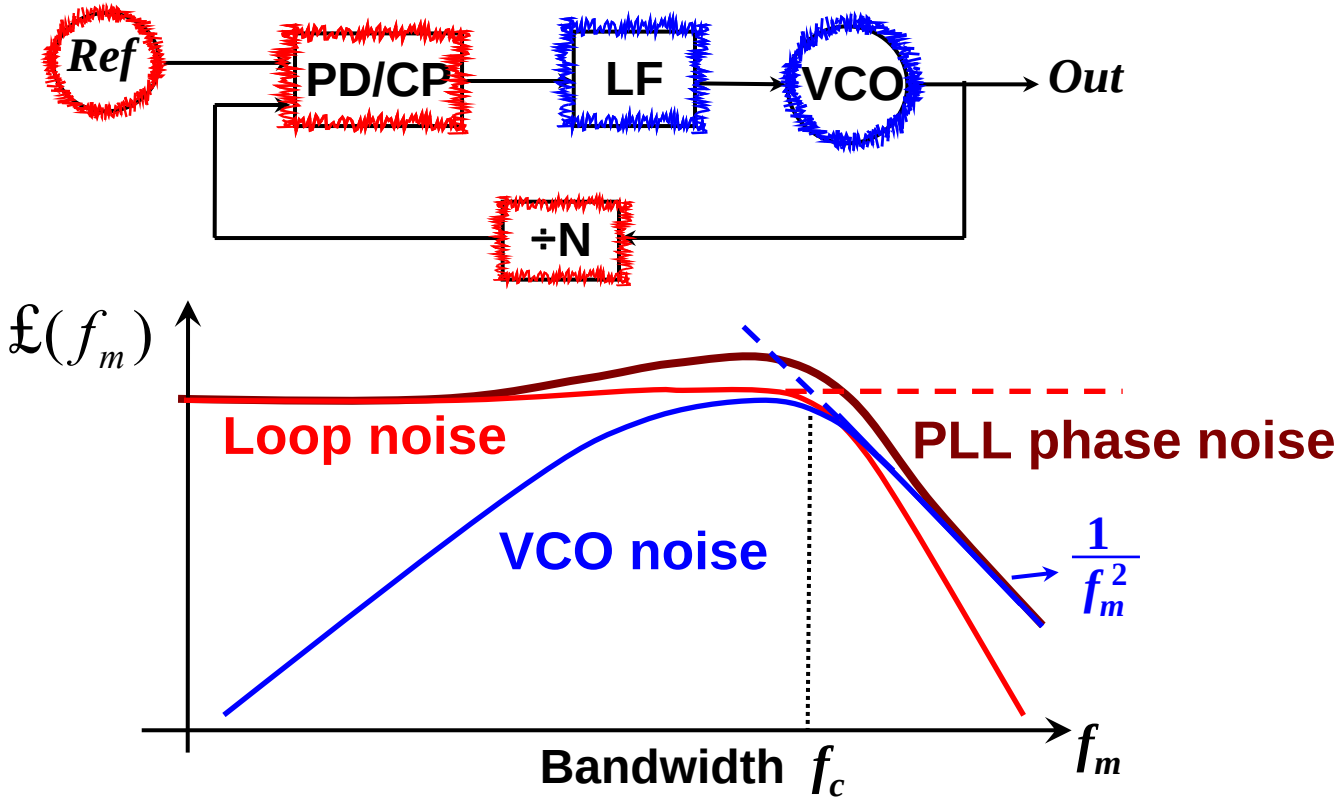
# Classical PLL Noise




- Loop noise multiplied by N, dominates in-band
- In optimized PLL, Loop and VCO noise contribute equal jitter[1]
  - We ignore 1/f noise as its contribution to jitter is usually negligible
  - Relating long term absolute jitter with phase noise

[1] Vaucher, Kluwer02

# PLL Benchmarking FOM

- **Proposed PLL benchmark Figure-of-Merit [1]**

$$FOM_{PLL} = 10\log[(\frac{\sigma_{t,PLL}}{1s})^2 \cdot \frac{P_{PLL}}{1mW}]$$

- **To optimize $FoM_{PLL}$ for a classical PLL:**
  - **Loop and VCO have equal jitter contribution (optimum bandwidth)**
  - **Design quality of Loop and VCO is equally important**

$$FOM_{PLL} \propto FOM_{loop} + FOM_{VCO}$$

  - **Loop and VCO have equal power consumption**

- $f_{out}$ and $f_{ref}$ do not affect $FoM_{PLL}$ for optimized case assuming:
  - Long-term absolute jitter
  - Only dynamic loop power dissipation
  - No significant flicker noise
  - Divider power proportional to $f_{ref}$
  - Steep enough Reference clock

[1] Gao, TCASII09

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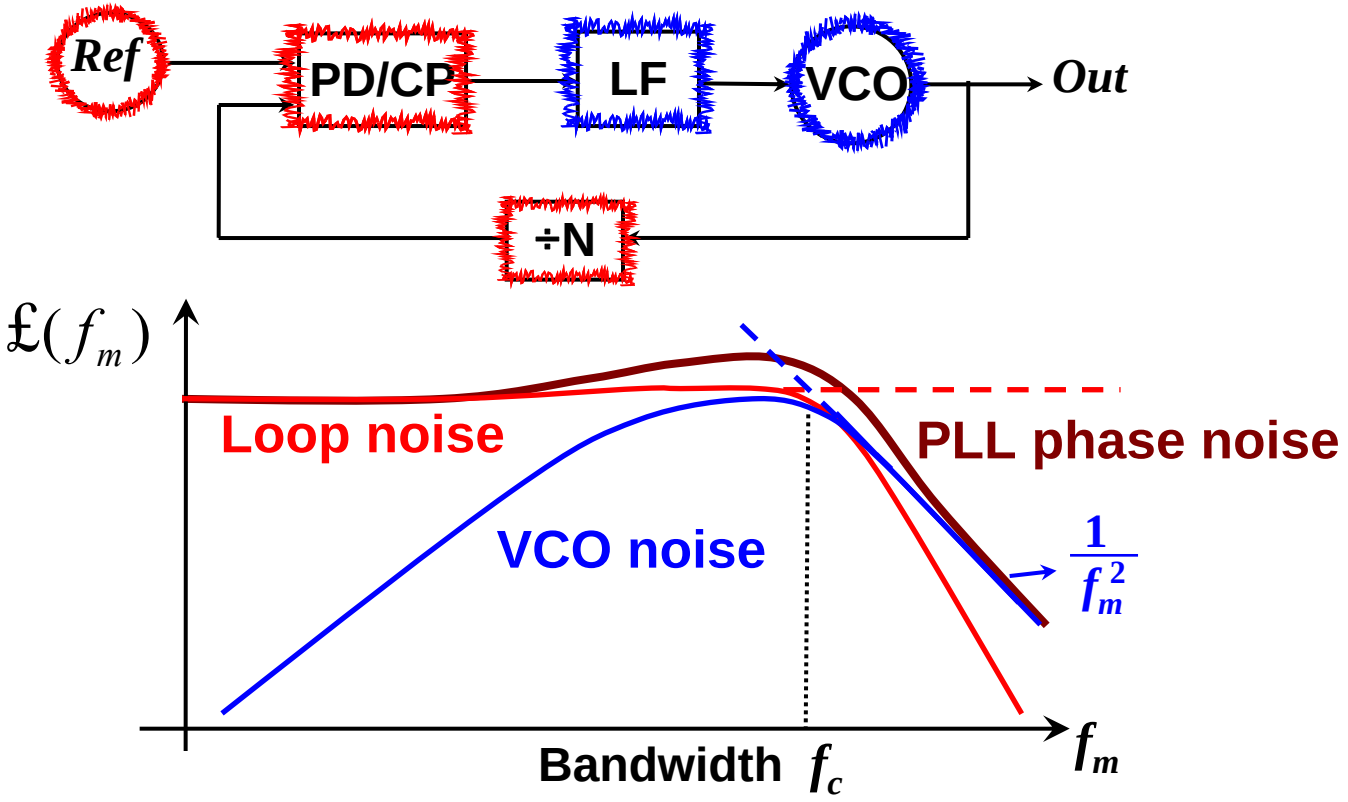
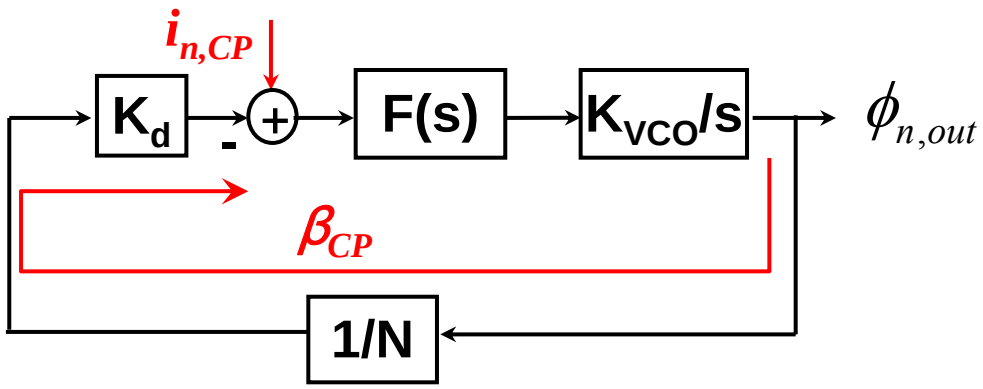



- Loop noise multiplied by N, dominates in-band
- In optimized PLL, Loop and VCO noise contributes equally

**This work focuses on reducing loop noise**

# Noise from CP referred to Output

- Main loop noise sources: usually CP and divider



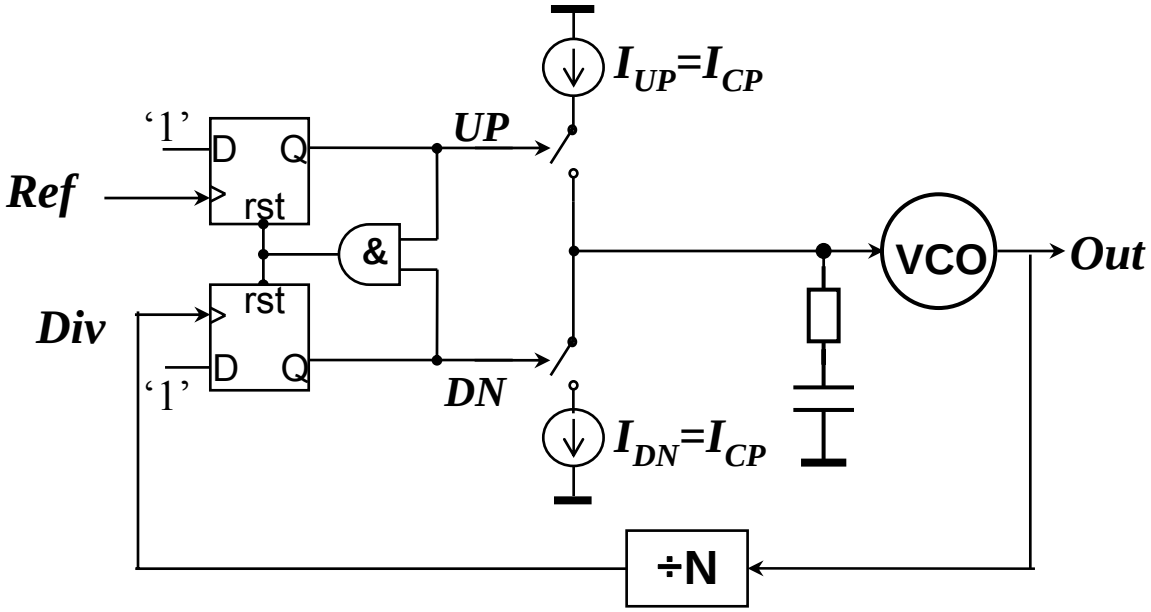

- Define a CP feedback gain: $\beta_{CP} = \frac{1}{N} \times K_d$

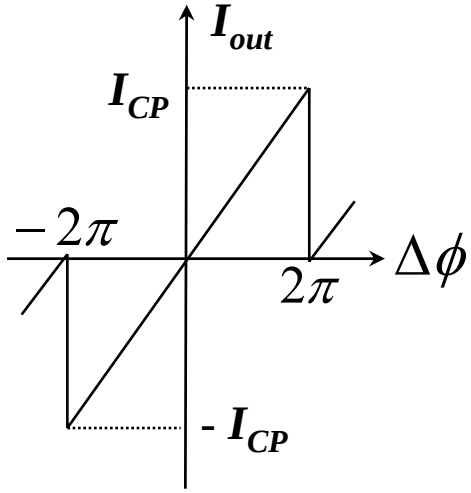
- Inside bandwidth, loop gain is big:

$$\phi_{n,out} \approx \frac{i_{n,CP}}{\beta_{CP}}$$

**CP noise suppressed by $\beta_{CP}$ , large $\beta_{CP}$ desired**

# Classical 3-state PFD/CP

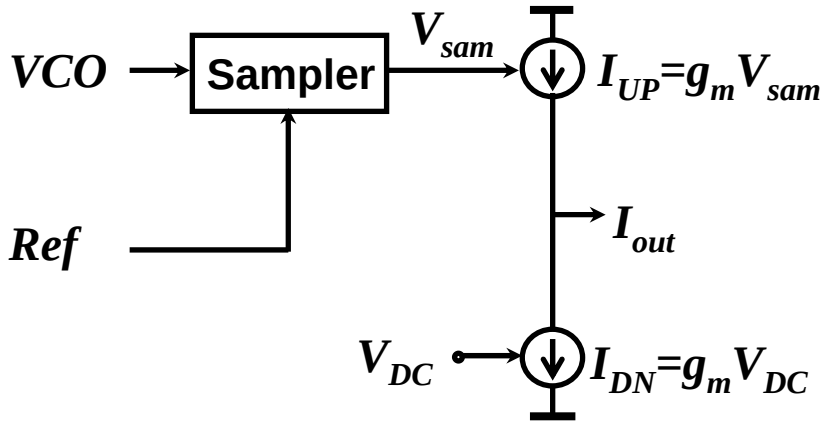


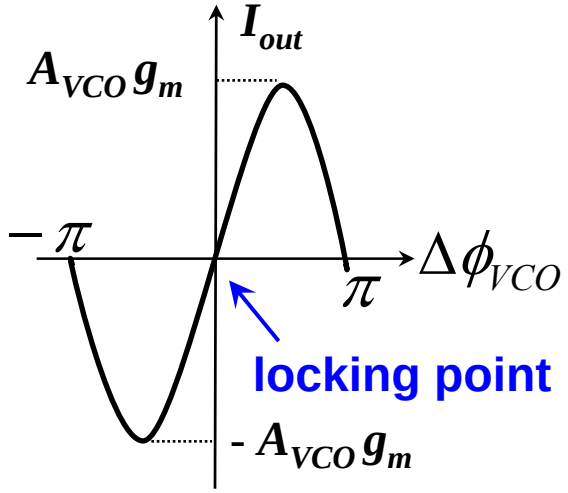




- **CP Feedback Gain** $\beta_{CP,3state} = \frac{1}{N} \times \frac{I_{CP}}{2\pi}$

**Can we get rid of N ?**

# Sub-Sampling PD/CP (SSPD/CP)




- Voltage controlled CP
- Ideal characteristic

- Detection is fairly linear once in lock

$$\beta_{CP} = K_d = \frac{\Delta I_{out}}{\Delta \phi_{out}} = \frac{g_m \cdot A_{VCO} \sin(\Delta \phi_{VCO})}{\Delta \phi_{VCO}} \approx g_m A_{VCO}$$

**Yes, we can get rid of N!**

# SSPLL *VS* Classical PLL

- **Divider noise**

**SSPLL can work without divider**

- **CP noise**

$$\frac{\beta_{CP,SSPD}}{\beta_{CP,3state}} = 4\pi \cdot N \cdot \frac{A_{VCO}}{2I_{CP}/g_m} = \boxed{4\pi \cdot N} \cdot \boxed{\frac{A_{VCO}}{V_{gs,eff}}} \quad >>1$$

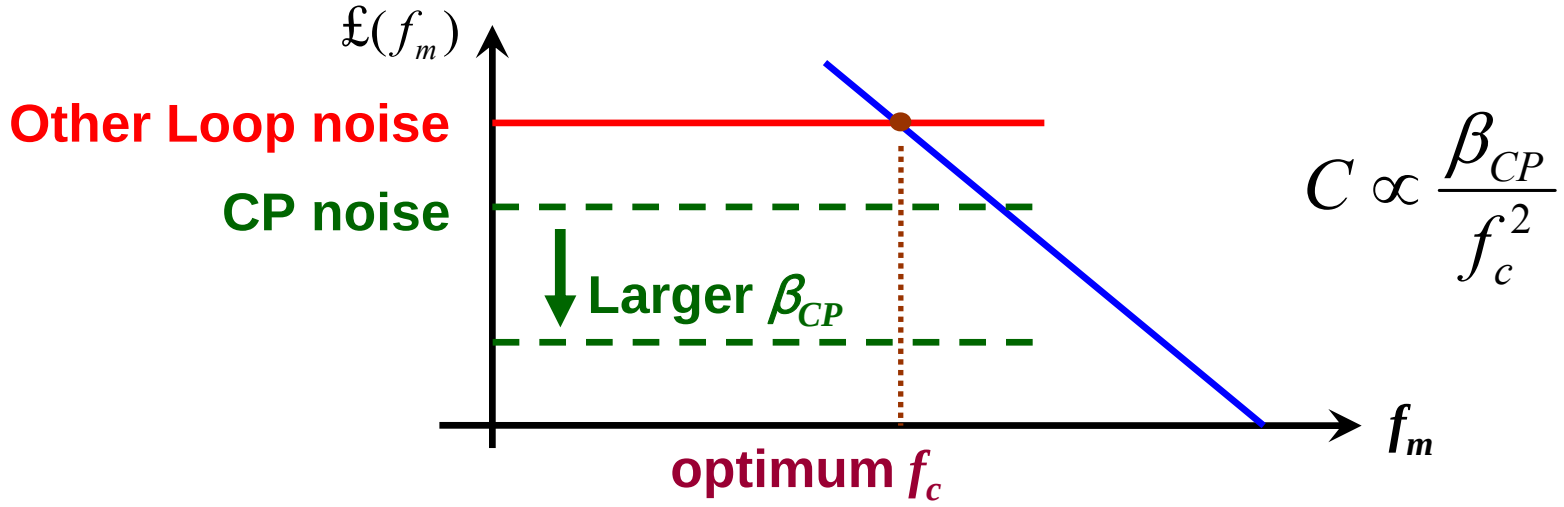
$>>1$ $>1$

**SSPLL has much larger $\beta_{CP}$ to suppress CP noise!**

**e.g. N=50, $A_{VCO}$=0.4V, $V_{gs,eff}$=0.2: 1000x bigger**

# $\beta_{CP}$ and Filter Cap

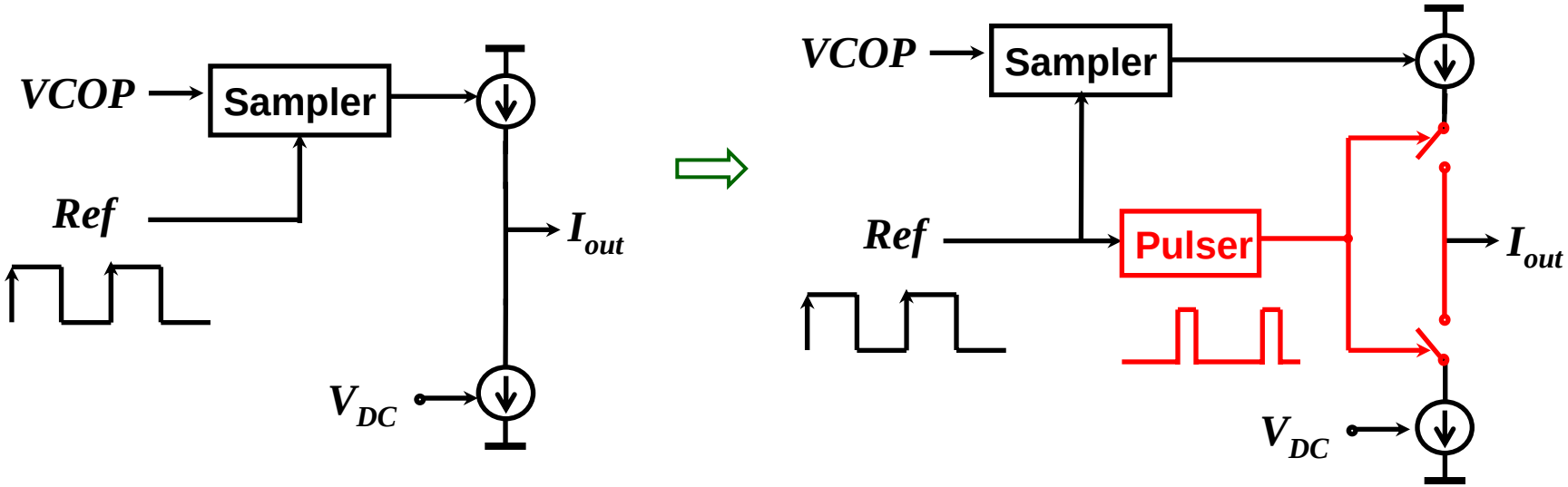
- In SSPLL, CP noise becomes negligible




**Even larger $\beta_{CP}$ hardly affects overall loop noise and $f_c$ but requires bigger C to stabilize the loop**

**Some way of $\beta_{CP}$ control is desired**

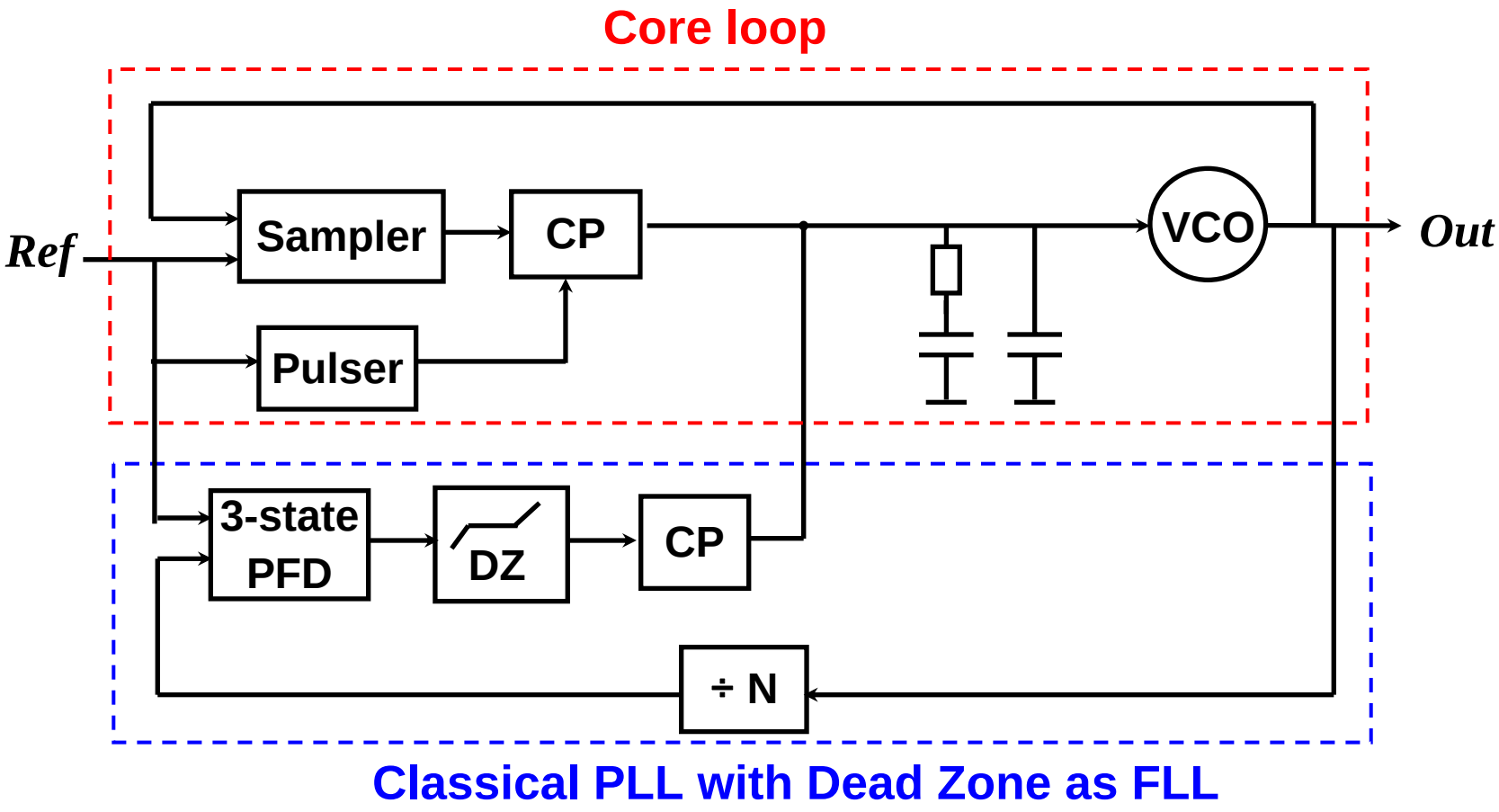
# SSPD/CP with Gain Control




$$\beta_{CP} = A_{VCO} \cdot g_m \cdot DR_{pul}$$

**A proper choice of $DR_{pul}$ reduces Cap area while still making CP noise negligible**

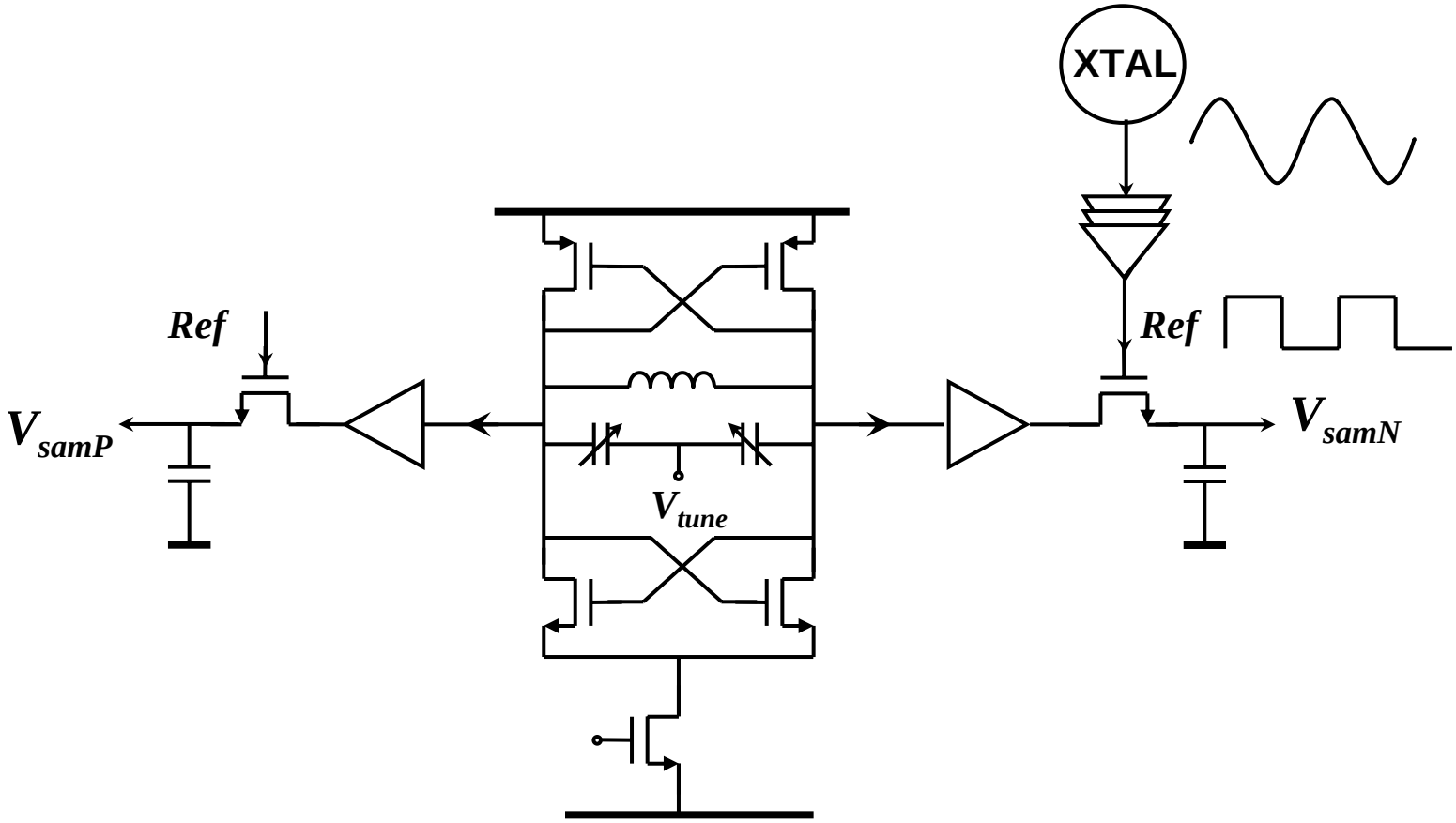
# Proposed SSPLL Architecture




1. During locking, ΔΦ > DZ, FLL has large gain, brings loop to lock

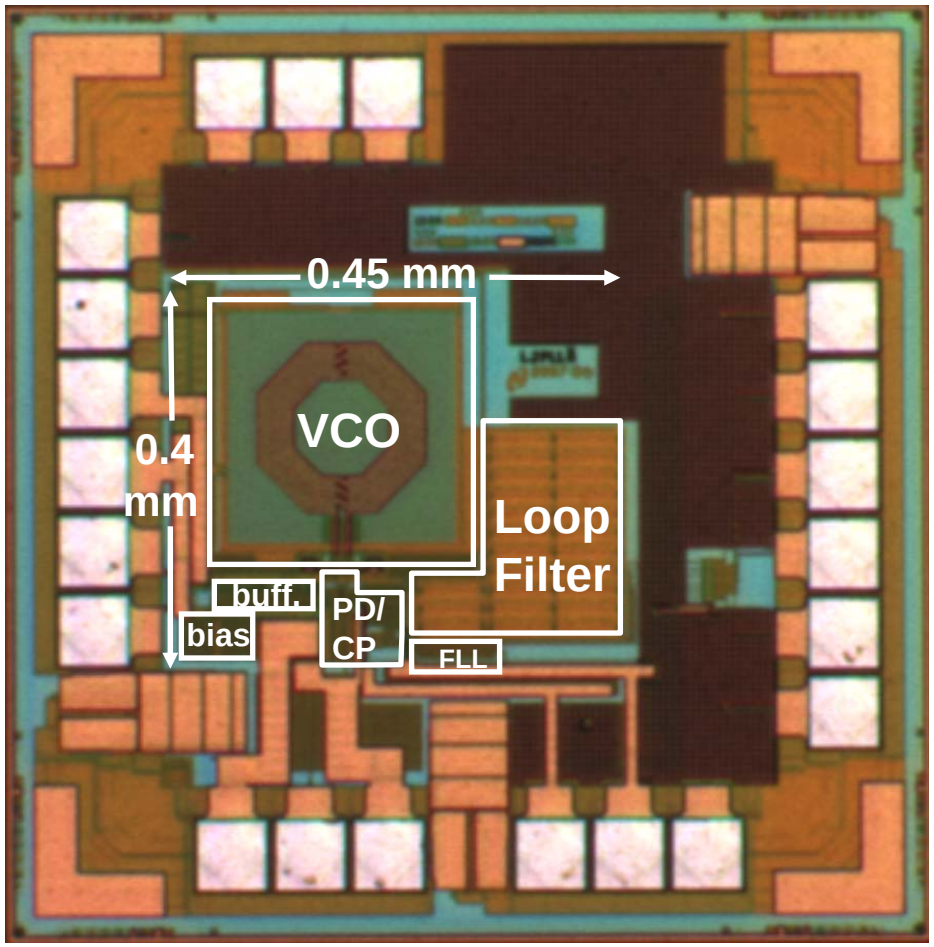
2. Close to locking, ΔΦ < DZ, FLL has zero gain, not injecting noise

# VCO & Sampler Design




**Differential sampling doesn't need $V_{DC}$, cancels clock feed-through and charge injection**

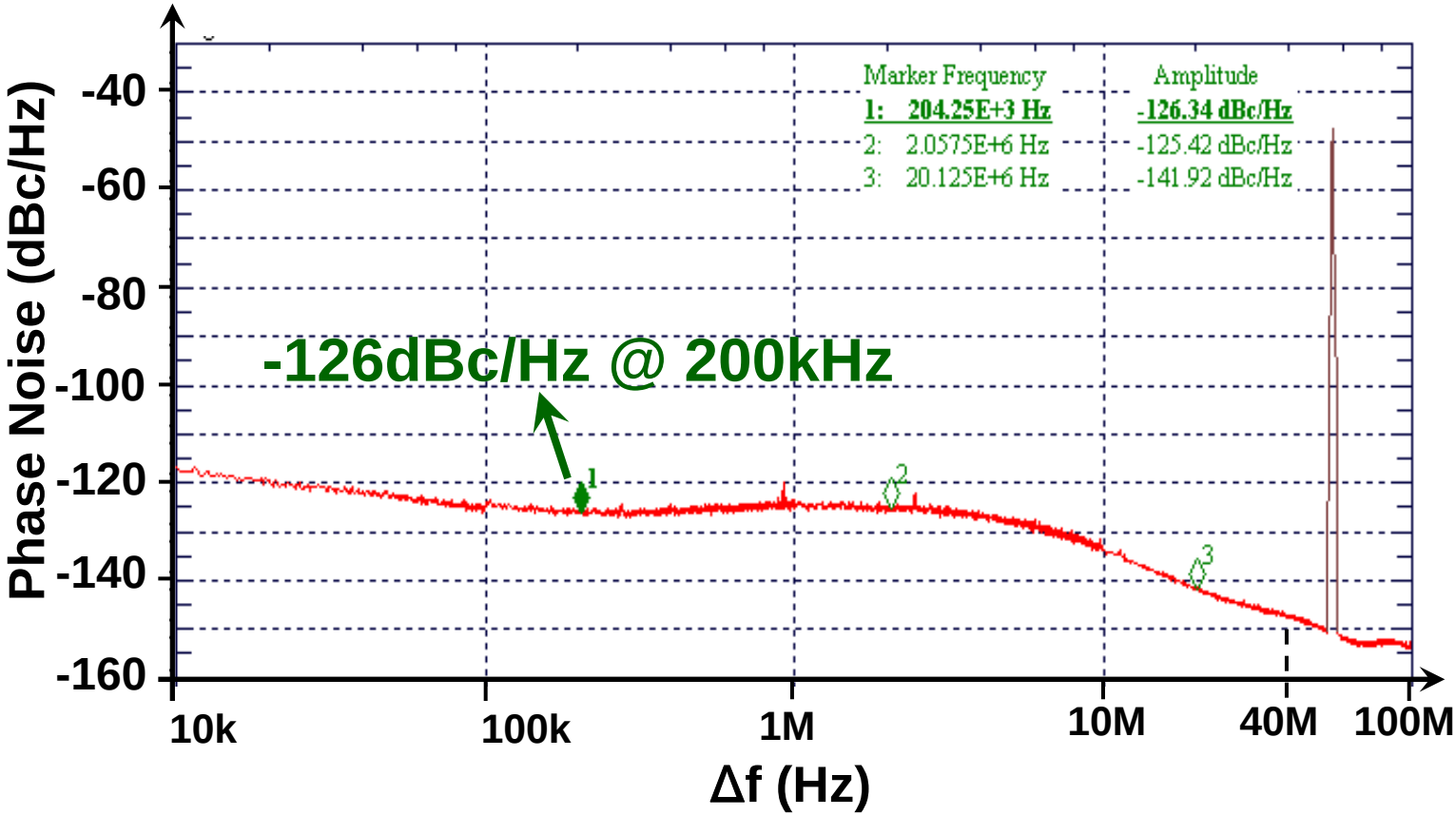
# Die Photograph




- 0.18um CMOS
- 24-pin LLP package
- Active Area: 0.18mm$^2$
- VDD: 1.8V
- Power Consumption
  - VCO 1mA
  - Core Loop 3.2mA
  - FLL 0.8mA (disabled after locking)

[Gao,ISSCC09]

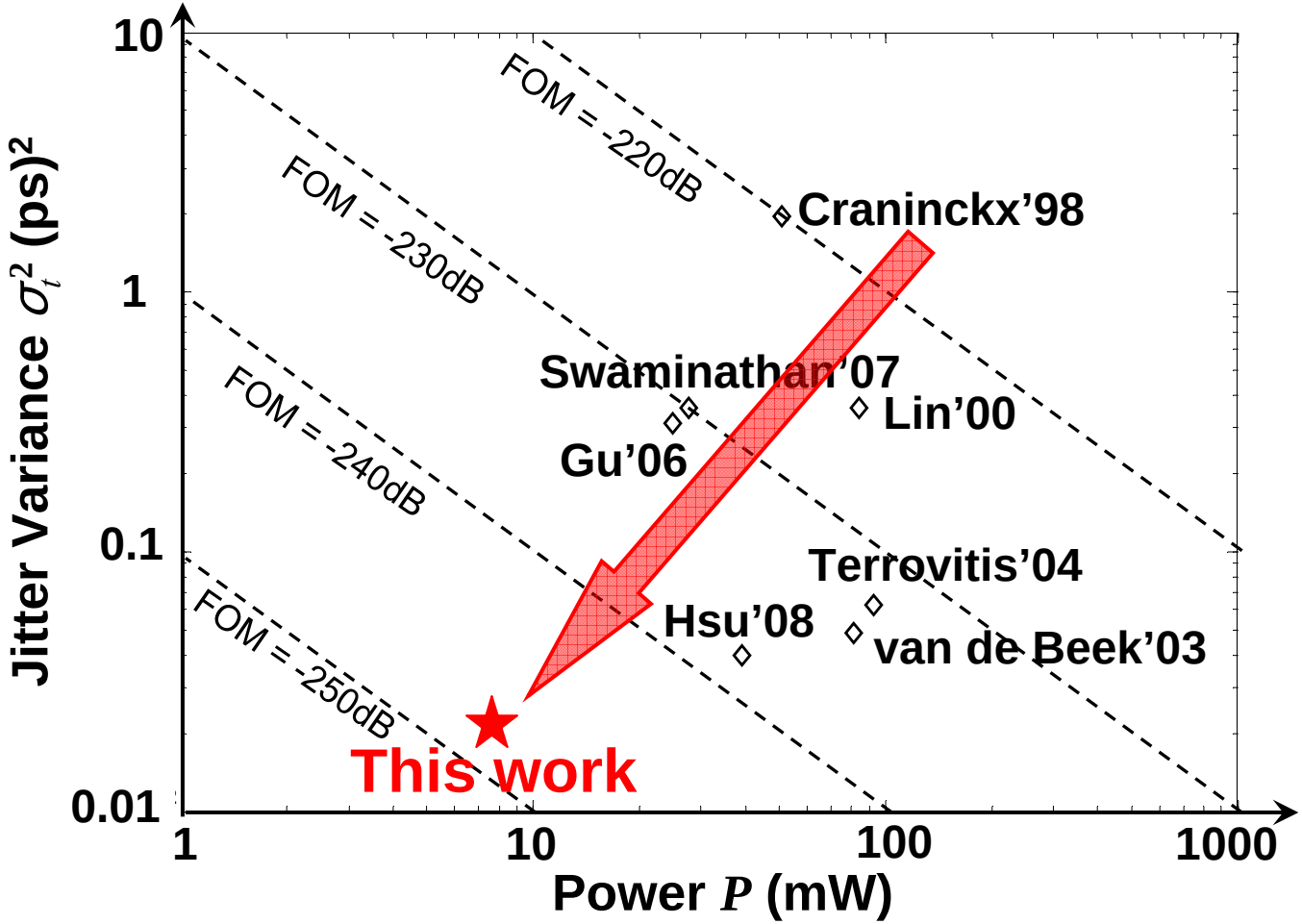
# Measured Phase Noise




**In-band Phase Noise: -126dBc/Hz @ 200kHz**

**Integrated Jitter [10k, 40M]: 0.15ps**

# ISSCC Low Jitter PLL Comparison




**This work improves FOM by 9.5dB, normalized to same jitter, it consumes ~10x less power**

# Conclusions

- Admittance level scaling: n x SNR at cost of n x $P_{dis}$
  ⇔ FoM should normalize for admittance scaling
- Useful FoMs for phase noise and jitter (low⇔ good):

$$\mathrm{FoM}_{osc} = £(f_m)\left(\frac{f_m}{f_{osc}}\right)^2 \frac{P}{1\,\mathrm{mW}}$$

$$\mathrm{FoM}_{abs.jitter} = \sigma_t^2 \cdot P$$

$$\mathrm{FoM}_{PLL} = 20\log\frac{\sigma_t}{1\mathrm{s}} + 10\log\frac{P}{1\mathrm{mW}}$$

- Designs stimulated by FoM Definitions:
  - Relaxation oscillator with $FoM_{osc}$ similar to Ring Oscillators
  - Smaller delay ⇔ better $FoM_{abs.jitter}$ ⇔ SR better then DLL
  - Sub-Sampling PLL with 10x better $FoM_{PLL}$

# Literature


[Vaucher,Kluwer02] C. S. Vaucher, Architectures for RF Frequency Synthesizers, Kluwer, 2002

[Levantino,JSSC05] S. Levantino, et al., “Phase noise in digital frequency dividers”, IEEE J. Solid-State Circuits, vol. 39, no.5, pp. 775 – 784, May 2004.

[Klumperink,JSSC04] E. A. M. Klumperink, S. M. Louwsma, G. J. M. Wienk, and B. Nauta, "A CMOS switched transconductor mixer," Solid-State Circuits, IEEE Journal of, vol. 39, pp. 1231-1240, 2004.

[Navid, JSSC05] R. Navid, T. H. Lee, R. W. Dutton, “Minimum Achievable Phase Noise of RC Oscillators,” IEEE J. Solid-State Circuits, Mar. 2005, pp. 630-637.

[Shrestha,JSSC06] E. Mensink, E. A. M. Klumperink, and B. Nauta, "Distortion cancellation by polyphase multipath circuits," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 52, pp. 1785-1794, 2005.

[Klumperink,ComMag07] E.A.M. Klumperink, R. Shrestha, E. Mensink, V.J. Arkesteijn, B. Nauta, “Cognitive radios for dynamic spectrum access - polyphase multipath radio circuits for dynamic spectrum access”, IEEE Communications Magazine, Volume 45, Issue 5, May 2007 pp. 104 – 112.

[Geraedts, ISSCC08] Geraedts, P.F.J., Tuijl, A.J.M. van , Klumperink, E.A.M., Wienk, G.J.M., Nauta, B., "A 90µW 12MHz Relaxation Oscillator with a -162dB FOM“, 2008 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, February 8-12, Digest of Technical Papers, pp. 348-349+618, 2008, ISBN 978-1-4244-2011-7.

[Gaol,TCASII08] X. Gao, E.A.M. Klumperink, B. Nauta, “Advantages of Shift Registers Over DLLs for Flexible Low Jitter Multiphase Clock Generation”, IEEE Transactions on Circuits and Systems II, vol. 55, no.3, pp. 244-248, March 2008.

[Gao, ISSCC09] Xiang Gao, Eric Klumperink, Mounir Bohsali, and Bram Nauta, “A 2.2GHz 7.6mW Sub-Sampling PLL with -126dBc/Hz In-band Phase Noise and 0.15psrms Jitter in 0.18µm CMOS”, ISSCC, Feb. 2009.

[Gao,TCASII09] Gao, X., Klumperink, E.A.M., Geraedts, P.F.J., Nauta, B., "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops“, IEEE Transactions on Circuits and Systems II, vol. 56, no.2, pp. 117 -121, Feb. 2009.