

linear combinations of two or more signals. One possible circuit realisation uses degenerated differential pairs to convert the input voltages to currents. The advantage of this approach is that it accepts differential voltages and generates differential currents which can then be easily combined to create the required combinations. Extra DC current sources optionally connected to the current summing nodes can control the DC components of the error currents. This reduces the operating-voltage requirement by decreasing the direct-voltage drops across the feedback resistors in Fig. 2b.

To obtain the comparison results from the decoder, mirror transistors are employed to replicate the currents of the differential cell transistors. These output currents are used to update the path memory.

Finally, it should be mentioned here that although BJTs have been used in this circuit description, to reduce the cost, a full CMOS realisation is also possible by careful circuit design.

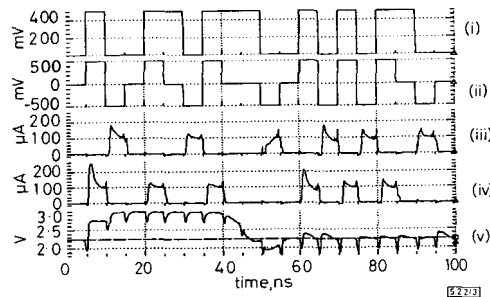


Fig. 3 Typical dicode-Viterbi decoder waveforms, based on SPICE simulation

- (i) Original data
  - (ii) Encoded data
  - (iii) Output current I
  - (iv) Output current II
  - (v) Common-mode voltage
- reference level

**Simulation results:** Using 0.8μm BiCMOS process parameters, a simple two-state dicode Viterbi detector was designed and simulated. Although this special case can be efficiently decoded through a simplified algorithm [4], the approach introduced in this Letter was followed to prove the concept. Ping-pong S/Hs with source-follower buffers were employed, and the CMFB circuit was operating on the DC-level shiftings introduced by these buffers. Low-impedance nodes, described in Fig. 2a, were provided by emitter followers. Degenerated differential pairs were used to produce the error current signals. Fig. 3 shows the SPICE-simulation results. The original as well as the encoded data are shown along with the mirrored currents of the differential cell transistors as the comparison results. It can easily be verified that ideal versions of these signals result by applying the nodal equations to the encoded signal. The memory management of the decoder is beyond the scope of this Letter and can be shown to translate the comparison results to the original uncoded data. Also shown in Fig. 3 is the common-mode voltage of the state metrics which settles to the desired value as soon as the start-up transition has been completed.

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M. H. Shakiba, D. A. Johns and K. W. Martin (Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario M5S 1A4, Canada)

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#### Comment

#### Low-voltage CMOS transconductance cell based on parallel operation of triode and saturation transconductors

E.A.M. Klumperink, C.H.J. Mensink and P.M. Stroet

Indexing terms: CMOS integrated circuits, Transconductors

**Introduction:** Recently a new linearity improvement technique for low voltage CMOS transconductors was proposed [1]. The technique is based on the parallel operation of a triode and saturation transconductor. According to the simple square-law MOST model extended with the 'θ-model' for mobility reduction,

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} \quad (1)$$

These transconductors have third order distortion terms with opposite sign, enabling third order nonlinearity cancellation. As analysed in [1], the cancellation occurs when the aspect ratios of the triode and saturation converter are chosen according to

$$\frac{(W/L)_{tri}}{(W/L)_{sat}} \approx \frac{1}{2 \cdot \theta \cdot V_{DS}} \quad (2)$$

The proposed linearisation technique was evaluated using PSPICE simulations and it was found that a THD of -87dB was possible at 800mV peak-to-peak input voltage for a supply voltage as low as 1.5V. In this Letter we want to comment on the significance of these simulation results. Two aspects are discussed: first the model used for distortion prediction and secondly the effect of device mismatch. Measurement results will be presented which indicate that the third order distortion terms of a saturation and triode converter do not have an opposite sign for a low supply voltage as predicted by simulations. As a result the newly proposed linearisation technique will most probably not work in that case. Furthermore inevitable device mismatch easily introduces non-negligible second order distortion which limits the achievable THD.

**Comment on model used for distortion prediction:** In [1], the distortion of a circuit embodying the newly proposed linearisation technique was evaluated by means of PSPICE simulations. Because θ values are mentioned in [1], presumably the level 3 model [2] was used, which uses eqn. 1 for mobility reduction modelling (level 4 BSIM [3] mobility modelling is similar though uses different nomenclature). The third order distortion that is found in this way is mainly determined by the third order derivative  $d^3I_D/dV_{GS}^3$  of the level 3 MOS transistor model (at constant  $V_{DS}$  and  $V_{SB}$ ). As discussed in [4], CAD models sometimes even fail to predict the first order derivative of the current of an MOS transistor with adequate accuracy, therefore placing distortion simulations that rely on higher order derivatives under great suspicion. This is especially true for low distortion levels and for circuits in which a nonlinearity cancellation occurs. In the latter case the final result even depends on the difference of the value of the third order

derivatives instead on the value itself. For the above reasons it seems indispensable to perform measurements for a fair evaluation of low distortion circuits.

The derivative  $d^3I_D/dV_{GS}^3$  as predicted by the PSPICE level 3 model, shows an abrupt change of sign at the transition of the triode region to the saturation region. Measurement results indicate that a rather sharp transition between the triode and saturation region does indeed occur [5, 6]. At this transition the third order derivatives becomes zero [Note 1]. To find the biasing dependence of this transition point we performed third order derivative measurements. A third order intermodulation product at 500Hz was detected with a measurement setup similar to that described in [7] (the excitation frequencies used were 100kHz, 110kHz and 209.5kHz). The biasing points for which the third order distortion becomes zero were determined. The measurements results for a 50/10 nMOS transistor fabricated in a 2.5µm CMOS process are given in Fig. 1. Also given in the Figure is the transition point as obtained from level 3 PSPICE simulations (most important parameters:  $V_{TO} = 0.75V$ ,  $KP = 70\mu A/V^2$ ,  $THETA = 0.05V^{-1}$ ). Fig. 1 shows that both lines roughly linearly depend on  $V_{DS}$  as might be expected, because the drain-source saturation voltage linearly depends on  $V_{GS}$ . However, in measurements, the transition takes place at a drain-source voltage significantly smaller than in simulation (roughly 0.8V). In [6] only results are available for  $V_{DS} = 0.5V$ , yet the same trend is found (transition at  $V_{GS} \approx 2.5V$ ). Although more measurements are needed to draw final conclusions about the universality of this phenomenon, serious doubt about the significance of distortion simulations according to the  $\theta$ -model is justified.

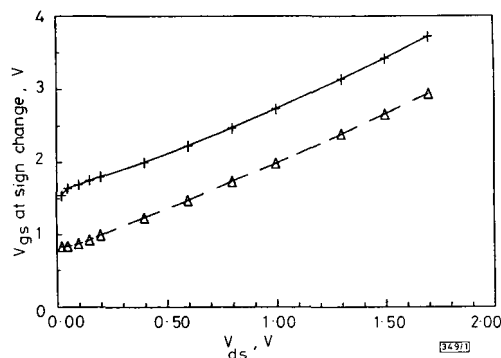


Fig. 1 Measured and simulated  $V_{GS}$  at which the third order derivative changes sign as a function of  $V_{DS}$

The measured values are significantly larger

+ measurement  
 Δ SPICE simulation

When taking the measurement results and relating these to the linearisation technique proposed in [1], it is concluded that the technique does not work for low voltages. For  $V_{DS} = 0.25V$ , the third order distortion transition point occurs at 1.9V which is higher than the supply voltage of 1.5V. This means that no third order nonlinearity cancellation takes place, but instead the third order terms add in a parallel combination of a triode and saturation transistor. Yet, for higher supply voltages, a third order distortion cancellation might still be acquired by the proposed technique.

*Comment on effect of mismatch on THD:* In [1] it is stated that mobility reduction is the main source of nonlinearity. In our experience this is indeed true for many moderate linearity transistor designs, but most probably not for a transistor with a THD of -87dB. Transistors usually have a balanced circuit topology in which even order distortion products are cancelled for nominal component values. However, because of random mismatch the cancellation will not be perfect and second order harmonic distortion HD2 will occur. Compared to a single-ended

circuit, HD2 will decrease by a factor that depends on the matching of the circuit halves of the balanced converter. Typically an improvement factor between 10 and 100 is found. For a single-ended transistor modelled by the ' $\theta$ -model' and the parameters used in [1] ( $\theta = 0.1V^{-1}$ , single ended amplitude 0.2V,  $V_{GS} - V_T = 0.45V$ ) an HD2 of 1% is found for the triode converter and 11% for a saturation transistor (HD2 is proportional to  $V_{in}$ ). Consequently, after balancing, an HD2 in the range -40dB to -80dB is expected. Thus it is concluded that in general, mismatch effects cannot be disregarded for high linearity transistors. It is therefore not sufficient to carry out simulations with nominal values as done in [1].

Fortunately, the second order distortion terms of a triode and saturation converter also have opposite sign according to the ' $\theta$ -model' and even cancel each other for  $V_{DS} \approx 0.25V$  if the condition of eqn. 2 is met in the circuit proposed in [1]. However, this cancellation depends on  $V_{DS}$ . Moreover again the validity of the ' $\theta$ -model' distortion prediction is questionable and measurements seem indispensable.

*Conclusions:* Measurements indicate that simulations based on the ' $\theta$ -model' (e.g. SPICE level 3 and BSIM model) incorrectly predict the sign of the third order derivative of a triode transistor for  $V_{DS}$  ranging from the saturation voltage to roughly 0.8V below (50/10 nMOST fabricated in a 2.5µm CMOS process). As a consequence the linearisation technique proposed in [1] will most probably not work for low voltages as was claimed. Moreover, in general, it is argued that low distortion predictions based on simulations should be looked on with great suspicion, and that measurement results would seem indispensable. Furthermore, the taking into account of device mismatch is crucial for low distortion circuits. Nevertheless the basic concept of the linearisation proposed in [1] remains interesting and an evaluation of the technique by means of measurements would seem useful.

Somewhat aside, it can be concluded that correct modelling of the higher order derivatives of the device characteristics is essential for accurate distortion simulations. Because usually the second order and third order distortion products are most important, at least the second and third order derivatives should be adequately modelled.

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E. A. M. Klumperink, C. H. J. Mensink and P. M. Stroet (MESA Research Institute, University of Twente, Department of Electrical Engineering, PO Box 217, 7500AE Enschede, The Netherlands)

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Note 1: As discussed in [5] this biasing point renders a low HD3, yet the optimum region is quite small