Systematic Comparison of HF CMOS Transconductors

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***Abstract*—Transconductors are commonly used as active elements in high-frequency (HF) filters, amplifiers, mixers, and oscillators. This paper reviews transconductor design by focusing on the *V-I* kernel that determines the key transconductor properties. Based on bandwidth considerations, simple *V-I* kernels with few or no internal nodes are preferred. In a systematic way, virtually all simple kernels published in literature are generated. This is done in two steps: 1) basic 3-terminal transconductors are covered and 2) then five different techniques to combine two of them in a composite *V-I* kernel. In order to compare transconductors in a fair way, a normalized signal-to-noise ratio (NSNR) is defined. The basic *V-I* kernels and the five classes of composite *V-I* kernels are then compared, leading to insight in the key mechanisms that affect NSNR. Symbolic equations are derived to estimate NSNR, while simulations with more advanced MOSFET models verify the results. The results show a strong tradeoff between NSNR and transconductance tuning range. Resistively generated MOSFETs render the best NSNR results and are robust for future technology developments.**

***Index Terms*—Figure of merit, Gm-C filter, linearization, noise, signal to noise ratio, transconductor, transconductor-C filter, tunable filter, *V-I* converter, variable gain, voltage to current converter.**

I. Introduction

TRANSCONDUCTORS are ubiquitous as active elements in high-frequency integrated circuits. They implement a voltage-to-current conversion or transconductance Gm. Often this transconductance is electronically tunable. Fig. 1 shows some examples of circuits exploiting a transconductor combined with passive components. Examples are well-known, *Gm-C* filters [1] and Gm-R variable gain amplifiers [2], but also Gm-*LC* filters, gyrators, negative resistance networks, controllable delay elements, and active mixers. Actually, in high-frequency circuits, most of the transistors are functionally best considered as transconductors.

In some applications variations of the transconductance value over process and temperature are acceptable. If this is not the case, compensation for such variations is possible via transconductance tuning. Practical transconductors typically allow for tuning Gm over 10 % to 50%, enough to maintain an accurate transfer function over IC production tolerances and temperature changes [1]. Furthermore, tuning allows circuits to adapt their transfer to changing environmental conditions (e.g., AGC amplifier or adaptive filter for a variable communication channel).

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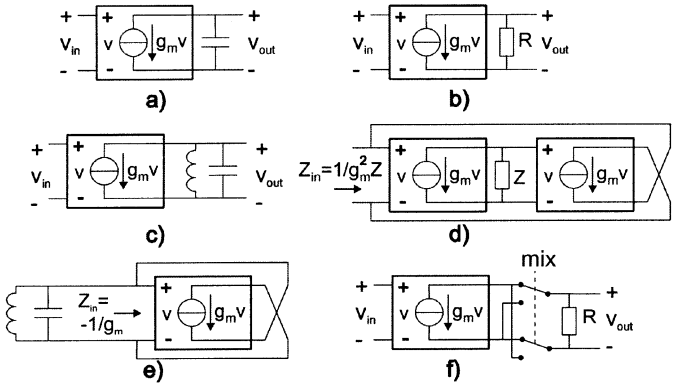

Fig. 1. Transconductor application examples at high frequencies: a) *Gm-C* integrator for filters or delay elements; b) Gm-R wideband (variable-gain) amplifier; c) Gm-*LC* filter; d) Gyrator; e) *LC* oscillator with negative resistance; f) active mixer with Gm and switches.

In such cases larger control ranges are wanted, e.g., 1 : 3 or even more then 1 : 100 [3].

One might wonder why transconductors are ubiquitous at high frequencies. Perhaps the key reason is simply that a MOS transistor operating in saturation already behaves very much like a transconductor up to very high frequencies. Many commonly used MOS circuit simulation models even do not model an upper-frequency limit in the intrinsic conversion from gate-source voltage to drain current (eliminating the gate-drain capacitance). Only by taking into account gate-resistance effects or non quasistatic effects [4], a high-frequency limit is found.

Apart from good high-frequency behavior, MOS transconductors have some other favorable properties. As will be discussed extensively later in this paper, they can achieve good linearity over a large signal swing. Provided that the noise is low enough this makes high signal-to-noise ratios (SNR) possible. Furthermore, a huge range of transconductance values can be realized on chip; transconductance values as low as 1 nS and high as 1 S can be implemented, exploiting different aspect ratios W/L and different bias regions of the MOS transistor. Moreover, the matching of transconductance values can be good. If due care is taken, a mismatch well below 1% is achievable, as transconductance is determined by well-controlled technological parameters like mobility, oxide thickness and transistor dimensions. Thus, transconductors have useful properties that actually can be exploited at any frequency. However, at low frequencies negative feedback circuits with virtually infinite loop-gain often outperform open-loop transconductor circuits. On the other hand, the "infinite gain paradigm" is clearly unrealistic at higher frequencies. In contrast, finite

transconductance is much closer to physical reality, explaining why "the transconductor rules" in HF[1] circuits.

Some papers and book chapters review CMOS transconductor design (e.g., [3], [5], [6]). Various circuit topologies are usually discussed, classified on a rather ad hoc basis. This paper aims at a *systematic* classification to cover *all* simple transconductor implementations, within a set of boundary conditions. One reason to focus on simple circuits is their attractive HF behavior, as motivated in Section II. Moreover, we observed in comparative studies that complex circuits only seldom outperform simpler ones, provided that a *fair* comparison is made not only based on linearity, but also on noise, transconductance and power dissipation. This paper aims to substantiate this claim. To this end, we show in Section III that SNR directly relates to the admittance level, allowing for improving SNR via "admittance level scaling," at the cost of power dissipation. Taking this scalability into account, we propose a "normalized signal to noise ratio" (NSNR) as a figure of merit for transconductor comparison. We will then compare the NSNR of virtually all *V-I* kernels that we are aware of, generated based on [7]–[9] and partly on [10]. First, simple 3-terminal kernels are introduced in Section IV and compared in Section V. Then all five different classes of "composite *V-I* kernels" [9] combining two 3-terminal *V-I* kernels are discussed in Section VI and compared in Section I. Section VIII presents conclusions.

II. Why Simple High-Frequency Transconductors?

In this section, we aim to motivate why simple transconductor circuits are preferred at high frequencies. To do so, we first discuss well-known simple *V-I* kernels, and ways to improve their output impedance. We will then analyze and compare the resulting circuits with respect to high frequency behavior and conclude that "simple is beautiful."

A. Basic V-I Conversion

Starting from the ideal desired functionality in applications shown in Fig. 1, we can already arrive at useful insights. First of all, a frequency independent, i.e., wideband, *V-I* conversion is wanted. A resistor provides *V-I* conversion, but has only two terminals, that are simultaneously voltage and current terminals [see Fig. 2(a)]. A *trans*conductor should at least have one, and preferably two current–source terminals, separate from the voltage control terminals [Fig. 2(b), (c), and (e)]. Clearly, any current-source terminal should deliver a current independent of the voltage applied to that terminal. A common source nMOS or pMOS transistor operating in saturation, as shown in Fig. 2(b) and (c), very much has the properties we are looking for: its drain terminal is high ohmic, provided that the channel length modulation and other second order effects are small. Moreover, at least at low frequencies, it has high input impedance and a low reverse transfer function (mainly determined by the gate-source and drain-gate capacitance, respectively).

In contrast to the drain, the source cannot be considered as a pure current terminal, as its voltage strongly affects the current and hence, is low ohmic. It can be considered as a simultaneous voltage and current terminal of a VCCS, resulting in 3-terminal VCCSs as shown in Fig. 2(b) and (c). Fortunately, as shown in Fig. 2(d), we can simply connect the low-ohmic terminals of two 3-terminal VCCSs to implement a 4-terminal VCCS with two separate voltage and two separate current terminals. The low-ohmic node becomes an internal node now. Of course, this node must have a well-defined bias. In the well-known differential pair, this is often done by adding a bias current source ("long-tailed pair") or by grounding the low-ohmic node. Actually, there are more ways of implementing 4-terminal transconductor starting from 3-terminal ones [9], and we will return to this subject later when we discuss composite *V-I* kernels in Section VI. For now it suffices to state that it is possible to realize a 4-terminal transconductor starting from 3-terminal transconductors and we focus on the question how we can make 3-terminal transconductors. Output impedance is a relevant issue in this respect.

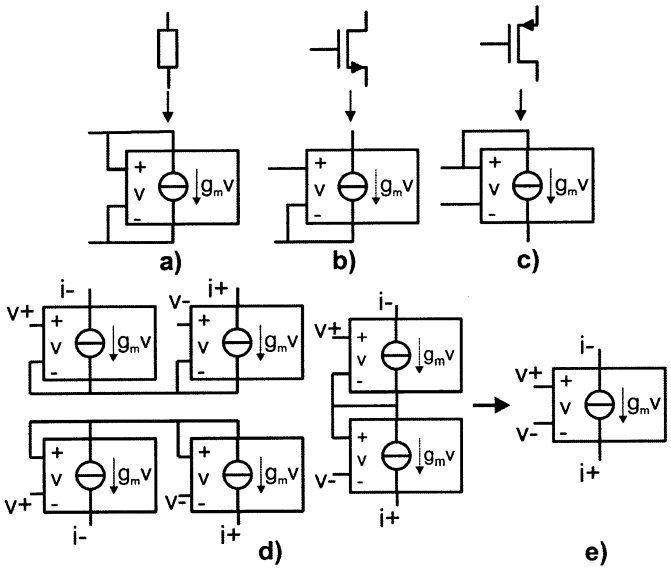

Fig. 2. VCCS representations of: (a) resistor. (b) nMOS. (c) pMOS. (d) Two 3-terminal VCCSs can be combined to implement a 4-terminal VCCS with two separate voltage and two separate current terminals (biasing not shown). (e) Symbol of 4-terminal VCCS.

B. Increasing Output Impedance

A single MOS transistor has an output resistance which is not always high enough, because of channel length modulation and other second-order effects in short channel transistors. For instance in filter applications, high-output resistance may be required, especially in high Q filters. Four frequently used techniques to increase the output resistance are shown for a N-MOSFET in Fig. 3. First, a common gate transistor can be added as shown Fig. 3(a). If this does not bring enough improvement, an active cascode can be added as in Fig. 3(b). The combination of M2 with the OPAMP aims to implement a nullor[2], that acts as a voltage follower from V_{bias} to the drain of M1, and as a current follower from drain current I_{d1} to I_{out}. A further possibility involves adding a source degeneration resistance as shown

[1]HF in this paper refers to high frequencies compared to typically $f_T/100$. For practical achievable values of f_T in CMOS and trends see [11].

[2]The combination of M2 and the OPAMP can also be considered as a current conveyor CCII- or an H-stage [14].

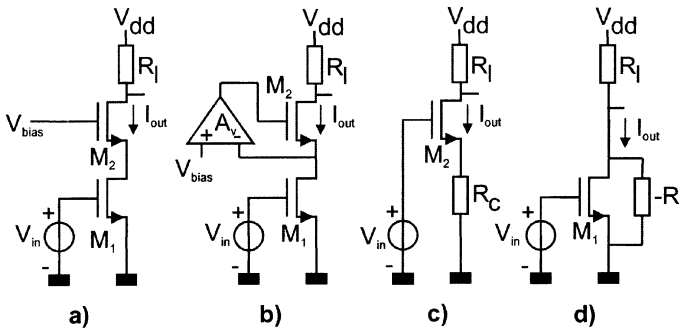

Fig. 3. Ways to increase the output resistance. a) Simple cascode. b) "Active" cascode with auxiliary amplifier implementing a nullor. c) Source degeneration. d) Adding a negative resistance.

in Fig. 3(c). Finally a negative resistance, e.g., implemented as Fig. 1(e), can be added in parallel to the output impedance as shown in Fig. 3(d). Of course, due care must be taken to ensure stability, depending on the application.

The (active) cascode in Fig. 3(a) and (b) also allows for biasing transistor M1 in triode instead of saturation. A so-called "active" triode transconductor results if the transconductance of M1 is exploited [12]. Alternatively, we can exploit the conductance of M1, which is referred to as "passive" triode operation [13]. In the latter case, the function of input and bias are exchanged: the gate voltage of M1 is used to control the conductance of M1, while the input voltage replaces $\mathrm{V_{bias}}$. In effect, the circuit in Fig. 3(a) operates as Fig. 3(c), where $\mathrm{R_c}$ is equal to the drain-source resistance of the triode MOSFET.

C. High-Frequency Behavior

Let us now analyze the HF behavior of the circuits in Fig. 3. The small signal transconductance of the circuit in Fig. 3(a) can be estimated as

$$\frac{i_{\mathrm{out}}}{v_{\mathrm{in}}} = -\frac{(g_{m1} - \mathrm{j}\omega C_{\mathrm{gd1}})(g_{m2} + g_{\mathrm{o2}})}{g_{m2} + g_{\mathrm{o2}} + g_{\mathrm{o1}}(1 + g_{\mathrm{o2}}R_{\mathrm{l}}) + \mathrm{j}\omega(1 + g_{\mathrm{o2}}R_{\mathrm{l}})C_{\mathrm{int}}} \tag{1}$$

where index 1 and 2 refer to transistor M1 and M2, Gm is the transconductance, g_{o} the output conductance, R_{l} the load resistance and C_{int} the capacitance of the "internal" node to ground ($\approx C_{\mathrm{db1}} + C_{\mathrm{gd1}} + C_{\mathrm{gs2}} + C_{\mathrm{sb2}}$). In order to achieve the desired transfer function g_{m1}, g_{m2} should be much higher then $g_{\mathrm{o1}}(1 + g_{\mathrm{o2}}\mathrm{R_l})$, as typically is the case if M1 and M2 operate in saturation. If M1 operates in triode, this is difficult to achieve without an auxiliary amplifier, as g_{o1} in triode is typically in the same order of magnitude as g_{m2} for the same dc current. The key pole is located approximately at g_{m2}/C_{int}, which is a serious problem for HF filter applications, where small parasitic phase shifts already limit the achievable quality factor of a filter seriously [1]. Adding an auxiliary amplifier introduces further excess phase shift and stability problems. Moreover, capacitance C_{gd1} introduces a right half-plane zero rendering additional excess phase shift. This zero can be cancelled by means of cross-coupling capacitances, sometimes referred to as "negative capacitors" or "neutrodynization capacitors."

Another simple option to achieve higher output impedance is by "source degeneration" via resistance R_c, as shown in Fig. 2(c). Assuming the right half-plane zero due to the gate-drain capacitance is cancelled as discussed above, we find

$$\frac{i_{\mathrm{out}}}{v_{\mathrm{in}}} = -\frac{g_{m2}}{1 + g_{m2}R_{\mathrm{c}}} \frac{(1 + \mathrm{j}\omega R_c C_{\mathrm{s}})}{1 + \mathrm{j}\omega\,(C_{\mathrm{s}} + C_{\mathrm{gs2}})\,\frac{R_c}{(1+g_{m2}R_c)}} \tag{2}$$

where C_{gs2} is the gate-source capacitance of M2 and C_{s} the total capacitance from source to ground. The effective transconductance becomes $1/R_c$, if $g_{m2} \gg 1/R_c$, and the output impedance approximately $g_{m2}r_{\mathrm{o2}}R_c$. Note that the transfer function has a pole and a *left* half-plane zero. The pole can be designed to cancel the zero by choosing $(C_s + C_{gs2})/C_s = (1 + g_{m2}R_c)$. This makes source degeneration more attractive from an excess phase point of view than the cascoded transconductor topology in Fig. 3(a).

Excess phase shift can even be reduced further exploiting simple CMOS inverters [15]. Implemented with N-MOSFETs only, the basic concept boils down to Fig. 3(d), where a negative resistance $-R$ increases the output impedance of transconductor M1. In a fully differential filter $-R$ is easily implemented using a transconductor driven by an antiphase signal. The key attractiveness of the circuit is that all gates and drains are directly connected to either the input or the output, while the source and bulk are connected to signal ground. Thus, there are *no* signal carrying nodes except for the inputs and outputs of the transconductors, which are filter nodes with a desired capacitance to ground, in which parasitic capacitance of the MOSFETs can be incorporated. Also, in gyrator-based filters, a balanced implementation of a gyrator as shown in Fig. 1(d) eliminates the effect of gate-drain capacitances, due to the cross coupling [16], [17]. Thus, to first order all frequency dependencies are cancelled, and only second-order effects like gate-resistance and non-quasi static behavior, render frequency dependence. At the time of the introduction of this transconductor, a cutoff frequency of 100 MHz was achieved in 2.5-μm CMOS technology, an order of magnitude higher then competing techniques [16]. The same techniques can also be used in current-mode filters.[3] Recent applications exploit long transistors to achieve a high dc-gain and very good matching, enabling applications in image reject IF filters, e.g., for Bluetooth [18].

Looking back on this section, we conclude that very simple circuits, with no or very few internal nodes are preferred for high frequencies. Therefore, the focus in the rest of the paper will be on simple transconductors kernels.

III. Admittance Level Scaling and Normalized SNR

The information processing capacity of circuits is strongly related to their SNR. Therefore we want to analyze the achievable SNR of transconductor circuits, and define a figure of merit for this purpose. The maximum signal is normally limited by distortion considerations, but there are many ways to express distortion (see [20] for a good overview). In the following, we will discuss the possibilities and motivate why we propose to use 1% third order intermodulation distortion as a criterion for linear signal swing. Then the noise level will be discussed to show

[3]Most filters published as "current-mode filters" are actually identical to voltage-mode filters, except for the input and output coupling stages [19].

that it can be reduced by "admittance level scaling" at the cost of power consumption. Finally, a "normalized signal to noise ratio" (NSNR) will be defined as a figure of merit to compare transconductors in a fair way.

A. Input Swing and Nonlinearity

Transconductor nonlinearity introduces unwanted frequency components and changes the transconductance at very large signal swing, and thus limits the useful input swing. In the weakly nonlinear region of a transconductor circuit, a third-order Taylor series can usually adequately model the dominant distortion mechanisms in a wide-frequency band

$$I_{\rm out}\left(V_{\rm in0}+V_{\rm in}\right)-I_{\rm out0}(V_{\rm in0})\approx g_1V_{\rm in}+g_2V_{\rm in}^2+g_3V_{\rm in}^3 \quad (3)$$

where the index 0 refers to bias values, and g_1, g_2, and g_3 are the Taylor coefficients proportional to the first-, second-, and third–order derivative of $i_{\rm out}(V_{\rm in})$. Nonlinearity is quantified in many different ways, e.g., via second- and third-order harmonic distortion HD2 and HD3, intermodulation distortion IM2 and IM3, intercept points IIP2 and IIP3, intermodulation free dynamic range and compression point. Fortunately, these quantities are related in a simple way in the weakly nonlinear region [20], e.g., $\mathrm{IM3}=3{*}\mathrm{HD3}$. For comparing stand-alone transconductors it is to some extent immaterial which quantity we use, but not from an application point of view. For narrowband applications like bandpass filters for radio receivers, it is useless to characterize harmonic distortion, as distortion products fall out-of-band. The same holds for even order intermodulation distortion products. Moreover, it is common practice to reduce even order distortion products by balancing techniques, making them of less concern. Considering the above, we decided to use the third order intermodulation distortion as the key quality criterion to compare transconductors. We propose to use *1% IM3 to define the linear input swing*. This value is high enough to be measured relatively easy, with widely available equipment. Moreover, it is low enough to still reside in the weakly nonlinear region in most practical cases, allowing for easy translation between various third-order distortion quantities to IM3. Applying two sine wave signals with equal amplitude $\hat{V}_{\rm in}$ to the input of a transconductor, IM3 can be expressed as follows [20]:

$$IM3\approx\frac{3g_3}{4g_1}\hat{V}_{\rm in}^2. \quad (4)$$

Thus, IM3 scales with the square of $\hat{V}_{\rm in}$ in the weakly nonlinear region. Extrapolation to 100% IM3 renders the "input referred third-order intercept point" (IIP3). This simple relation allows for easy translation from IIP3 data to linear input swing at 1% IM3: subtract 20 dB from IIP3. Similar reasoning reveals that the 1-dB compression point resides roughly 10-dB below IIP3 [20], i.e., 10-dB above the linear input swing. Other translations are also straightforward, e.g., the linear input swing at $\mathrm{IM3}=1\%$ is $\sqrt{3}$ times smaller than for $\mathrm{HD3}=1\%$. Finally, the linear input swing can be estimated easily from the $g_m(V_{\rm in})$ curve. With only a linear and third-order term, a parabolic curve results, where 1% IM3 roughly corresponds to 4% change in g_m, compared to $V_{\rm in}=0$.

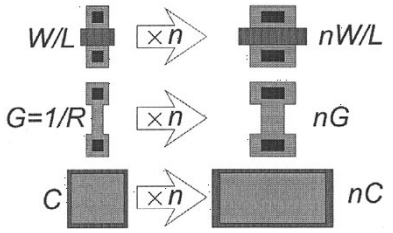

Fig. 4. Admittance level scaling with a factor n.

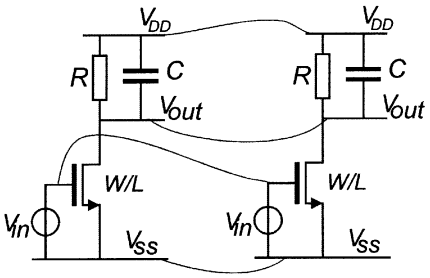

Fig. 5. Admittance level scaling with a factor n is equivalent to putting n circuits in parallel.

Summarizing, we propose to use 1% IM3 to define the linear input swing, as it has a finite meaningful value for any circuit and can be measured easily. On the other hand, it is related in a straightforward way to other well-known quantities to define nonlinearity.

B. SNR and Admittance Level Scaling

Where distortion limits the SNR at the upper side, noise is the limitation at the low side. For HF transconductors, white thermal noise is the main source of noise, and it is convenient to relate the noise current to transconductance g_m, via a noise excess factor (NEF), where

$$\bar{i}_{n,\rm out}^2=4\cdot k\cdot T\cdot\mathrm{NEF}\cdot g_m\cdot\Delta f. \quad (5)$$

A transconductor exploiting a resistor to implement $g_m=1/R$, combined with an ideal current conveyor has $\mathrm{NEF}=1$. According to simple theory, a MOSFET in strong inversion and saturation has $\mathrm{NEF}=2/3$ (in practice closer to 3/2) and a bipolar transistor and MOSFET in weak inversion has $\mathrm{NEF}=1/2$. Thus, we see that the "admittance level" of a circuit strongly determines the noise level. Actually, we can tune the thermal noise level by means of "admittance level scaling," sometimes also referred to as W-scaling of impedance scaling. Fig. 4 shows how this is done for transistors, resistors and capacitors in an IC layout, for scaling factor n. Doing so, the ratio between admittances is unchanged and as a direct result also bias voltages, signal voltages, transfer function, bandwidth and distortion do *not* change. Intuitively this is perhaps most easily understood as illustrated in Fig. 5: admittance level scaling is equivalent to putting n *identical* circuits in parallel. As all equivalent subcircuit nodes have equal bias and signal voltages, the horizontal wires do not carry any current and hence the subcircuits do not affect each other. Of course, the total bias current and signal current increases with a factor n, due to the increased admittances.

TABLE I
EFFECT OF ADMITTANCE LEVEL SCALING WITH A FACTOR n ON SIGNAL S, NOISE VARIANCE N, SIGNAL TO NOISE RATIO SNR AND POWER DISSIPATION $P_{\rm dis}$

	I_{branch}^2	V_{node}^2
S	$\times n^2$	$\times 1$
N	$\times n$	$\div n$
SNR	$\times n$	$\times n$
P_{dis}	$\times n$	

For stochastic effects, the story is different, as the parallel circuit sections are *not* identical, but show stochastic variations. Modeling these variations via stochastic current sources in parallel to the MOSFET and resistor, we can directly add the variance of parallel branch-currents, which means that the total variance *increases* with n. The variance of the node noise-voltages is proportional to the variance of the branch current, but also inversely proportional the square of the admittance, leading to n times *lower* variance.

Table I gives an overview of the effect of admittance scaling on *S*, *N*, and SNR, and power dissipation P, both in terms of squared branch currents and node voltages (squared because SNR is a power ratio). The conclusion is the same: SNR improves with with n, while the power consumption increases with the same factor (assuming constant supply voltage). Note that other stochastic properties scale in a similar way: both the variance of the equivalent input flicker noise [4] and threshold voltage mismatch [21] scale inversely with area, and hence, with scaling factor n.

Admittance level scaling is a very useful circuit design technique, as SNR is improved while distortion and bandwidth do not change.[4] Hence, we can consider the noise level (and other stochastic effects) as orthogonal and first optimize a design for distortion and bandwidth, without considering noise. In a second step, we can then tune SNR to the desired level via admittance scaling, without affecting distortion and bandwidth.

Summarizing, we conclude that admittance level scaling can improve the SNR ratio with a factor $\rm n$, however, at the cost of an equal factor $\rm n$ in power consumption.

C. Normalized SNR

In Section III-B, it was concluded that SNR of *any* transconductor can be improved by admittance level scaling, at the cost of power dissipation. To make a fair comparison between different *V–I* kernels with respect to SNR, it is important to take this degree of design freedom into account. Another issue that complicates comparison is the fact that transconductors used for different applications are designed for different distortion level and noise bandwidth. However, if we know how SNR scales with power consumption, noise and distortion, we can eliminate the differences, and make a fair comparison under "normalized" conditions. We saw in the previous section that SNR increases linearly with power, assuming admittance level scaling. Furthermore, assuming white noise and fixed $\rm S$, SNR scales inversely proportional with bandwidth BW. For distortion the relation is in general more complex. However, if we characterize a transconductor in the weakly nonlinear region, IM3 increases with the square of the input voltage (4), i.e., linearly with power $\rm S$. As a result SNR scales linearly with the IM3 requirement, i.e., if higher IM3 is tolerated, then SNR can be higher.

Due to these direct proportionalities, we can now derive a simple relation between the NSNR and the actual SNR, IM3, bandwidth BW, and power dissipation $\rm P_{dis}$ of a specific transconductor. In dB it is

$$\mathrm{NSNR[dB]} = \mathrm{SNR[dB]} + 10\log\left(\frac{\mathrm{IM3_N}}{\mathrm{IM3}}\frac{\mathrm{BW}}{\mathrm{BW}_N}\frac{P_N}{P_{\rm dis}}\right) \quad (6)$$

where the index $\rm N$ refers to normalized values. We propose to normalize to the following "1–1–1 conditions:"

- $\mathrm{IM3_N} = 1\%$
- $\mathrm{BW_N} = 1$ Hz
- $\mathrm{P_N} = 1$ mW.

The choice for 1% IM3 was motivated in Section III-A. 1-Hz normalization bandwidth is common for noise measurements and simulation. 1 mW is mainly for practical reasons, as the power consumption of circuits is typically expressed in mW, while signal power is RF circuits is often expressed in decible milliwatts, again with 1 mW as reference.

Thus, all "normalization actions" linearly affect the power-ratio SNR, and are in between the brackets of the $10*\log$ term. This results in a simple conversion to normalized values. E.g. if a transconductor achieves 70-dB SNR ratio in a bandwidth of 10 MHz, at $\mathrm{IM3} = 0.1\%$, while dissipating 10 mW, the normalization action corresponds to multiplying by $10\times 1\mathrm{E}7\times 0.1 = 1\mathrm{E}7$, so $\mathrm{NSNR} = 140$ dB.

Using (6), we can calculate and compare NSNR based on simulated or measurement data. However, we also would like to estimate the achievable NSNR directly, in terms of transistor properties. To this end, let us analyze the SNR of the output current, assuming operation at normalized conditions where possible. In this case $\mathrm{S} = 1/2\cdot(g_m\cdot V_{\mathrm{in},1\%\mathrm{IM3}})^2$, where the 1/2 is for conversion from pk- to rms-values, and $\mathrm{N} = 4\mathrm{kT}\cdot g_m\cdot\mathrm{NEF}\cdot\mathrm{BW_N}$. Normalization for $\rm P_{dis}$ leads then to

$$\mathrm{NSNR} = \frac{\frac{1}{2}g_m^2\cdot\hat{V}_{\mathrm{in},1\%\mathrm{IM3}}^2 P_N}{4kTg_m\mathrm{NEF}\cdot\mathrm{BW}_N P_{\rm dis}} = \alpha_{\rm N}\frac{g_m\cdot\hat{V}_{\mathrm{in},1\%\mathrm{IM3}}^2}{\mathrm{NEF}\cdot P_{\rm dis}} \quad (7)$$

where $\alpha_{\rm N}$ is independent of circuit design, given by

$$\alpha_N = \frac{P_N}{8kT\cdot\mathrm{BW}_N}. \quad (8)$$

Thus, it turns out that in order to optimize the NSNR of a transconductor, we should maximize the g_m and the linear input swing ($\hat{V}_{\mathrm{in},1\%\mathrm{IM3}}$), while minimizing NEF and $P_{\rm dis}$. It is interesting to note that g_m times the linear input swing is the peak output signal current, which is always smaller then the supply current for a transconductor implemented with only resistors and transistors. The useful linear input swing is in practice limited to half of the supply voltage, assuming

[4]This holds as long as everything scales, which may not be possible at the input and output of a system, where admittance levels are often fixed.

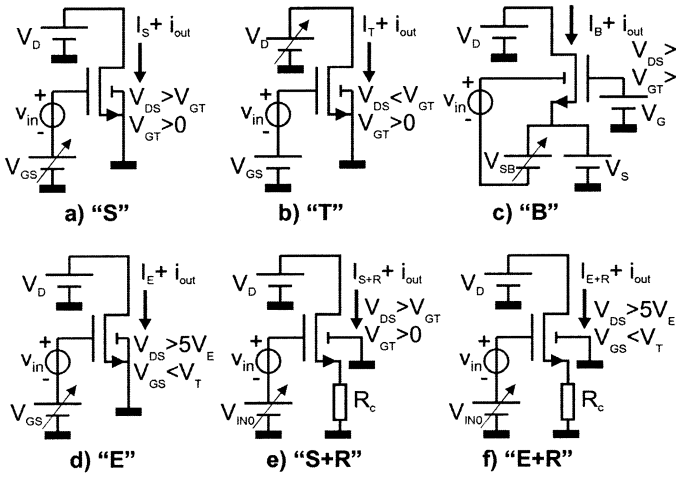

Fig. 6. Overview of the basic *V-I* kernels "S", "T", "B", "E", "S+R," and "E+R." The transconductance is tuned via the battery with arrow.

rail-to-rail operation. Furthermore, NEF is 1 for a resistor, and higher then 1/2 for any transistor we are aware off. We conclude that for any practical transconductor circuit implemented with resistors and transistors, $\alpha_{\rm N}$ is the *maximum achievable NSNR*. Expressing $\alpha_{\rm N}$ in dB, this result in approximately *165 dB* at room temperature.

IV. Systematic Generation of 3-Terminal *V-I* Kernels

As motivated in Section II, simple *V–I* kernels are highly preferred for high-frequency applications. We would like to cover *all* possible simple *V–I* kernels based on a MOSFET and resistor in a systematic way. It was already concluded that the drain should be the output. This leaves the gate, source, and bulk as input voltage terminals. Moreover, a MOSFET can be used in different operating regions. Thus, the number of possibilities quickly grows, if we take into account more elements and different operating regions of the transistor. For the comparison we want to take all relevant cases into account, but also like to limit the number of cases. In the following paragraphs, different options to implement a 3-terminal transconductor are discussed and a pre-selection is made. We also like to obtain symbolic expressions for the bias current, g_m, g_3, NEF, and NSNR. First, we will briefly discuss the basically different *V–I* kernels found in literature. Fig. 6 gives an overview of the resulting kernels and Table II lists the key symbolic expressions. For briefness we indicate each case by a unique letter combination.

A. Saturated Strong Inversion MOSFET: "S"

According to simple theory, a MOSFET operating in strong inversion and saturation, has infinite output impedance and a square-law $\mathrm{I_D}(V_{\rm GT})$ characteristic, where $V_{\rm GT}$ represents the "overdrive voltage" or "effective" gate-source source voltage, i.e., the amount of gate-source voltage in excess of $V_{\rm T}$ ($V_{\rm GT} = V_{\rm GS} - \mathrm{V_T}$). In this idealized case it can be considered as a true "S-VCCS," with S referring to saturation but also square-law. Its transconductance $\beta \mathrm{V_{GT}}$ linearly increases with $\mathrm{V_{GT}}$, with $\beta = \mathrm{W/L} * \mu \mathrm{C_{ox}}$. This holds until the transistor leaves strong inversion ($\mathrm{V_{GT}} < 0$) or saturation ($\mathrm{V_{GT}} > V_{\rm DS}$). According to this simple model, the third-order Taylor coefficient g_3 is zero, and hence $\mathrm{IM3} = 0$ [see (3)]. A practical MOSFET of course has second–order effects, where mobility reduction is usually the most important effect modeled via a $\theta V_{\rm GT}$ term in Table II. As a result g_m does not increase linearly with $V_{\rm GT}$. In practice, it even drops at high $V_{\rm GT}$, which is not modeled adequately by the θ-model. However, we want to derive first-order estimation expressions that are simple and grasp the main trends. We use the θ-model for lack of a better simple alternative. We will verify the results later with simulations using advanced models. For consistency with the other operating regions, we decided to include δ-terms modeling the bulk effect (see Section IV-B). The noise in saturation will be coarsely modeled as $\mathrm{NEF} = \gamma_{\rm S}$, where $\mathrm{NEF} = \gamma_{\rm S} \approx 1.5$ based on simulation results.

B. Triode Strong Inversion MOSFET: "T"

As mentioned in Section II, the transconductance of MOSFET in the Triode region ("T") can also be exploited [12], but a high-gain (active) cascode circuit is required, which is definitely a disadvantage at high frequencies. Its transconductance is $\beta V_{\rm DS}$ according to the ideal square-law model. Theoretically, $V_{\rm DS}$ can vary from $V_{\rm GT}$ down to zero. In practice, inaccuracies limit the minimum robustly achievable $V_{\rm DS}$ to around 10 mV. Still, a large transconductance range results. Also, large input voltage swing is possible as $V_{\rm GT}$ can vary from 0 up to $V_{\rm DS} + V_{\rm T}$ (transition to saturation). Usually, mobility reduction is the dominant source of nonlinearity, and we use the θ-model despite of the inaccuracy discussed in [10]. For noise modeling, we use $\mathrm{NEF} \approx \gamma_{\rm S} V_{\rm GT}/V_{\rm DS}$, modeling the main trend discussed in [4]. Note NEF becomes equal to $\gamma_{\rm S}$ at the boundary of saturation ($V_{\rm GT}/V_{\rm DS} = 1$), while it goes to infinity for $V_{\rm DS} = 0$.

C. Bulk Driven MOSFET: "B"

A saturated strong inversion MOSFET can also be used with the back-gate or bulk as input voltage terminal, exploiting $\mathrm{g_{mb}}$ of a MOSFET [22], [23]. Especially in new twin-well IC-processes this is becoming a more vital option for both nMOS and pMOS devices. For simplicity, and to isolate effects, we will keep other device potentials constant. Note that changing only the bulk potential actually modulates the threshold voltage, and thus effectively changes the overdrive voltage $V_{\rm GT}$ with $-V_{\rm SB}\delta$, where δ models the linearized body effect [4]. Thus, bulk driving can be modeled in the same way as gate-driving, with an additional attenuation $-\delta$ [23]. In principle, we can also make the attenuation in another way, e.g., via a floating gate device. Also, we can bias the MOSFET in triode instead of saturation or weak inversion. To limit the number of cases, we will not consider these cases further, but stick to the saturated case which is most common. Based on the insight that will result from this, one can easily analyze the operation in other cases combining expressions given in Table II.

D. Exponential Weak Inversion: "E"

In weak inversion, the MOSFET has an exponential $I(V)$ characteristic relating to diffusion currents, similar to a bipolar transistor. Where a bipolar transistor has a current proportional to $\exp(V_{\rm BE}/V_E)$ with $V_E = \phi_T = kT/q$, the current of a

TABLE II
OVERVIEW OF THE MAIN PROPERTIES RELEVANT FOR THE NSNR CALCULATION, FOR THE *V-I* KERNELS IN FIG. 6
($V_{GT} = V_{GS} - V_T$, $V_{GT0} = V_{GT}$ FOR $V_{SB} = 0$)

	I_{dd}	g_m	g_3	NEF	NSNR
S	$I_S = \frac{\beta}{2(1+\delta)} \frac{V_{GT}^2}{1+\theta V_{GT}}$	$\frac{\beta}{1+\delta} \frac{V_{GT}\left(1+\frac{\theta}{2}\cdot V_{GT}\right)}{(1+\theta\cdot V_{GT})^2}$	$-\frac{\beta}{2(1+\delta)} \frac{\theta}{(1+\theta\cdot V_{GT0})^4}$	$\gamma_S \approx 1.5$	$\approx \frac{16(1+\theta V_{GT})^2 \alpha_N IM3_N}{3\gamma_S \theta V_{dd}}$
T	$I_T = \beta \frac{V_{GT}V_{DS} - \frac{1+\delta}{2}V_{DS}^2}{1+\theta V_{GT}}$	$\frac{\beta V_{DS}\left(1+\frac{1+\delta}{2}\theta V_{DS}\right)}{2(1+\theta V_{GT})^2}$	$\frac{\beta V_{DS}\theta^2\left(2+\frac{1+\delta}{2}\theta V_{DS}\right)}{2(1+\theta V_{GT})^4}$	$\approx \frac{V_{GT}}{V_{DS}}\gamma_S$	$\approx \frac{4V_{DS}\left(1+\frac{\theta}{2}V_{DS}\right)(1+\theta V_{GT})\alpha_N IM3_N}{3V_{GT}^2\gamma_S\theta^2 V_{dd}}$
E	$I_E = I_{E0} e^{V_{GS}/V_E}$	$\frac{I_E}{V_E}$	$\frac{I_E}{6V_E^3}$	$\approx \frac{1+\delta}{2}$	$\approx \frac{16 V_E \alpha_N IM3_N}{(1+\delta)V_{dd}}$
B	$I_B = I_S\Big\vert_{V_{GT}=V_{GT0}-\delta V_{SB}}$	$-\delta\cdot g_{m,S}\Big\vert_{V_{GT}=V_{GT0}-\delta V_{SB}}$	$-\delta^3\cdot g_{3,S}\Big\vert_{V_{GT}=V_{GT0}-\delta V_{SB}}$	$\approx \frac{\gamma_S}{\delta}$	$\approx NSNR_S$
S+R	$I_{S+R} = I_S\Big\vert_{V_{GT}=V_{IN0}-V_T-I_{S+R}R_c}$	$\approx \frac{\beta V_{GT}}{1+\beta V_{GT}R_c+\frac{3}{2}\theta V_{GT}}$	$-\frac{\beta^2 R_c}{2\cdot(1+\beta V_{GT}R_c)^5}$	≈ 1	$\approx \frac{16(1+\beta V_{GT}R_c)^3\alpha_N IM3_N}{3\beta R_c V_{dd}}$
E+R	$I_{E+R} = I_E\Big\vert_{V_{GS}=V_{IN0}-I_{E+R}R_c}$	$\frac{I_{E+R}}{I_{E+R}R_c+V_E}$	$\frac{V_E I_{E+R}(V_E-2I_{E+R}R_c)}{6(V_E+I_{E+R}R_c)^5}$	≈ 1	$\approx \frac{8(I_{E+R}R_c+V_E)^3\alpha_N IM3_N}{(2I_{E+R}R_c-V_E)V_E V_{dd}}$

weak inversion MOSFET depends on $\exp(V_{GS}/V_E)$ with $V_E = (1+\delta)\phi_T$. We will use V_{DS} values above a few hundred mV, where the drain current effectively saturates and is largely independent of the drain voltage. In principle we can also use low drain–source voltages. However, this introduces a problem (low output resistance), while it does not seem to offer any advantages. For the weak inversion region $\mathrm{NEF} = (1+\delta)/2$ [4].

With the ever-reducing supply voltage and higher f_T of deep submicrometer processes, the moderate inversion region is becoming increasingly attractive as operating region. For lack of space, and to gain insight, our analytical analysis will only deal with the "S" and "E" case as extreme cases, relying on physics for a smooth interpolation between the two in moderate inversion. The model proposed in [24] might be useful to derive one expression for all regions.

E. S-MOSFET With Degeneration Resistor ("S+R")

If continuous tuning range is not so important, then a fixed resistor can be used as the basis for *V–I* conversion, using a MOSFET as nullor approximation. If we bias the MOSFET in strong inversion and saturation, we can use the "S" model equations, substituting $V_{GT} = V_{IN0} - I_{S+R}R_c$. We will choose R_c and W/L such that the resistors dominates the *V–I* conversion and noise, i.e., $\mathrm{NEF} = 1$.

F. E-MOSFET With Degeneration Resistor "E+R"

Source degeneration can also be applied for a MOSFET biased in weak inversion. The exponential $I(V)$ characteristic is more nonlinear, but also offers higher transconductance, i.e., more degeneration loop-gain improving linearity. Hence it is interesting to compare it to the S+R case. Furthermore, in BiCMOS processes a bipolar exponential device is an alternative for using a strong inversion MOSFET, and this case can be analyzed by substituting $V_E = \phi_T = kT/q$.

G. Passive MOSFET Transconductors

The source of a MOSFET can also be used as input, exploiting the MOSFET in as "passive" way. It has been shown [10] that passive use of a strong inversion saturated transistor renders behavior very similar to the "active" gate-driven case. This is because the key difference is due to the body effect, typically introducing much less nonlinearity then the mobility reduction effect. Thus passive use of a saturated MOSFET renders $I(V)$ characteristics very similar to active use, but with the disadvantage that the input impedance is low. Hence we skip this case.

A passive triode resistor can also be used [13], [10]. However, even if the linearity of the conductance is good, a current conveyor is needed. Thus, the S+R case gives a first order estimate for the achievable NSNR in this case, by substituting a variable resistance $1/g_{ds}$ in place of R_c. In the section on transconductance tuning range, we will return to this subject.

V. NSNR OF 3-TERMINAL *V–I* KERNELS

Having generated a set of different 3-terminal *V–I* kernels, we can now compare their performance with respect to linear input swing, transconductance tuning range, and NSNR. Before we do so we need to discuss the test conditions and parameter choices for the comparison.

A. Parameter Choice and Biasing Conditions

It is difficult to make a fair comparison between published transconductors based on the results reported in literature, as different IC technologies are used, different device dimension and different biasing conditions. Therefore we simulate all transconductor circuits using fixed transistor dimensions and bias ranges, and a nominal set of parameters for a standard 0.18-micrometer CMOS process. nMOS transistors were used, as these have 2–3 times less capacitance for the same transconductance, improving the bandwidth. For the same reason we use minimum length MOSFETs.

TABLE III
BIAS VARIABLE RANGES AND PARAMETERS USED FOR THE CALCULATIONS AND COMPARATIVE TESTS OF SIMPLE *V-I* KERNELS IN FIG. 6

	S	T	B	E	S+R	E+R
Tune:	V_{GS}	V_{DS}	V_{SB}	V_{GS}	V_{IN0}	V_{IN0}
min	0.55V	.01V	0V	.25V	0.5V	0.5V
max	1.5V	0.7V	.5V	.45V	1.5V	1.5V
V_D	1.2V	= V_{DS}	1.2V	1.2V	1.2V	1.2V
V_G	= V_{GS}	1.2V	1.2V	= V_{GS}	= V_{IN0}	= V_{IN0}
V_S	0V	0V	.5V	0V	$I_{S+R}R_c$	$I_{E+R}R_c$
V_B	0V	0V	.5-V_{SB}	0V	0V	0V
R_c	-	-	-	-	1KΩ	100KΩ
All:	W=10μm, L=0.18μm, β=0.02A/V^2, V_T=.5V δ=0.2, θ=2.5V^{-1}, V_{dd}=1.8V					

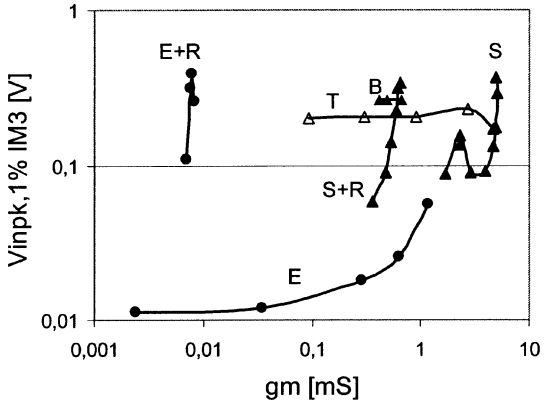

Fig. 7. Linear input swing at $\mathrm{IM3} = 1\%$ versus g_m of the basic *V–I* kernels, for fixed W/L and tuning via bias values as indicated in Table III.

Fig. 6 shows how the *V–I* kernels are biased, with arrows indicating the transconductance tuning variable. Table III lists the biasing ranges used for the tuning variables and other key parameters for the 0.18-μm CMOS process that was used. The input and output dc level are chosen equal, roughly halfway V_T and V_{dd}, for direct voltage compatibility of transconductor in- and outputs. This is a practical value for more or less optimal signal swing in strong inversion circuits. Furthermore, this still allows for a reasonable voltage headroom for a pMOS bias current source that is usually required between V_{dd} and the output node. As the variance of the noise current is roughly proportional to $g_m = 2I_{\mathrm{bias}}/V_{\mathrm{GT}}$, we want to use a pMOS with as high a $|V_{\mathrm{GT}}|$ as possible. As V_{GT} is also the saturation voltage, this means that considerable voltage drop must be reserved for reducing the noise of the pMOS current source.

B. Input Swing at 1% IM3 and Tuning Range

We will now compare the *V–I* kernels, using 1% IM3 as a criterion as motivated in Section III. Fig. 7 shows the linear input swing versus g_m, as simulated with the Philips MM9 model [25]. Simulation with BSIM3v3 models were also done and show very similar trends, discussed below.

- The highest input swing is achieved with the resistively degenerated case (S+R and E+R), and the S case. However, all curves are very steep, meaning that the available g_m-tuning range at high swing is very small.
- The B case renders good input swing but less tuning range than the S case, because of the $\delta \cdot \mathrm{V_{SB}}$ term can only be tuned over 0.1 V. with 0.5 V. source-bulk voltage bias-range. In principle, δ^2 times better linear input swing is expected according to Table II. However, this calculation assumes weakly nonlinear operation, and the actual voltage swing is hard-limited here due to the low $\mathrm{V_{GT0}}$ of 0.2 V (note that $VS = 0.5$ V).
- As expected, the triode (T) case renders large tuning range with large linear input swing. Only at high g_m a slight tradeoff with input swing is seen (entering the saturation region).
- The E case has large tuning range due to the exponential characteristic, but also low linear input swing.

C. Non-Linearity Modeling and Distortion Cancellation

Between weak inversion and strong inversion, a peak in linear input swing occurs. This is because, as can be verified from Table II, the third-order coefficient g_3 is positive in weak inversion (E) and negative for the S case, and passes zero in between. Such a zero also occurs between the saturation and triode region, and for the E+R case if $V_E = I_{E+R}R_c$ [20]. However, in practice the value of such optima is limited. Even if $\mathrm{g_3}$ is zero, this does not mean that zero IM3 results, as higher order nonlinearities also contribute to IM3. Moreover, the robustness of such optima over process spread and temperature variations is highly questionable (no data available from foundries). Similar problems often occur when aiming for distortion cancellation. In general we consider such cancellations only robust if one nonlinearity effect is cancelled with another originating from the *same* physical cause. However, even if this is the case, models may be inadequate. For instance, attempts have been made to exploit the difference in the sign of $\mathrm{g_3}$ in the T and S case (θ-model see Table II) [26], [27]. However, it turns out that the θ-model is simply not accurate enough [10], [26], [28], [30]. Although models have improved in some respect, the key issue of the reproducibility and hence robustness of cancellation techniques remains. The full benefit of such cancellation techniques can probably only be achieved if combined with some form of automatic distortion tuning. Therefore, during the comparison of *V–I* kernels that will follow later in this paper, we do not take such cancellations into account further. For the same reason and for lack of space, we also do not discuss other optimized combinations of saturated devices combined with triode devices (e.g., [29], [31]).

D. NSNR of Simple 3-Terminal Transconductors

We will now calculate and compare the NSNR of the basic *V–I* kernels. Using (7) and (4), NSNR can be rewritten as

$$\mathrm{NSNR} = \alpha_{\mathrm{N}} \frac{g_m \cdot \hat{V}^2_{\mathrm{in,1\%IM3}}}{\mathrm{NEF} \cdot P_{\mathrm{dis}}} = \alpha_{\mathrm{N}} \frac{4 \cdot g_m^2 \cdot \mathrm{IM3_N}}{3 \cdot \mathrm{NEF} \cdot g_3 V_{\mathrm{dd}} I_{\mathrm{dd}}}. \quad (9)$$

The equations in Table II and the biasing ranges of Table III were used to calculate NSNR and the results are shown in Fig. 8. Simulation results are shown in Fig. 9.

Comparing the two figures, we see that the θ-model leaves a gap between the S and the T cases, and does not predict the

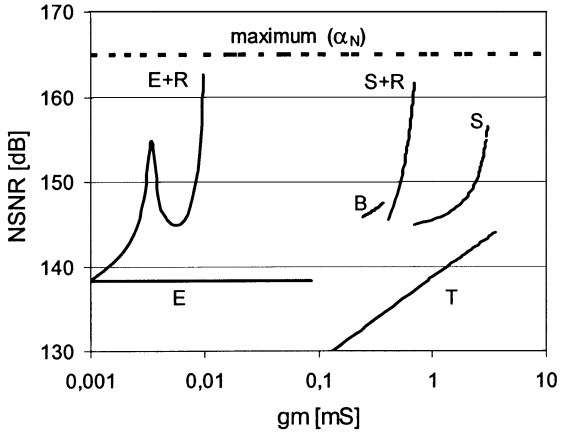

Fig. 8. NSNR versus g_m of the basic *V–I* kernels, calculated according to Table II for fixed W/L and tuning via bias ranges indicated in Table III.

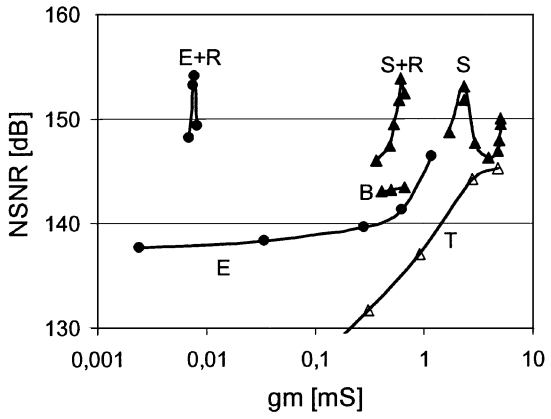

Fig. 9. Simulated NSNR versus g_m of the basic *V–I* kernels, for fixed W/L and tuning via bias values as indicated in Table III.

distortion cancellation points discussed in the previous section. Still, the model can serve as a coarse indication of trends, which is useful for first order design considerations. We will now discuss the NSNR results, starting with the best.

- The best NSNR results are obtained by the S+R and E+R kernels, and are around 154 dB. The calculations of Fig. 8 predict somewhat higher values, as they assume weakly nonlinear operation, which is not always valid the higher signal swings. The E+R case achieves roughly the same NSNR as the S+R case, but at much lower g_m. This is because $\mathrm{R_c}$ is 100 times larger for the E+R case, to bias the MOSFET with fixed W/L in weak inversion. To scale this up to the same g_m, much larger area is needed resulting in much higher input capacitance of the *V-I* kernel.
- The saturated MOSFET (S) achieves NSNR values in the range of > 145 dB over a $1:3$ gm-range. However, the tuning range decreases for newer technologies due to mobility reduction effects. Good linearity is still expected [11].
- The bulk driven MOST ("B") theoretically renders the same NSNR as the S case for the same bias point. This is because its input voltage swing is $1/\delta^2$ times higher (see Table II), but $\mathrm{NEF} = 1/\delta$ and g_m is δ times smaller. Thus, the $\mathrm{NSNR_B}$ curve can be considered as a part of the $\mathrm{NSNR_S}$ characteristic, shifted to the left due to the lower transconductance (see Fig. 8). In practice, the B case is worse, as the maximum V_{GT} is reduced by the value of V_{S} (0.5 V in this example).
- The weak inversion (E) case renders $\mathrm{NSNR} \approx 138$ dB, as predicted accurately by the model. For increasing gate-bias, this value gradually goes up in the moderate inversion region to around 145 dB at the threshold voltage. An attractive point is its large tuning range.
- The triode (T) device also has a large tuning range, but unfortunately its NEF goes to infinity for low V_{DS}, rendering very poor NSNR, even worse than for weak inversion.

These results strongly illustrate the importance of NEF and g_m for the NSNR, apart from the linear input range. Many transconductor linearization techniques that have been proposed more or less neglect this issue by using lots of additional transistors for improving linearity, without considering the noise performance and reduction in g_m. Note that three times worse NEF results in roughly 10-dB loss in NSNR, which means that ten times more power consumption is required to achieve a given SNR! In many case, it is more effective to use an attenuator followed by a simple transconductor, scaled with admittance level scaling to achieve sufficiently low noise. This highlights the usefulness of NSNR as a figure of merit for comparing transconductors.

E. NSNR of Practical Transconductors

Note that the operating conditions of the basic *V–I* kernels is highly idealized. Thus in practice there are many reasons why the NSNR of a practical circuit will be lower, for instance:

- Large transconductance tuning range. As discussed above, high NSNR is only available over a small tuning range. If a large tuning range is needed, e.g., for adaptive filters, this often comes at the cost of lower NSNR.
- Cascode and biasing circuits. Such circuits are often needed for instance to improve the output impedance or implement level shifts. These circuits add noise and power consumption, while the linear input swing and g_m typically remains equal to the values obtained by the *V–I* kernel devices.
- Over-design for robustness. As circuits have to work over IC-process and temperature variations, it is common practice to create margin by "oversized" admittance level scaling.

For these reasons it is not uncommon to loose 30 dB of NSNR, especially when large tuning range is required. Still, NSNR is very useful as a figure of merit comparing various design alternatives. Moreover, comparison to the maximum achievable $\mathrm{NSNR} = \alpha_{\mathrm{N}}$ (165 dB) is very instructive, to see where the design "looses its decibles."

F. Future Trends: Switched Degenerated MOSFETs

Having discussed the basic kernels and their combination in composite kernels, we conclude that large tuning range and large NSNR is not easily obtained simultaneously. In principle, a passive triode transistor can be tuned over a reasonably large range of conductance values (although second-order effect lead to less

tuning range). However, experiments show that passive triode MOSFETs alone do not bring the level of linearity (and NSNR) that resistive degeneration can bring [32], [33]. Also, physical effects, which used to be second order effects, are now becoming first-order effects, complicating modeling and circuit design. In contrast, resistive degeneration is a very robust technique relying on resistor linearity and negative feedback. With processes becoming faster and allowing more degeneration loop gain up to higher frequencies, this seems to be the most robust technique to obtain high NSNR and high linearity in future processes. This also helps to improve output impedance and reduce the nonlinearity of the output conductance, which is of increasing concern especially in applications with voltage gain. Moreover, it helps to reduce $1/f$ noise, which is dominating thermal noise up to ever higher frequencies (using an simple textbook model, the $1/f$ corner frequency tracks f_T).

If we use resistive degeneration, transconductance tuning needs to be solved. With the trend to more and more digital systems with digital control and calibration, switching transconductors seem the obvious way to go. If analog continuous control is needed, a combination of fixed degeneration resistors and gradually switched ("soft-switched") triode MOSFETs seems the most attractive techniques to achieve high NSNR [32], [33].

VI. Composite 2-VCCS *V-I* Kernels

In Section II, we briefly mentioned that there are several options in combining 3-terminal VCCSs to acquire a 4-terminal VCCS, with separate *V*-terminal and *I*-terminals. This is one reason to look at the various options to combine VCCSs. Furthermore, combining VCCSs might lead to linearity and other advantages, and this is another reason to consider VCCS-combinations. If this leads to a new 3-terminal VCCS, we can even use combination-techniques in a nested way to implement a 4-terminal VCCS if that is required.

It can be shown that there exist only a limited number of different ways to combine two VCCS blocks to create a two-port network with a well-defined transfer function [9]. Such networks have a transfer function defined by the transconductance values of the two VCCSs, e.g., the sum or difference of two g_m-values or a g_m-ratio. Systematic circuit topology generation via graphs leads to 145 possible two-ports with two VCCSs [8]. The circuit can be classified in 12 classes of circuits [9], based on the set of two Kirchhoff relations that is forced by the interconnection pattern of the VCCSs, and their connection to the signal source and load. In case of transconductors, five classes with useful behavior result[5] [9], represented in Fig. 10. The name of each class refers to the two variables that are being forced by Kirchhoff equations (e.g., $\{V_\Sigma, V_\Delta\}$ means that a sum-voltage and difference-voltage is forced). Many variants on these circuits exist, but the behavior of the transconductor core is essentially the same in a lot of respects.

For the circuits with a differential output, the output current will be $I_{o1} = I_{\rm bias} + i_{\rm out}$ and $I_{o2} = I_{\rm bias} - i_{\rm out}$. To obtain an output current $i_{\rm out} = g_m v_{\rm in}$ for the 4-terminal transconductor in Fig. 3(e), the output current is defined as

$$i_{\rm out} = \frac{I_{o1} - I_{o2}}{2}. \tag{10}$$

For cases with a differential input, the *differential* voltage should be equal to $v_{\rm in}$. Pure differential drive hence means

$$V_{\rm in+,-} = V_{\rm IN,CM} \pm \frac{1}{2} v_{\rm in}. \tag{11}$$

We will now discuss the five classes of circuits which combine two VCCSs is essentially different ways. Fig. 10 shows circuit implementations using two 3-terminal VCCSs and one example of a transistor implementation. Table IV summarizes the most important functional properties of the five classes of circuits: the input voltage variable, the tuning variable, the output current definition and g_m. The other columns will be discussed in the next section, when we deal with NSNR.

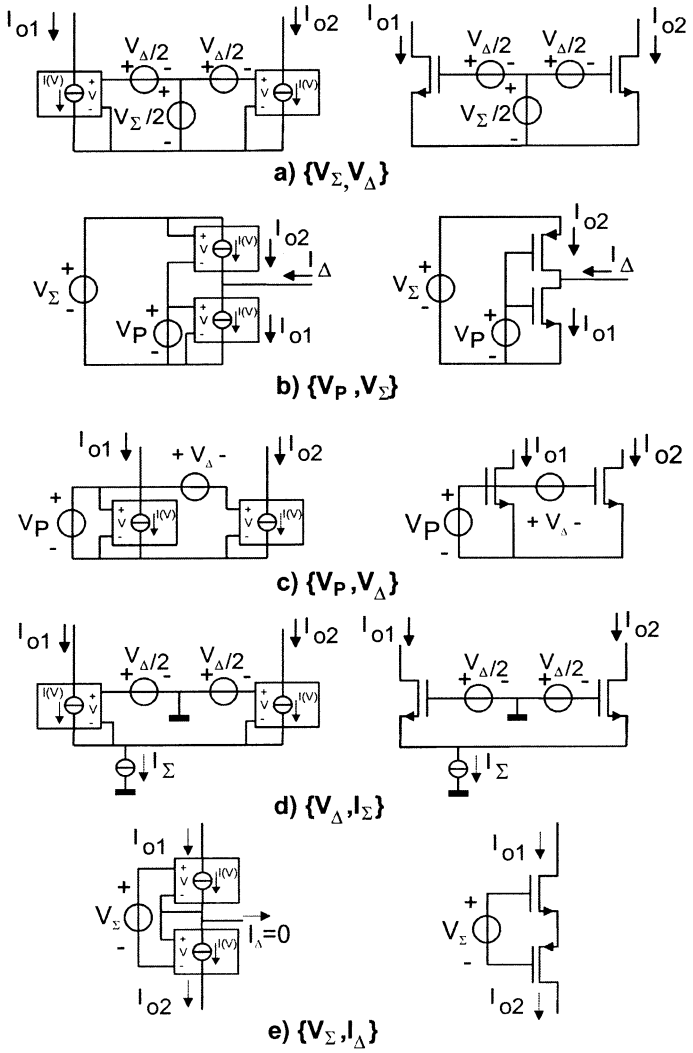

Fig. 10. Five different ways of combining two transconductors by forcing a different set of two Kirchhoff relations, indicated in the class name. One example of a circuit implementation is also given.

[5]Due to lack of space, we limit ourselves here to the cases that have proven to be useful in actual circuits. For other options see [7] and [9]

TABLE IV
EFFECT OF THE FIVE CLASSES OF TWO-VCCS COMBINATION TECHNIQUES ON DISTORTION AND NSNR COMPARED TO A SINGLE 3-TERMINAL VCCS

Class	V_{in}	Tune	i_{out}	g_m	g_2	g_3	$V_{in,1\%IM3}$	NEF	P_{dis}	NSNR
$\{V_\Sigma, V_\Delta\}$	V_Δ	V_Σ	$\frac{I_{o1}-I_{o2}}{2}$	$\div 2$	$\times 0$	$\div 8$	$\times 2$	$\times 1$	$\times 2$	$\times 1$
$\{V_P, V_\Sigma\}$	V_P	V_Σ	$I_{o1}-I_{o2}$	$=g_{mn}+g_{mp}$ $\approx \times 2$	$=g_{2n}-g_{2p}$ $\approx \times 0.1$	$=g_{3n}+g_{3p}$ $\approx \times 2$	$\approx \times 1$	$\approx \times 1$	$\approx \times 1$	$\approx \times 2$
$\{V_P, V_\Delta\}$	V_P	V_Δ	$\frac{I_{o1}-I_{o2}}{2}$	$=\Delta g_m/2$	$=\Delta g_2/2$	$=\Delta g_3/2$	depends on I(V)	$\times \Sigma g_m/\Delta g_m$	$\times 1...2$	$\times 1.....\times 0$ (bad NEF!)
$\{V_\Delta, I_\Sigma\}$	V_Δ	I_Σ	$\frac{I_{o1}-I_{o2}}{2}$	$\div 2$	$\times 0$	$=\pm\frac{g_1 g_3 - 2g_2^2}{8g_1}$	depends on sign of g_3	$\times 1$	$\times 2$	depends on sign of g_3
$\{V_\Sigma, I_\Delta\}$	V_Σ	V_Σ	$I_{o1}=I_{o2}$	$\div 2$	$\div 4$	$\div 8$	$\times 2$	$\times 1$	$\times 1$	$\times 2$

A. $\{V_\Sigma, V_\Delta\}$ Circuits

Fig. 10(a) shows a $\{V_\Sigma, V_\Delta\}$ circuit, in which the sum of the two VCCS-voltages is forced equal to V_Σ, while the difference is forced equal to V_Δ. A commonly used example is the balanced driven common source pair. It realizes a 4-terminal VCCS with differential input voltage V_Δ, and an output current as defined by (10). Transconductance tuning is possible via V_Σ, provided that the VCCS has a nonlinear characteristic. For ideally matched VCCSs, and $V_\Delta = 0$, the circuit has infinite common mode rejection, from common mode input voltage $V_\Sigma/2$ to the differential output current. However, for nonzero differential input voltage or in case of mismatch, a differential output will result.

B. $\{V_P, V_\Sigma\}$ Circuits

Fig. 10(b) shows a $\{V_\mathrm{P}, V_\Sigma\}$ circuit, in which the input voltage source forces a so-called "primary" VCCS voltage V_P [9], while the sum of the VCCS-voltages is forced equal to V_Σ. This class is strongly related to the previous one, but the full input voltage swing is now applied to both VCCSs, and it has a single-ended input. Thus it implements a 3-terminal VCCS from V_P to the difference of two VCCS-currents. The simplest implementation is a CMOS inverter configuration [15]. The transconductance can be tuned by V_Σ and is equal to $g_{mn} + g_{\mathrm{mp}}$, the sum of the transconductances of the N and P devices. It is also possible to force $\{V_\mathrm{P}, V_\Sigma\}$ in a circuit with two identical VCCSs, e.g., two nMOS-FETs [34]. However, this requires additional circuitry, e.g., a voltage buffer driving the low ohmic terminal of a 3-terminal VCCS [35], or a third VCCS [34]. Without such means, this circuit has an input impedance $1/g_m$ which is useful in low noise amplifiers or mixers requiring impedance matching.

C. $\{V_\mathrm{P}, V_\Delta\}$ Circuits

Fig. 10(c) shows a $\{V_\mathrm{P}, V_\Delta\}$ circuit, in which the input voltage source forces again a "primary" VCCS voltage, while the difference of the VCCS-voltages is forced equal to V_Δ. If 3-terminal VCCSs are used, it implements a new 4-terminal transconductor. Note, however, that the lower V_P-voltage terminal is also a current terminal, i.e., it must be connected to ground in practice. The transconductance is equal to the difference of the transconductance values of the two VCCSs. With single transistors, it has been proposed as a transconductor [36]. If two 4-terminal VCCSs are used as a starting point, a 4-terminal VCCS with extended tuning range can be implemented [37].

D. $\{V_\Delta, I_\Sigma\}$ Circuits

Fig. 10(d) shows a $\{V_\Delta, I_\Sigma\}$ circuit, in which the input voltage source forces the difference between the VCCS-voltages to be equal to V_Δ, while the current source forces the sum of the VCCS-currents equal to I_Σ. It implements a 4-terminal VCCS. The transconductance is equal to half the value of the transconductance of a single VCCS, and current I_Σ can be used to tune it. A well-known circuit implementation is the differential pair or long-tailed pair, which has been used a lot in filters [38]. However, any single-ended transconductor can be used instead of a single MOSFET, e.g., a resistively degenerated MOS, or a triode transconductor. A very important advantage of this circuit is its high common mode rejection, due to the current source that isolates the "internal" node from ground. Thus the circuit has two basic mechanisms for common mode rejection, namely isolation and balancing.

E. $\{V_\Sigma, I_\Delta\}$ Circuits

Fig. 10(e) shows a $\{V_\Sigma, I_\Delta\}$ circuit, in which the input voltage forces the sum of the VCCS-voltages equal to V_Σ, and the difference of the VCCS current equal to I_Δ. Usually $I_\Delta = 0$, and we will assume that for simplicity. A well-known implementation is the complementary MOS pair [39]. Other simple examples are stacked nMOS transistors [40] and resistively degenerated MOSFETs (case E+R and S+R).

F. Nested Hierarchical Use of Combination Techniques

It is worth mentioning that the 2-VCCS combination techniques can be used in a nested way at different hierarchical levels. For instance, we can combine a 3-terminal saturated "S-VCCS" with a resistor in a $\{V_\Sigma, I_\Delta\}$ configuration ("S+R" case), while driving two of these structures in a balanced $\{V_\Sigma, V_\Delta\}$ configuration. The analysis of the overall circuit can simply be done by nested analysis at different hierarchical levels. Note that any 3-terminal VCCS implementation can be

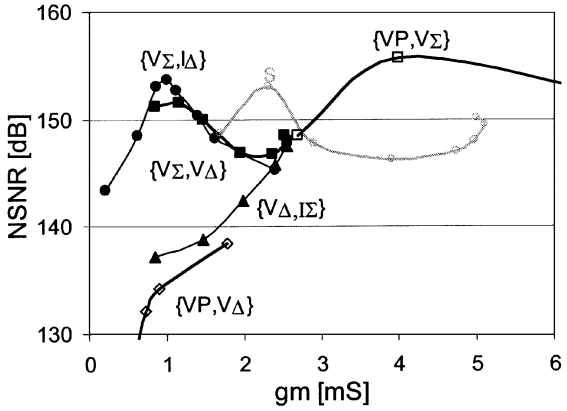

Fig. 11. Simulated NSNR of the 5 classes of composite 2-VCCS *V-I* kernels, using a S-VCCS as building block (included for reference).

used (including a 4-terminal VCCS + wire), resulting in a huge number of possible circuits. Virtually all transconductors that we are aware of, can be considered as consisting of a basic *V–I* kernel discussed in Section IV, combined on higher hierarchical levels using the techniques discussed in Section VI-A–E. For some well-known transconductors, e.g., [34]–[46], examples of the decomposition are given in [9] and a more extensive discussion can be found in [7].

VII. Effect of Two-VCCS Class on Distortion and NSNR

Consider now the effect that of the five classes of two-VCCS combination techniques have on NSNR. Using (7), we need to know the g_m, g_3, NEF, and $P_{\rm dis}$ to calculate NSNR. Table IV gives an overview of the *change* in properties, taking a single VCCS as reference. Moreover, the effect on g_2 [see (3)], which determines the second order distortion, is included. Whenever possible, we assume matched devices for simplicity. To verify the validity of the analysis, simulation results are given in Fig. 11, using an "S-VCCS" as building block and the bias ranges as defined in Section V.

A. $\{V_\Sigma, V_\Delta\}$ Circuits

This class not only renders zero differential output offset current for matched VCCSs, but cancellation of all even order distortion products. Assuming 1% mismatch, second-order of magnitude reduction can typically be achieved. As only half of the differential input voltage is applied to each VCCS, two times more input swing is possible for the same distortion, and g_3 is divided by 8 [substitute $(1/2)V_{\rm in}$ in (3)]. NEF remains unchanged, while $P_{\rm dis}$ is obviously doubled. As can be seen in Fig. 11, the resulting NSNR is the same as for a single VCCS, but at halved transconductance, thus leading to a shift to the left.

B. $\{V_{\rm P}, V_\Sigma\}$ Circuits

Also in this case, the second-order terms of the two VCCSs are subtracted and cancel for identical VCCSs. However, implemented via an nMOS and pMOS, "complementary matching" is required, which is typically approximated by choosing three times wider pMOS transistors compared to the nMOS. In practice process spread will render errors in the order of 10%, which still renders an order of magnitude reduction. As the full input voltage is directly applied to each VCCS, while the output currents are subtracted, the first- and third-order Taylor terms are both doubled, leaving the linear input swing unchanged in the case of complementary matching. NEF also remains equal, and so does the current consumption, as the VCCSs share one bias current. As g_m is doubled, the NSNR is improved by 3 dB (NSNR curve is shifted up and to the right in Fig. 11).

C. $\{V_{\rm P}, V_\Delta\}$ Circuits

For this class, the bias point of the two VCCSs is not equal, with an amount controlled by V_Δ. As a result the output current $i_{\rm out}$ is proportional to the difference of (unequal) Taylor coefficients. The effect on distortion strongly depends on the $I(V)$ characteristic. In general, this will not lead to second-order distortion cancellation, unless the second-order taylor coefficient are equal, despite of the different bias. More importantly, NEF of this class is very poor for small values of V_Δ, as the overall transconductance becomes smaller and smaller (signal subtraction) while the noise of the two VCCSs is added. This leads to very poor NSNR at low g_m, as can be seen in Fig. 11.

D. $\{V_\Delta, I_\Sigma\}$ Circuits

As is well known, this class again features second–order distortion cancellation for matched VCCSs. On the other hand, the third-order Taylor coefficient is a complex function of the $I(V)$ characteristic, and depends both on the third- and second-order coefficient of the single VCCS [7], [33]. This is because the second-order term of the $I(V)$ currents produces a second-order spectral voltage component on the "internal" node of the $\{V_\Delta, I_\Sigma\}$ circuit, which is proportional to g_2/g_1. The second-order term of the VCCS mixes this component with the first harmonic on the gate, resulting in third-order distortion products proportional to g_2^2/g_1, apart from the normal g_3-term. The net result strongly depends on the VCCS characteristic, and especially on the sign of the third-order term. If the sign is positive, as in weak inversion, a lower third-order distortion results. Nonlinearity cancellation is even possible if $g_1 g_3 = 2g_2^2$, for instance via deliberately mismatched pairs [5].

Higher order distortion terms determine the input swing in that case. In the strong inversion, which is more relevant for high frequencies, the second-order term unfortunately has a negative effect on third-order distortion. For newer IC processes the second-order term becomes smaller, which reduces the third-order linearity disadvantage of a differential pair compared to a single S-VCCS. Simulations in Fig. 11 show that the NSNR is 3–12 db worse at halved transconductance.

E. $\{V_\Sigma, I_\Delta\}$ Circuits

Assuming identical devices, the input voltage is divided in two equal parts. Thus, the input voltage can be two-times larger for the same distortion (this holds for both IM2 and IM3), hence g_2 is reduced with a factor 4, and g_3 with a factor 8 compared to a single VCCS. Note that this effect is independent of the VCCS device characteristic, if the devices would be identical. For different devices, e.g., a linear resistor in series with a transistor, the formulas are more complicated [7], [33]. The transconduc-

tance is halved for matched devices, while NEF remains the same. Thus, according to Table IV, we expect 3-dB NSNR improvement. Indeed, in Fig. 11 we see a high value for NSNR at halved transconductance. However, the stacking of devices leads to hard limits in voltage swing, reducing the benefit at low-supply voltages.

VIII. Conclusion

In this paper, we reviewed HF transconductors, focusing on simple circuits with very few internal nodes, which are attractive for high-bandwidth and low-excess phase. The most important contribution of this paper probably lies in the systematic coverage of virtually all published MOSFET *V-I* kernels, and a fair comparison of their relative performance based on the definition of a NSNR. For simple 3-terminal transconductors with one combined voltage-current terminal, the key conclusion is that resistively degenerated saturated MOSFETs operating in strong inversion ("S+R") render the best NSNR, albeit over a very limited transconductance tuning range. Exponential weak inversion devices with degeneration ("E+R") achieve similar NSNR, but require much larger MOSFET devices for the same overall transconductance. If transconductance control is required, switching can be used without loss of NSNR. Gate-driven saturated MOSFETs ("S") also offer good linearity and NSNR. They do allow for significant transconductance tuning, but are more sensitive to changes in the $I(V)$ characteristics expected for future CMOS devices. Bulk-driven saturated devices ("B") in theory achieve the same NSNR at δ times lower transconductance, but less in practice due to bias voltage constraints. Triode transconductors have good linearity and a large tuning range, but bad noise properties in deep triode, resulting in poor NSNR. Exponential devices show poor NSNR mainly because of their strong nonlinearity.

Using two 3-terminal VCCSs, composite *V–I* kernels can be constructed in different ways. Based on a systematic classification technique that covers all 2-VCCS circuits, five essentially different ways of combining VCCSs were identified and analyzed (see Table IV). These VCCS-combination techniques can be used in a nested way, covering virtually all published *V–I* kernels. The $\{V_\Sigma, V_\Delta\}$ technique (e.g., balanced common source pair) renders the same NSNR as a single VCCS, but achieves common mode rejection and even order distortion cancellation. The $\{V_\mathrm{P}, \mathrm{V}_\Sigma\}$ technique (e.g., CMOS inverter) achieves two times better NSNR and two times higher transconductance. The $\{V_\Delta, I_\Sigma\}$ class (e.g., differential pair) renders common mode rejection and even order distortion cancellation. Comparing to a single MOSFET, the overall effect on NSNR depends strongly on the $I(V)$ curve, leading to better NSNR in weak inversion but worse NSNR in strong inversion. $\{V_\mathrm{P}, V_\Delta\}$ circuits have large tuning range, but very poor NSNR due to the subtraction of signals, while adding noise. The $\{V_\Sigma, I_\Delta\}$ class (series connection) can achieve two times better NSNR for "stacked " identical devices at halved transconductance.

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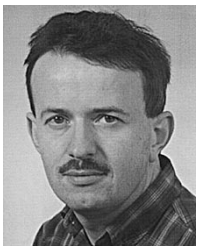

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