Experimental Verification of a Harmonic-Rejection Mixing Concept using Blind Interference Canceling

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***Abstract*— This paper presents the first practical experiments on a harmonic rejection downconverter, which offers up to 75 dB of harmonic rejection, without an RF filter. The downconverter uses a two-stage approach; the first stage is an analog multi-path/multi-phase harmonic rejection mixer followed by a second stage providing additional harmonic rejection based on blind adaptive interference canceling in the discrete-time domain. The aim is to show its functional operation and to find practical performance limitations. Measurement results show that the harmonic rejection of the downconverter is insensitive to frontend nonlinearities and LO phase noise. The canceler cannot cope with DC offsets. The DC offsets are removed by highpass filters. The signal paths used to obtain an estimate of the interference must be designed to provide as much attenuation of the desired signal as possible.**

I. Introduction

Harmonic downmixing is a problem in direct-conversion receivers employing switching mixers. Owing to the harmonic content of the effective local oscillator (LO) waveform, RF signals present at multiples of the LO frequency ω_{LO} appear at baseband together with the desired signal [1], [2]. These RF signals, or *harmonic images*, can be much stronger than the desired signal and can thus cause interference.

This is especially a challenging problem in multi-band receivers such as television tuners [3]. Traditionally, this is solved by removing the harmonic image signals, before they reach the mixer stage, by means of an RF tracking filtering. Such filters are power hungry and it is difficult to design them so that they keep their desired filter shape over a wide range of frequencies.

A different approach to avoid harmonic downmixing is to minimize the harmonic content of the effective LO waveform. By putting multiple switching mixers in parallel and summing their weighted outputs, the effective *aggregate* LO waveform contains less harmonics than a pure square wave. This technique has been successfully used in transmitters [1] and receivers [4] to remove the 3rd and 5th harmonic images. The first uncanceled image is the 7th harmonic image.

In theory, the multipath solution in [4] is able to reject the 3rd and 5th harmonic images completely, but around 30 to 40 dB attenuation has been reported in practice. This limitation is due to the amplitude and phase imbalance between the signal paths, arising from mismatches in component values. Timing errors in the multi-phase LO clock generator also cause imbalances, which further reduce the attenuation of the harmonic images.

Some RF receivers, such as multi-band television tuners and upcoming cognitive radio receivers require more than 90 dB of harmonic rejection. Clearly, the 40 dB offered by the multi-path solution is not enough. In an attempt to solve this problem, we proposed a combined analog-digital technique based on interference canceling to further attenuate a strong harmonic image [5]. The previous work is based on simulations only. Here, we evaluate the properties by measurements on a breadboarded harmonic rejection downconverter circuit. The aim is to demonstrate functionality and to find practical performance limitations.

II. Overview of the Harmonic Rejection System

The harmonic rejection downconverter comprises an analog multi-path mixer built from off-the-shelf components, a four-channel A/D board and PC running the interference cancellation algorithm. The use of off-the-shelf components calls for a down-scaling of the frequencies. The aim is not to produce a circuit that is directly applicable, but to learn about the general circuit properties before designing a high-frequency chip. A system diagram of the downconverter is shown in Fig. 2.

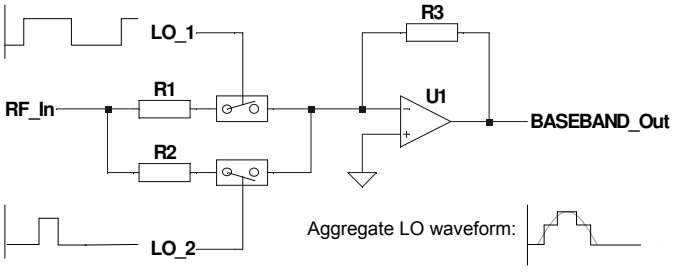

Fig. 1. One half of a differential mixer circuit. The resistors R1 and R2 are used to provide the necessary $1:\sqrt{2}$ weighting ratio of the RF. Also shown is the resulting aggregate LO waveform.

The antenna signal is split into two paths, an I channel and a Q channel. Each channel consists of two 74HC4066-based switching mixers, each with a different LO waveform as indicated in Fig. 2. One half of the switching mixer is shown in Fig. 1. Note that the aggregate LO waveform, which is also shown in Fig. 1, approximates the first half-period of a sine wave. The $1:\sqrt{2}$ weighting ratio is implemented by

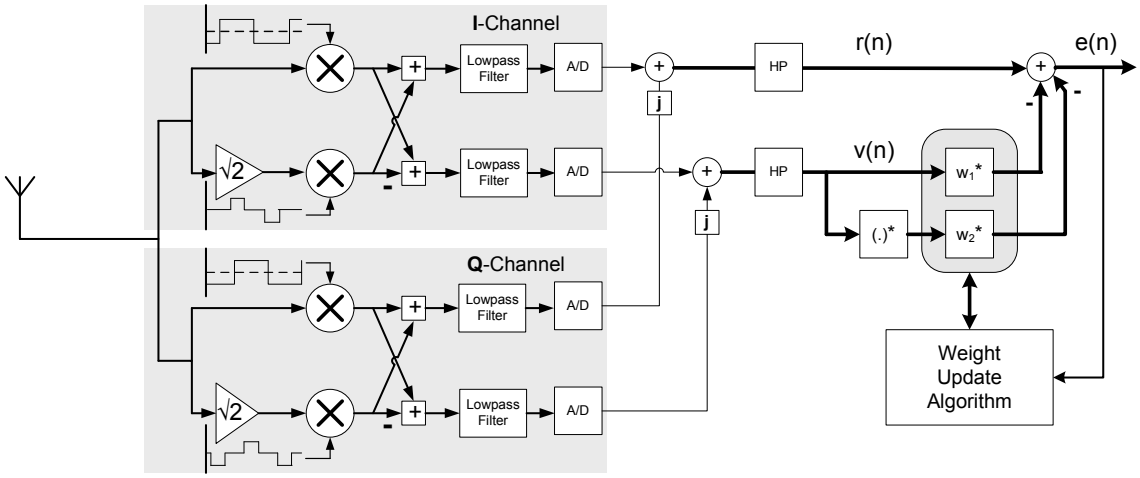

Fig. 2. A two-stage harmonic rejection downconverter.

the resistors R1 and R2. The other half of the switching mixer (which is not shown) takes care of the second half-period of the sine wave.

The output of the mixers are added to form the signal r and subtracted to form the signal v. Both operations are done using CMOS opamps. The addition leads to the rejection of the 3rd and 5th harmonic images leaving the desired signal, while the subtraction leads to the rejection of the desired signal, leaving the aforementioned harmonic images. Amplitude and phase imbalances cause the rejection to be around 30 dB in case of the breadboarded system.

In other words, r contains the desired signal and some residual harmonic image signals, while v contains the harmonic image signals and some residual of the desired signal. In effect, v forms an estimate of the interference contained in r. This fact is exploited by the digital interference canceler.

The multi-phase LO clock generator consists of parallel-loadable 8-bit shift registers (74HC166). Each distinct LO waveform is made by one shift register of which the output is routed to its serial input. The parallel loading feature is used to load the desired switching pattern into the register at startup. The shift registers are clocked at 8 MHz making the base period of the eight-phase clock 1 MHz. Therefore, the downconverter is tuned to 1 MHz, the scaled LO frequency.

The signals are converted to the discrete-time domain by four 12-bit A/D converters (AD9342) running at 500 ksamples/s. Their data streams are read by a PC, which performs the digital signal processing. The 'added' I/Q and 'subtracted' I/Q signals are combined into two complex-valued signals, $r(n)$ and $v(n)$, from which two highpass filters (HP) remove any DC offsets and reduce the LF self-mixing noise.

A. The Interference Canceler

The interference cancellation (IC) algorithm, which is based on least mean squares (LMS) adaptive filter theory [6], consists of two complex weighting coefficients w_1 and w_2, as shown in Fig. 2. The coefficients scale and rotate $v(n)$ and its complex conjugate $v^*(n)$. The need for $v^*(n)$ in the canceler arises from I/Q imbalance in v and r. The reader is referred to [7] for a more thorough treatment on I/Q imbalance and its relation to this complex conjugate.

The IC is performed by the following equation:

$$e(n) = r(n) - w_1^*(n)\, v(n) - w_2^*(n)\, v^*(n) \qquad (1)$$

,where $e(n)$ is the interference-reduced output.

The coefficients $w_1^*(n)$ and $w_2^*(n)$ approach the optimal (LMS) values as n goes to infinity, by applying the following multiple-input single-output (MISO) update algorithm [8]:

$$\begin{aligned} w_1(n+1) &= w_1(n) + \mu\, v(n)\, e^*(n) \\ w_2(n+1) &= w_2(n) + \mu\, v^*(n)\, e^*(n) \end{aligned} \qquad (2)$$

,where $\mu = \frac{10^{-4}}{\sigma_v^2}$ is a learning coefficient and σ_v^2 denotes the power of the interference estimate $v(n)$. The value of μ is small enough that (2) is stable and large enough for rapid convergence. In [5], the algorithm is described in greater detail.

III. Measurements

To show that the HR concept works in practice, the spectrum of $r(n)$ and $e(n)$ were determined. A 1.01 MHz sinusoidal signal of 10 mV peak-peak was used as the desired signal and a 412 mV peak-peak 3.02 MHz sinusoid was used as a third harmonic image; a 32.3 dB power difference. The 412 mV swing was chosen so the nonlinearities of the CMOS switches were below -85 dBFS, where 0 dBFS corresponds to the full-scale of the ADC.

The spectrum of $r(n)$ and $e(n)$ are shown in Fig. 3. The plots were produced by performing a 256-point FFT on $r(n)$ and $e(n)$ after decimation-by-four to reduce the sampling rate to 125kHz. Decimation was needed to meet the real-time constraints of the PC.

The desired signal and 3rd harmonic image appear at -34.8 dBFS (-10 kHz baseband) and -34.0 dbFS (20 kHz baseband) respectively, in $r(n)$. The analog HR stage is able to reduce the 32.3 dB difference to 0.8 dB, indicating a harmonic rejection figure of 31.5 dB. At the output of the canceler, $e(n)$, the third harmonic image signal appears at

-72.2 dBFS. Therefore, the canceler is able to increase the harmonic rejection by 37.4 dB to a total of 68.9 dB.

The spectrum of $e(n)$ shows that the third harmonic image, at $\pm$ 20 kHz, is not completely removed. The interference estimate $v(n)$ not only contains the interference, but also energy from the desired signal due to a finite amount of analog rejection, 28.50 dB in our case. Because of this, the attainable HR by the IC is also limited [9]; less desired signal energy (with respect to the interference energy) in $v(n)$ leads to greater HR of the harmonic image in $e(n)$. Therefore, the analog signal paths used to generate $v(n)$ should be designed to maximize the rejection of the desired signal.

To examine the dependence of the digital rejection on the signal-to-interference (SIR) ratio in $v(n)$, the third harmonic image signal was varied between 800 mVpp and 10 mVpp. The desired signal was kept at 10 mVpp. The same test was repeated for a 5th harmonic image signal at 5.02 MHz. As the SIR of $v(n)$ is related to the SIR of $r(n)$, we need only focus on $r(n)$.

The SIR of $e(n)$ against the SIR of $r(n)$ is shown in Fig. 4. As the SIR of $r(n)$ decreases, owing to a power increase in the third harmonic image, more harmonic image signal energy is present in $v(n)$ while the desired signal's energy remains the same. As the SIR of $r(n)$ decreases, the interference estimate $v(n)$ produces a better estmate. Thus, an increase in rejection is expected in $e(n)$ [5]. This remarkable trend is clearly visible in Fig. 4 for both the 3rd and 5th harmonic images. However, when the SIR of $r(n)$ is more than about 23 dB, the canceler makes the SIR of $e(n)$ worse. This feature can be avoided by bypassing the canceler when there is no improvement. Detecting this situation requires additional knowledge, such as the bit-error rate or signal power estimates. This is a topic for further research.

When the SIR of $r(n)$ is smaller than 0 dB, a droop in the SIR of $e(n)$ is visible. This coincides with an interferer voltage of 412 mVpp or higher, a region where the CMOS switches in the mixer circuit become nonlinear. As a result, the I/Q imbalance in $v(n)$ increases and more desired signal energy is found in $v(n)$. As discussed above, this has a detrimental effect on the harmonic rejection, hence the lower SIR of $e(n)$.

The total harmonic rejection was determined to show the system's performance, see Fig. 5. As expected, the harmonic rejection increases with increased harmonic image power, a favorable trend indeed! The harmonic rejection reaches its maximum when the downconverter becomes nonlinear, indicating resilience to intermodulation products. The maximum harmonic rejection attained by the downconverter is 75.4 dB, its minimum is 13.8 dB. The analog stage offers around 32 dB of rejection, irrespective of the harmonic image power. Switching off the canceler, as suggested above, makes the attainable harmonic rejection range from 32 to 75 dB. Note that the aforementioned range is without an RF filter.

IV. Effect of Circuit Imperfections

Other factors besides the desired signal energy in $v(n)$ determine the signal components at the output of the digital

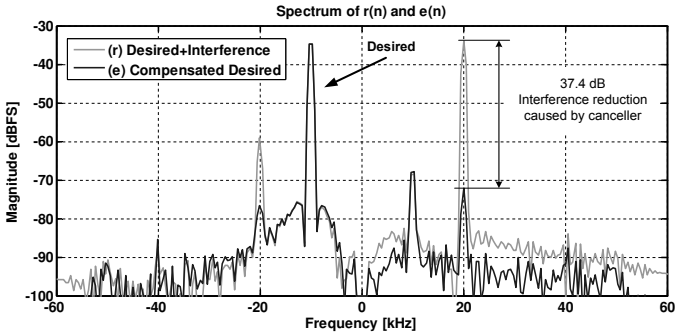

Fig. 3. Magnitude spectrum of $r(n)$ and $e(n)$. The desired signal (1.01 MHz RF, -10 kHz baseband) is 10 mVpp at the antenna, the third harmonic image signal (3.01 MHz RF, 20 kHz baseband) is 412mVpp at the antenna. Both signals are sinusoidal. Decimate-by-four and a 256-point FFT were used to obtain the spectrum.

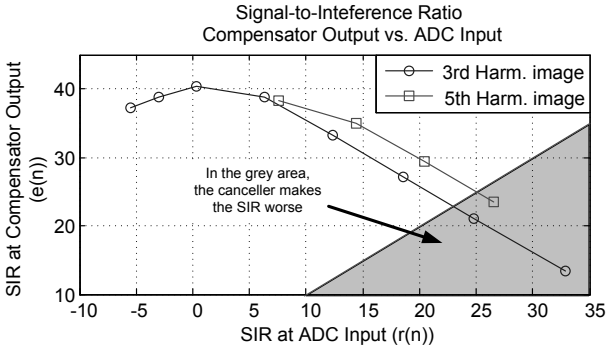

Fig. 4. Signal-to-interference ratio (SIR) of $e(n)$ versus the SIR at the mixer output $r(n)$. The desired signal is 10 mVpp at the antenna, the harmonic image signals are between 10 and 800 mVpp at the antenna. Both signals are sinusoidal.

canceler. Three effects will be considered next; nonlinearities in the mixer frontend, jitter of the LO or A/D sample clock and DC offset & LO leakage.

A. Nonlinearities

When the the frontend is in a blocking condition, i.e. the signals are being clipped or heavily distorted, there is no way to recover the desired signal. However, given mildly nonlinear conditions, intermodulation products that are generated before the mixer, for instance, in an low-noise amplifier, will be rejected when they exist in the same band as the interferer being canceled; thus either in the 3rd or the 5th harmonic image band.

Intermodulation products generated after the mixers are generally not canceled as they are not common among the paths. Luckily, this seperation also ensures that correlation between $r(n)$ and $v(n)$ cannot be attributed to these products. As the coefficients w_1 and w_2 of the digital compensator depend on the correlation between $r(n)$ and $v(n)$, low-level intermodulation products do not affect the performance of the canceler. Note that these products can, of course, cause interference to the desired signal.

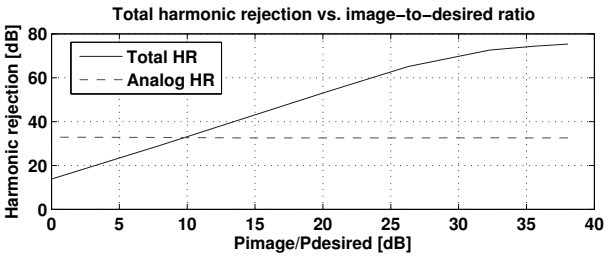

Fig. 5. Total harmonic rejection ratio (analog+digital) against the image-to-desired signal ratio.

B. Jitter of the master clock and A/D sample clock

Jitter of the clock driving the multi-phase LO generator, the master clock, is common to all the shift registers. When we ignore the timing jitter caused by the shift registers themselves, the transitions at the output of the registers share the same timing error. As the mixer clocking patterns are not all equal, this means that high-frequency jitter, i.e. edge-to-edge jitter, is not the same for each mixer, which leads to a decorrelation between $r(n)$ and $v(n)$ caused by phase modulation. The canceler is only able to remove the part common to $r(n)$ and $v(n)$, i.e. the correlating part, leaving the decorrelated part as a residue. Thus, the total harmonic rejection is reduced.

When the first measurements were taken, a function generator was used as the master clock. Its phase noise caused considerable skirting around the desired and harmonic carriers. When the function generator was replaced by a fixed-frequency crystal oscillator, the skirts disappeared but the HR performance remained the same. This points to a certain resilience with respect to phase noise.

Timing jitter of the A/D clock is not a problem for the canceler as the A/D converters share the clock and thus have the same timing error. As a result, there will be no decorrelating effect. However, as is to be expected, A/D clock jitter can cause problems in the carrier or symbol synchronization and decoding parts of the receiver.

C. DC offset and LO leakage

Both DC offset and LO leakage are well-known problems of direct-conversion receivers [10].

A DC offset at the input of the IC algorithm will cause a run-away effect of the filter coefficients, in this case w_1 and w_2. The reason for this is the accumulation that takes place in the coefficient update algorithm (2), in the presence of a DC term.

Direct-conversion receivers suffer from LO self-mixing. Self-mixing causes a slowly time-varying DC offset at the baseband output of the mixers. Energy radiates from the local oscillator and finds its way into the antenna or mixer, thereby mixing with itself to DC.

A practical solution to the DC offset problem is to include digital high-pass filters directly after the A/D converters. However, not all modulation schemes are compatible with a notch at DC. For example, GMSK used in GSM cellphones, has most of its signal energy near DC when the receiver is operated in zero-IF mode.

V. Conclusions

We presented measurements done on a two-stage harmonic rejection downconverter built from off-the-shelf components. The downconverter comprises a multi-path analog mixer, with approximately 32 dB of harmonic rejection, as a first stage and a digital harmonic rejection system based on adaptive blind interference canceling as a second stage.

The inclusion of the digital harmonic rejection stage does not pose any special requirements on the analog circuit other than two additional A/D converters and subtracters. The performance of the harmonic rejection algorithm depends mainly on the quality of the interference estimate $v(n)$. Therefore, careful design of the signal paths used to obtain $v(n)$ with respect to rejection of the desired signal, is advantageous. Frontend nonlinearities do not affect the performance of the digital canceler, but intermodulation products are generally not canceled unless they are generated before the downconverter. The canceler shows some resilitience to LO phase noise but is not capable of handling DC offsets at its inputs. Digital highpass filters are needed to remove these offsets. The harmonic rejection of the downconverter ranges from 32 to 75 dB, depending on the power of the harmonic image. A stronger harmonic image leads to more harmonic rejection; a very favorable trend indeed.

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