17.1 A Discrete-Time Mixing Receiver Architecture with Wideband Harmonic Rejection

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Recently several CMOS software-defined radio (SDR) demonstrators have been presented using mixers as the wideband downconverter [1,2]. Meanwhile, the feasibility of RF samplers as downconverter has also been demonstrated [3,4]. These samplers allow for more discrete-time (DT) and digital signal processing, and are therefore better suited for advanced CMOS technologies. However, samplers suffer from several problems if used in a wideband SDR. Charge sampling [3] gives a conversion gain which is inversely proportional to frequency [5]. Voltage sampling [4] doesn't have this problem, but suffers from wideband noise folding. In both cases, RF pre-filters are needed to prevent interferers around harmonics of the sampling clock from folding back to the baseband. In this paper, we propose a DT harmonic-rejection (HR) mixing architecture that relaxes RF filter requirements and reduces the noise folding.

The proposed SDR downconverter is aimed for the DVB-H standard (470 to 862MHz) and for emerging cognitive radio applications in the 200-to-900MHz band, which suffer from 3rd and 5th harmonic mixing. Figure 17.1.1 shows the architecture of the IC. An inverter-based RF-amplifier (RFA) drives a passive switched-capacitor (SC) core consisting of three stages. The first stage is effectively an oversampler, with $f_s=8f_c$ (f_s is the sampling frequency and f_c is the carrier frequency). The second stage consists of I/Q DT mixers for downconversion. The third stage is a low-pass IIR filter. The zero-IF quadrature outputs are buffered via source followers. A clock generator is implemented using a divide-by-4 circuit and NOR gates to generate 8-phase 12.5%-duty-cycle full-swing clocks to drive the sampling circuitry. An external sinusoidal differential master clock is used with a frequency of $4f_c$. Note that an LNA is not included in this design.

Figure 17.1.2 illustrates how the DT HR mixer works. Since the sampling rate is $f_s=8f_c$, the 7th harmonic folds to f_c, and the 5th harmonic folds to $3f_c$, etc. Two DT I/Q mixers multiply the incoming samples with a DT cosine and sine wave, i.e., weighting factors of 1 and $(1+\sqrt{2})$ (cosine and sine with frequency f_c sampled at $8f_c$). Since the DT clock is periodic, its spectrum only contains an impulse at f_c. Multiplying the oversampled signal with the DT clock will downconvert the signal from f_c to DC without folding harmonics at $2f_c$, $3f_c$, and $4f_c$. However, the harmonics already folded to f_c during the oversampling process cannot be differentiated from the wanted signal. These undistinguishable RF images are located at $(k\bullet n\pm1)f_c$ ($k=1,2,3\ldots$; and $n=f_s/f_c$). If n=8, the un-suppressed RF images are the 7th, 9th, 15th, 17th, … harmonics, but the problematic 3rd and 5th harmonics are cancelled. The DT cosine and sine waves have a 90° phase difference, which, similar to a continuous-time mixer, transfers the phase of the RF input signal to IF. In contrast to the case with an approximation by a time delay [3,4], which is only exact for one frequency [5], the 90° phase shift by DT I/Q mixing is frequency independent leading to a true wideband image rejection. Furthermore, the HR mixing also suppresses noise around harmonics, and hence reduces noise folding. In simulation, a 3dB NF improvement is observed, which intuitively makes sense since half of the odd-order harmonic folded noise components are suppressed.

Figure 17.1.3 shows the SC core circuitry. For clarity only half of the fully differential system is shown. Eight interleaved sampling cells are controlled by 8-phase non-overlapping clocks, with CLK_{in} for the sampling function and CLK_{out} for the mixing function. Each of the 8-phase clocks has a sample rate of f_c, and altogether an effective sample rate of $8f_c$ is achieved. In each sampling cell, there are two weighted sampling capacitors. To reliably make an non-integer $1:(1+\sqrt{2})$ ratio in layout is difficult. We use unit capacitor C_{su} with a 2:5 ratio as an approximation, which is theoretically sufficient for 35dB 3rd and 5th-order HR assuming 1° phase error. Second-order effects such as charge sharing and gain roll-off can give several dBs extra. Although 5:12 would be more accurate, gain errors still don't dominate over the phase errors originating from clock timing mismatches. The DT mixing function is implemented via a systematic combination of the output switches, to transfer charges from sampling capacitors to buffer capacitors (C_b). The charge sharing between the sampling and buffer capacitors implements a low-pass IIR filter [3]. The outputs can be decimated, e.g., via a moving average [3], to a lower sample rate and the next stages can use further DT signal processing as done in [3].

Figure 17.1.7 shows a micrograph of the chip that is fabricated in a 65nm CMOS process. The chip occupies an active area of $0.36mm^2$. Figure 17.1.4 shows the measured gain and SSB NF over the RF band. At the low side, AC coupling limits the gain and at the high end the clock-circuitry speed limit of 3.6GHz is reached. Due to the varying gain, the SSB NF ranges from 12dB to 19dB, which is 20dB better than [4] and is the lowest among all voltage-sampling mixers discussed in [6].

In literature, a continuous-time HR mixer for transmitters is proposed in [7], and a 2MHz IF HR sampler in [8], both using weighted amplifiers. We exploit weighted capacitors which can have superior matching properties, and only need one RF amplifier, while still generating quadrature IF signals. The same number of clock phases is needed for the proposed architecture and that of [7] and [8], and therefore, there is no extra cost on clock speed.

A good HR ratio over a wide channel BW is important for wideband standards and for future cognitive radio applications which might use multiple segments of free spectrum spreading over a wide band. It is also important to reduce the distortions caused by strong out-of-channel interferes. In [8], the IF HR sampler is implemented by summing the sampled data. This operation is equivalent to using a FIR filter to reject harmonics, which is only effective for a limited channel BW due to the limited notch BW inherent in any FIR filter. DT mixing, however, does not have this limitation. In Figure 17.1.5, the upper plot shows the HR ratio for a sampler using FIR filter drops significantly over the channel, while the proposed architecture gives wideband HR without channel BW limitation. The trend of the measured results is in good agreement with the simulated results. However, phase and gain mismatches limit the achievable HR ratio (not considered in the simulation results).

The lower plot in Figure 17.1.5 shows the measured results for the HR ratio over the RF band, averaged over 10 chips (σ=5dB). On average, the 3rd-order HR ratio from 0.5 to 0.8GHz and the 5th-order HR ratio from 0.3 to 0.9GHz reach around 40dB, which is comparable to the state-of-the-art continuous time HR mixer for RF receivers reported at only one frequency [1].

Figure 17.1.6 summarizes the measured parameters. The noise and linearity performances are competitive with those of continuous-time mixers at reasonable power consumption, which shows the feasibility of the proposed architecture for a practical receiver front-end.

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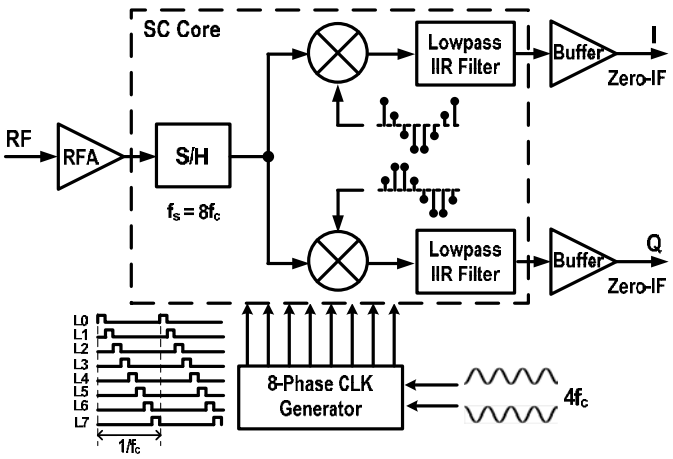

Figure 17.1.1: Architecture of the HR sampling downconverter IC using the proposed DT mixing technique. All blocks are implemented on chip.

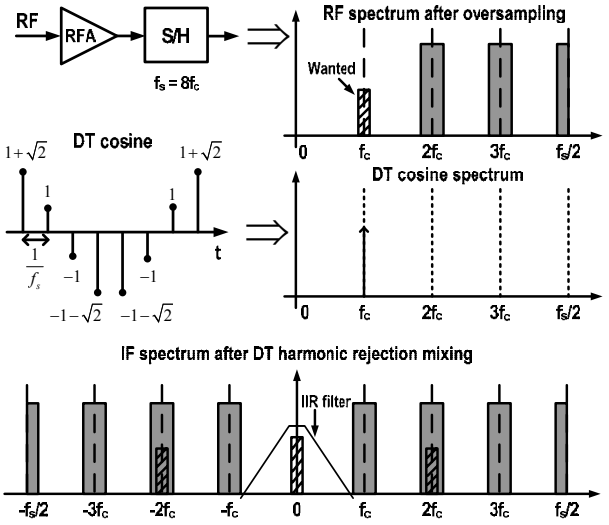

Figure 17.1.2: Illustration of the DT harmonic-rejection mixing mechanism.

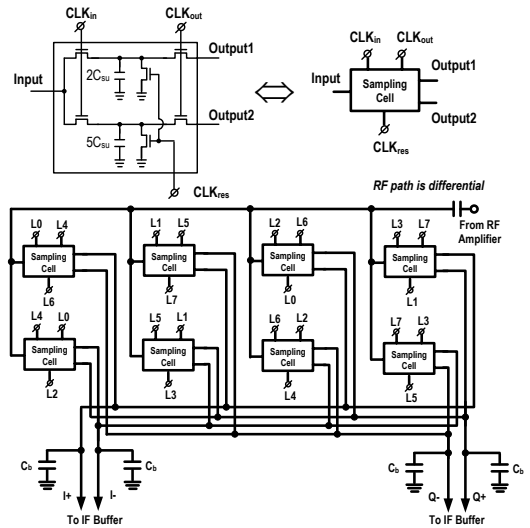

Figure 17.1.3: Switched-capacitor core circuitry of the harmonic-rejection sampling downconverter, with the clock scheme L0 to L7 shown in Fig. 17.1.1.

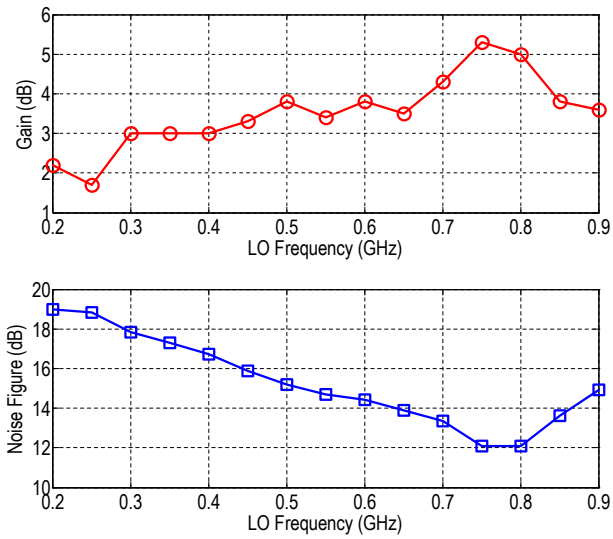

Figure 17.1.4: Gain and SSB NF over the RF band. Both gain and noise data are measured at 1MHz IF.

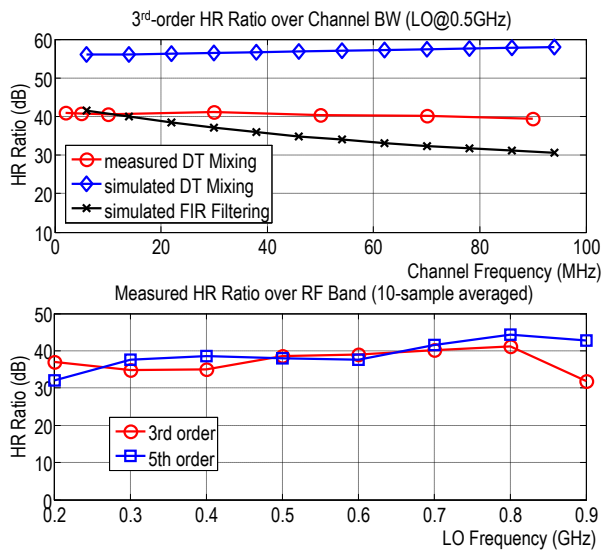

Figure 17.1.5: Harmonic rejection ratio over channel and RF band.

Frequency Range (GHz)	0.2 to 0.9
Gain (dB) @ 1MHz IF	Min: 1.7 Max: 5.3
SSB NF (dB) @ 1MHz IF	Min: 12 Max: 19
IIP3 (503 & 504MHz)	+11dBm
IIP2 (503 & 504MHz)	+43dBm
1/f noise corner	250kHz
IF bandwidth	10MHz

Supply voltage	1.2V
Current drawn (mA)	RFA & Buffer: 5.3
	Clock generator: 7.8@0.2GHz LO 10.6@0.9GHz LO

Harmonic-rejection ratio (10-sample averaged)	
3rd-order (0.2 to 0.9GHz)	Min: 32dB Max: 41dB
5th-order (0.2 to 0.9GHz)	Min: 32dB Max: 44dB

Figure 17.1.6: Measured key parameters.

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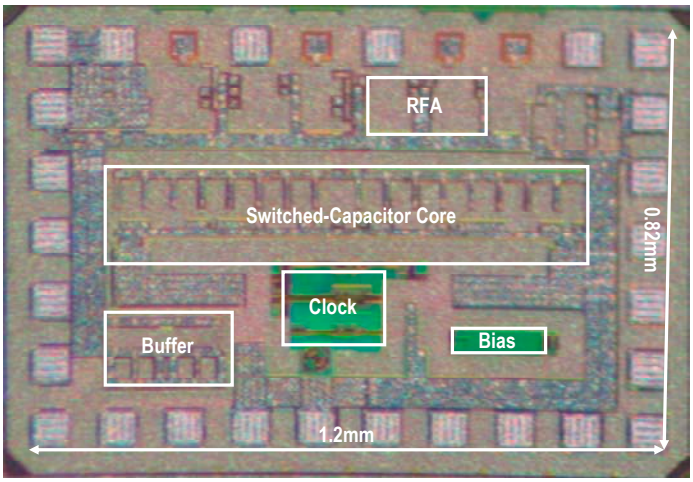

Figure 17.1.7: Micrograph of the chip fabricated in 65nm CMOS. The 0.36mm² active area includes all the blocks shown in Figure 17.1.1 and the bias current sources.

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