On the Suitability of Discrete-Time Receivers for Software-Defined Radio

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***Abstract*—CMOS radio receiver architectures, based on radio frequency (RF) sampling followed by discrete-time (D-T) signal processing via switched-capacitor circuits, have recently been proposed for dedicated radio standards. This paper explores the suitability of such D-T receivers for highly flexible software-defined radio (SDR) receivers. Via symbolic analysis and simulations we analyze the properties of D-T receivers, and show that at least three challenges exist to make a D-T receiver work for SDR: 1) the sampling clock frequency is related to the radio frequency, complicating baseband filter design; 2) a frequency-dependent phase shift is introduced by pseudo-quadrature and pseudo-differential sampling; 3) the conversion gain of a charge sampling front-end is strongly frequency-dependent. Compared to a mixer based radio receiver, extra costs are needed to solve these problems.**

I. INTRODUCTION

Recently, the feasibility of CMOS D-T radio receivers using RF sampling has been demonstrated for Bluetooth [1], GSM/GPRS [2] and WLAN [3]. As shown in Fig. 1, the main analog blocks of a typical D-T receiver are an RF pre-select filter, a low-noise amplifier (LNA), a track/hold (T/H) stage, a chain of switched-capacitor (S-C) circuits for bandwidth reduction and decimation, an intermediate-frequency amplifier (IFA), and an analog-to-digital converter (ADC). D-T receivers can be categorized based on their T/H structures as *charge sampling* [1, 2] or *voltage sampling* [3]. Briefly speaking, the main difference is that, charge sampling integrates current and samples charge, while voltage sampling samples voltage. As well known, voltage sampling often seriously suffers from noise-and-interference aliasing, and the suppression of the alias bands heavily relies on the RF pre-select filter. On the other hand, due to the integration effect of charge sampling, there is a *SINC* transfer function on the input spectrum, attenuating the aliasing [4].

A D-T receiver may offer some advantages compared to a continuous-time (C-T) architecture in a deep submicron digital CMOS process, e.g. due to the excellent component matching of capacitors [5] and the programmability to account for spread in process, voltage and temperature (PVT) and imperfections in simulation models [6].

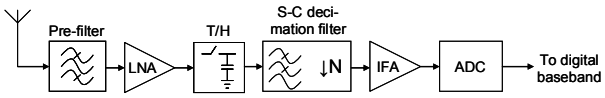

Figure 1. Analog part of a D-T receiver

These properties and especially the programmability feature can be very attractive for SDR applications. Therefore, this paper examines the suitability of D-T receivers for SDR, which has not yet been discussed in publications to our best knowledge. We will analyze the signal processing in a D-T receiver and show that it has some fundamentally different properties than traditional continuous-time receivers. This poses some challenges to the feasibility of D-T receivers for SDR. Section II, III, and IV will discuss three specific challenges. Conclusions are drawn in section V.

II. RF RELATED BASEBAND SAMPLE RATE

An ideal software radio (SR) samples and quantizes the antenna signal directly, and processes the samples in the digital domain to achieve maximum flexibility. Technically this is still far from feasible for high dynamic range GHz radio signals. Still, the utopian SR is a useful starting point to think about highly flexible SDR receivers programmable by software to suit a wide range of different radio applications. For an ideal SR, the sampling clock is an "auxiliary signal" which should not affect the radio reception, nor should the radio performance be dependent on the radio frequency. Assuming the clock rate of the T/H and the ADC in a SR is high enough to satisfy the Nyquist criterion, the sampling process does not cause any frequency downconversion.

In the proposed D-T receivers with RF sampling [1, 2, 3], the RF signal is downconverted to IF at the same time with sampling. The speed of the D-T analog baseband signal processing, e.g. finite-impulse-response (FIR) or infinite-impulse-response (IIR) filtering, and decimation, is thus connected to the RF sampling speed. This poses unwanted constraints on the filter. For example, for FIR and IIR filtering, the filter cut-off frequency scales with the sample rate, which is now related to the RF. Tuning to another

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channel thus changes the filter bandwidth! In a SDR application, the baseband-filter bandwidth should preferably be free to choose, either for the channel-select function or for the anti-aliasing function before A/D conversion.

To alleviate this problem, more complex D-T analog baseband blocks can be used, e.g. programmable capacitor arrays to tune the bandwidth of the IIR filter [2]. Furthermore, for an accurate demodulation it is important to have the sample rate connected to the symbol rate. Since the whole analog baseband including the ADC works at a sample rate connected to the RF, a re-sampling block in digital baseband is needed for sample-rate conversion [1, 2], which can be quite power hungry.

The receiver presented in [7] also applies charge sampling and discrete-time FIR and IIR filtering, but now after downconversion via a mixer. As the T/H stage operates at baseband, the sample rate can be chosen freely to adapt the channel bandwidth or symbol rate, as desired for SDR.

III. FREQUENCY-DEPENDENT PHASE SHIFT

In this section, frequency-dependent phase shift due to time-delayed sampling in D-T receivers will be discussed. This problem exists in both charge sampling and voltage sampling receivers.

As shown in Fig. 2, a pseudo-quadrature sampler, used in [1, 2, 3], multiplies the same input signal $x(t)$ with two different series of sampling impulses, with a delay of $T_s/4$ between each other, where T_s is the period of local oscillator (LO) signal. This procedure is also known as periodically nonuniform sampling of second order [8]. Here we will present an analysis from a circuit designer's viewpoint.

The sampled outputs in Fig. 2 are $x(nT_s)$ and $x(nT_s+T_s/4)$. For the digital baseband demodulation of amplitude and phase, a pair of I/Q samples will be treated as one complex sample. A complex sample can be written as

$$y_C(n) = y_I(n) + j \cdot y_Q(n) \cdot \tag{1}$$

From (1), we can see a complex sample $y_C(n)$ consists of a pair of I/Q samples, $y_I(n)$ and $y_Q(n)$, which corresponds to $x(nT_s)$ and $x(nT_s+T_s/4)$ respectively. Thus the timing difference of $T_s/4$ is removed, which can be modeled as a synchronizer (Fig. 2).

To generate an arbitrary-phase-shifted sample stream, a generalized analysis for a sampling system with a delay of Δt can be applied. If $0 \bullet \Delta t < T_s$, we have the two equivalent

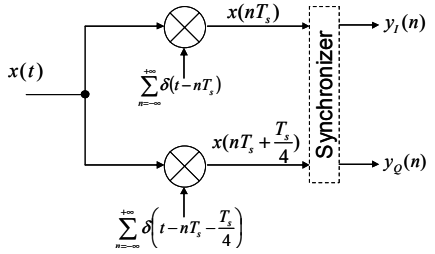
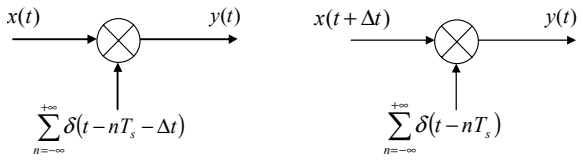


Figure 2. A pseudo-quadrature sampler



(a) (b)

Figure 3. Two equivalent general models for delayed sampling: (a) delayed sampling impulses; (b) delayed input signal.

sampling models in Fig. 3 (a) and (b). Due to the synchronization, the delay of Δt can be shifted from the sampling impulses $(t-nT_s-\Delta t)$ in Fig. 3 (a) to the input signal $x(t+\Delta t)$ in Fig. 3 (b), enabling the following analysis. Based on Fig. 3 (b), the output signal $y(t)$ can be written as

$$y(t) = x(t+\Delta t) \cdot \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \cdot \tag{2}$$

Taking the Fourier transform of (2), we get

$$Y(f) = \left[X(f) \cdot e^{j2\pi \cdot f \cdot \Delta t}\right] * \left[\frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \delta(f - nf_s)\right]. \tag{3}$$
$$= \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \left[X(f - nf_s) \cdot e^{j2\pi \cdot (f - nf_s) \cdot \Delta t}\right]$$

The symbol * denotes the convolution. In (3), it should be noticed that the convolution in frequency domain will fold the input spectrum $X(f) \cdot \exp(j2\,f \cdot \Delta t)$ but will not change its magnitude and phase. Therefore the phase shift of $y(t)$ is equal to that of $x(t+\Delta t)$, which can be written as

$$\Delta\varphi = 2\pi \cdot f_{in} \cdot \Delta t \cdot \tag{4}$$

From (4), we can see the phase shift of the sampled output is proportional to the input frequency (f_{in}) and the sampling delay (Δt). On the other hand, if using a mixer to generate the phase shift, the result would be $\Delta\varphi = 2\pi \cdot f_s \cdot \Delta t$ (f_s is the LO frequency), for the output signal that is downconverted by the fundamental harmonic of the LO. Note that the phase shift generated by a mixer is not systematically dependent on the input frequency but the phase shift generated by a sampler is!

Fig. 4 compares the theoretical results based on (4) with the simulated results. Ideal components are used during the simulation with the following settings: $f_s = 1GHz$, and $\Delta t = 250ps$. From the figure we can see the simulated results match with the theoretical results very well. If we want to generate a phase shift of $\Delta\varphi$ using an LO signal with a delay of Δt, the resulted phase shift will only be accurate at some specific input frequencies satisfying

$$f_k = \frac{\Delta\varphi}{2\pi \cdot \Delta t} + \frac{k}{\Delta t} \quad (k \text{ is integer}), \tag{5}$$

and present frequency-dependent phase errors at other input frequencies. Generally, at frequency $f_k + \Delta f$, the phase error is

$$\varphi_e = 2\pi \cdot (f_k + \Delta f) \cdot \Delta t - \Delta\varphi = 2\pi \cdot \Delta f \cdot \Delta t \cdot \tag{6}$$

From (6), we can see that a larger frequency offset (Δf) or a larger time delay (Δt) gives a larger phase error (φ_e).

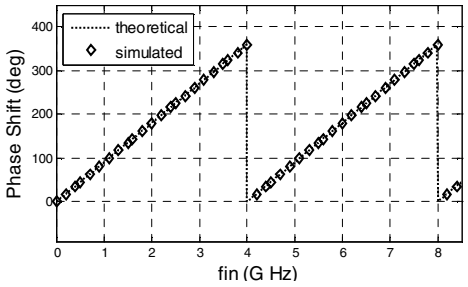


Figure 4. Phase shift with synchronized output (f_s=*1GHz*, and Δt=*250ps*)

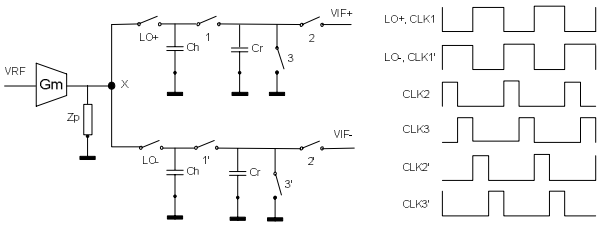


Figure 5. An RF charge sampler with an example of clock scheme

Due to the presented systematic phase error, the sampler in Fig. 2 is called ''pseudo-quadrature'' sampler. It should be noticed that the frequency-dependent phase error not only occurs for pseudo-quadrature sampling, but also for pseudo-differential sampling. Thus the D-T receivers presented in [1, 2, 3] all have this property. At GHz frequencies and a few MHz channel bandwidth, the error can still be acceptable without correction, but for lower RF it easily becomes several degrees. Since the error pattern is known as (6), it should be possible to correct this error in the digital domain [9]. But this will add extra costs.

IV. FREQUENCY-DEPENDENT CONVERSION GAIN

This section will discuss a fundamental challenge if using a charge sampler as downconverter for a SDR receiver. A typical RF charge sampler is shown in Fig. 5, consisting of transconductor (G_m), pseudo-differential T/H stages with a pair of history capacitors (C_h) and rotating capacitors (C_r) [5]. Impedance Z_p models the finite output impedance of G_m together with all the parasitic impedance at node X. The clock scheme has been designed without decimation, so all the switches are switched at the same frequency as the LO, i.e. f_s. In Fig. 5, the pseudo-differential sampling paths are driven by the clock *LO*+ and the clock *LO*- respectively.

In this paper, the conversion gain refers specifically to the voltage-to-voltage conversion gain. For an ideal RF charge sampler with infinite Z_p, its conversion gain has been investigated by [5]. We summarize the result here as

$$CG_{id} = \frac{v_{if,diff}}{v_{rf}} = \frac{2}{\pi} \cdot \frac{G_m}{f_s C_r} \cdot \tag{7}$$

Equation (7) is based on two assumptions: 1) zero-IF sampling, i.e. an LO frequency (f_s) equal to the frequency of the input signal (f_{in}); 2) 50% duty cycle for the LO. From (7), it should be clear that the conversion gain is inversely proportional to f_s, which is equal to f_{in} for zero-IF sampling. Compared to an active mixer with a load resistance R_L, the conversion gain is $(2/\pi)G_mR_L$, which is not systematically dependent on f_{in}. The frequency dependence in (7) is due to the integration feature of a charge sampler. This systematic frequency dependence is undesired for a wide-band receiver such as a SDR receiver.

In [5], a technique called temporal moving averaging (MA) is introduced which might be a solution. The temporal MA is the temporal integration of N RF-samples, performing a FIR operation with N all-one coefficients and an N-times decimation. N can be defined as the decimation ratio. The charge accumulation over N samples does result in a larger conversion gain. Ideally, the gain in case of accumulation of N samples is equal to N, so

$$CG_{id,N} = N \cdot \frac{2}{\pi} \cdot \frac{G_m}{f_s C_r} \cdot \tag{8}$$

From (8), we can see an N-times increase of input frequency might be compensated by an N-times temporal MA to keep the conversion gain stable. However, temporal MA suffers from at least two problems.

First, due to the fact that the MA output is read out via Cr at an N-times lower rate, i.e. f_s/N, there is additional aliasing with a fold-over frequency at $f_s/(2N)$. Although the intrinsic FIR filter in a MA generates notches to suppress the aliasing of noise and interference, the notch width is limited by N, i.e. a smaller N gives wider notches [5]. Circuit imperfections, such as the parasitics at node X, also limit the achievable notch depth [5]. Therefore, an RF pre-select filter is often needed to achieve sufficient alias suppression around the frequency points of $n\cdot(f_s/N)$ ($n=0,1,2,3\ldots$, *but* $n\neq N$), which will limit the flexibility for a SDR receiver.

Secondly, a finite Z_p causes a loss of gain as charge from C_h constantly leaks out every LO cycle. Therefore, it is important to understand how a finite Z_p affects the conversion gain.

If Z_p is capacitive, it can be modeled as a capacitor C_p connected from node X to ground. Both C_p and C_r share the charge with C_h every LO cycle. If the charge on C_p is stored, there will be a charge crosstalk between the pseudo-differential paths: in an LO cycle when switching from the positive path driven by *LO*+ to the negative path driven by *LO*-, the charge from positive path that has been stored on C_p will cancel one part of the charge on negative path, after which another part of the charge from negative path will be stored on C_p to cancel charge on positive path in the next LO cycle. If we focus on the signal downconverted from RF to DC, the amount of signal charge that is shared by C_p with the charge crosstalk effectively doubles the amount shared by C_p without the charge crosstalk. Therefore, due to this charge crosstalk, the effective value of C_p is doubled.

If Z_P is resistive, it can be modeled as a resistor R_p connected from node X to ground. One step further, R_p can be

modeled as an equivalent switched-capacitor resistor with a capacitor C_{Rp} operating at the same frequency with LO, i.e. f_s. Since R_p only connects to C_h and C_r in either positive or negative path for half of the LO period, we have the equivalent capacitor $C_{Rp}=0.5/(R_p f_s)$. Different from a real capacitor, the equivalent capacitor C_{Rp} does not cause any charge crosstalk, because R_p can not store charge.

Using the above analysis, it should not be difficult to derive that when both C_p and R_p are present, the non-ideal conversion gain can be written as

$$CG_{nid} = \frac{2}{\pi} \cdot \frac{G_m}{f_s(C_r + 2C_p) + 1/(2R_p)}. \quad (9)$$

From (9), we can see that at low frequency R_p will dominate the parasitic effect and at high frequency C_p will dominate. It can also be seen that the conversion gain is just the same to an active mixer loaded with three equivalent resistors in parallel, i.e. $1/(f_s C_r)$, $1/(2f_s C_p)$, and $2R_p$. With this intuition, for N-times temporal MA, we can view the RF charge sampler as a mixer loaded by $1/(f_s C_r/N)$, $1/(2f_s C_p)$, and $2R_p$ in parallel. Then the conversion gain, considering the parasitic effects and the decimation, can be written as

$$CG_{nid,N} = \frac{2}{\pi} \cdot \frac{G_m}{(f_s/N)C_r + f_s \cdot 2C_p + 1/(2R_p)}. \quad (10)$$

From (10), it should be clear that the conversion gain is strongly dependent on the sampling frequency, which is equal to the input RF (in the case of zero-IF sampling).

If a charge leakage ratio is defined as

$$\alpha_N = \left(1 + \frac{C_r/N}{2C_p + 1/(2f_s R_p)}\right)^{-1}, \quad (11)$$

equation (8) and (10) can be connected via this ratio:

$$CG_{nid,N} = CG_{id,N} \cdot (1 - \alpha_N). \quad (12)$$

Thus, to get closest to the ideal conversion gain, we need to minimize the charge leakage ratio α_N.

To verify the analysis, the circuit in Fig. 5 has been simulated, with the following settings: $G_m=20mS$, $C_h=10pF$, $C_r=500fF$. A buffer capacitor $C_b=10pF$ is added at the output of each pseudo-differential path to store the charge, and it will not change the conversion gain. Fig. 6 shows the conversion gain versus the decimation ratio (N) at *2.4GHz*, for ideal and non-ideal RF charge sampler based on (8) and (10) respectively. Two sets of non-ideal configuration have been simulated, one set is $R_p = 100K\Omega$ and $C_p=1fF$, which corresponds to a charge leakage ratio of roughly *1%* when $N=1$; the other set is $R_p=10K\Omega$, and $C_p=10fF$, which corresponds to a charge leakage ratio of roughly *10%* when $N=1$. Fig. 6 shows the simulated results match the theoretical results very well.

Equation (10) also suggests we can tune the parameters such as G_m, C_r, C_p, R_p, or N to compensate for the dependence on f_s. For example, we can make a bank of transconductors which is programmable via switches. The whole frequency range of input signal can be divided into several sub-bands. The activated G_m can be tuned for different sub-bands to keep the conversion gain almost flat. Similarly, programmable C_p or C_r can also be used.

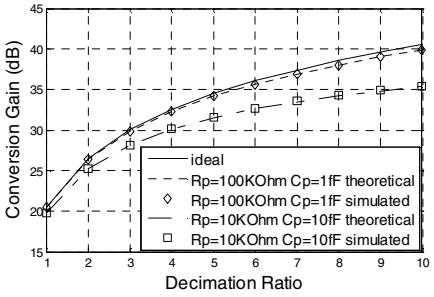


Figure 6. Conversion gain of RF charge sampler at 2.4GHz

V. CONCLUSION

In this paper, we examined the suitability of a D-T receiver with RF sampling to realize a SDR receiver. We identified three challenges. Firstly, we showed the sample rate is directly related to the RF, complicating baseband filter design. Secondly, a frequency-dependent phase shift is introduced by pseudo-quadrature and pseudo-differential sampling. Finally, the conversion gain of a charge sampling front-end is strongly frequency-dependent. All the mentioned effects render frequency-dependent radio receiver properties, which are functionally not desired. To correct these variations, extra costs have to be made.

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