A Polyphase Multipath Technique for Software-Defined Radio Transmitters

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***Abstract*—Transmitter circuits using large signal swings and hard-switched mixers are power-efficient, but also produce unwanted harmonics and sidebands, which are commonly removed using dedicated filters. This paper presents a polyphase multipath technique to relax or eliminate filters by canceling a multitude of harmonics and sidebands. Using this technique, a wideband and flexible power upconverter with a clean output spectrum is realized in 0.13-μm CMOS, aiming at a software-defined radio application. Prototype chips operate from DC to 2.4 GHz with spurs smaller than −40 dBc up to the 17th harmonic (18-path mode) or 5th harmonic (6-path mode) of the transmit frequency, without tuning or calibration. The transmitter delivers 8 mW of power to a 100-Ω load (2.54 $V_{pp\text{-}diff}$ voltage swing) and the complete chip consumes 228 mW from a 1.2-V supply. It uses no filters, but only digital circuits and mixers.**

***Index Terms*—CMOS, cognitive radio, communication, distortion cancellation, harmonic rejection, image rejection, mixer, multipath, nonlinear circuits, polyphase, power upconverter, radio transmitter, software-defined radio, software radio.**

I. Introduction

IN RECENT years, explosive growth in the wireless market has led to wireless transceiver terminals that have multiple applications and cover multiple standards. For consumer products, low price and small form factor are of primary importance, which is typically achieved by increasing the level of integration, and reducing the number of external discrete components. Generally in a wireless transmitter, filters are the main discrete components and those filters are considered inevitable to suppress the strong harmonics and sideband products generated during the mixing and amplification process.

Fig. 1(a) shows a typical multi-standard transmitter, with multiple narrow-band Power Amplifiers (PA) which are limited in bandwidth by *dedicated filters*, one for each standard, selectable by a switch. With the ever increasing number of different standards to be supported, this architecture becomes increasingly unpractical, as support for every new frequency band requires *adding external dedicated components*. In this paper, we aim at a much more flexible architecture as shown in Fig. 1(b): one wideband integrated power upconverter with no dedicated external filters, with a digitally controlled output spectrum. Taking a visionary viewpoint, we aim for "the holy grail of software radio" [2], [3]. Of course, dedicated filters

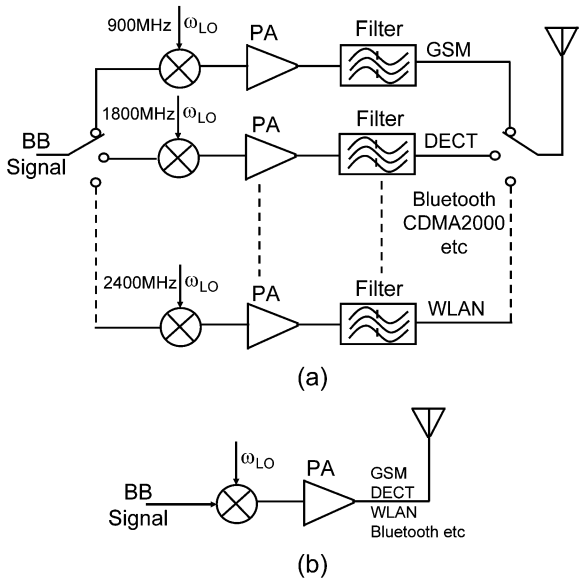

Fig. 1. (a) Conventional multi-standard transmitter architecture. (b) Software-defined radio dream: one flexible upconverter with no filters.

are there for a good reason. However, if we can significantly reduce unwanted spectral components via other more flexible techniques than frequency selective filters, this is likely to be a crucial step to new more flexible transmitter architectures. A recent step in this direction is the use of zero-order hold filtering in a mixer-DAC [4] to reduce DAC related spurs. However, this approach does not address the problem of mixer harmonics around odd LO-harmonics, caused by multiplication with a square-wave LO-signal (hard switching mixer). A harmonic rejection mixer canceling the third and fifth harmonics [5] does relax analog filter requirements. In the current paper, we exploit the polyphase multipath circuit theory recently proposed in [6], to further reduce or even completely eliminate filters by canceling a very large multitude of harmonics and sidebands. We apply the technique to realize a wideband *filterless* power upconverter [1], using only digital circuits and switched transconductor mixers [7]. Compared to previous work, this paper adds a detailed analysis of the polyphase multipath technique, and an extensive discussion on the operating principle and design considerations for the CMOS power upconverter. In this paper, we mainly focused on a proof-of-concept of the polyphase multipath technique and did not aim for any particular standard.

The paper is organized as follows. In Section II, the principle behind the rejection of harmonics and sidebands using the polyphase multipath technique [6] is explained intuitively. An

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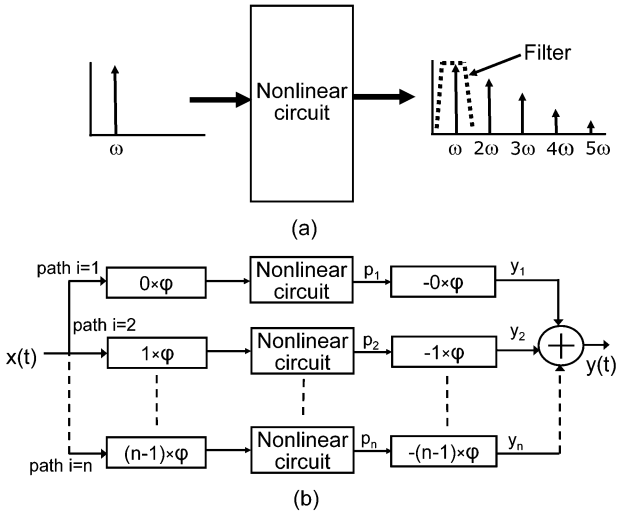

Fig. 2. (a) Nonlinear circuit (1-path). (b) Polyphase n-path circuit.

implementation of this technique aiming at a filterless power upconverter and various design considerations are discussed in Section III. Measurement results are presented in Section IV, and conclusions are drawn in Section V.

II. Polyphase Multipath Technique

A. Basic Principle of Harmonic Cancellation

Fig. 2(a) shows a nonlinear circuit excited by a single sinewave at ω, producing a wanted output signal at ω but also unwanted harmonic distortion at 2ω, 3ω, 4ω, etc. Fig. 2(b) shows a polyphase n-path circuit, cancelling many harmonics of ω [6]. The basic idea is to divide the nonlinear circuit in Fig. 2(a) into n equal smaller pieces, and apply an equal but opposite phase shift before and after each nonlinear circuit. If the phase shift in path i is $(i-1)\times\phi$, where ϕ is a phase shift constant satisfying $n\times\phi = 360^\circ$, the circuit will produce the same wanted harmonic as Fig. 2(a), but cancel many higher harmonics. Mathematically, this can be shown using a power series expansion, assuming a memoryless weakly nonlinear system. If the signal $x(t) = A\cos(\omega t)$ is applied to the input, the output of the *nonlinear circuit* of the ith path can be written as

$$p_i(t) = b_0 + b_1\cos(\omega t + (i-1)\varphi) + b_2\cos(2\omega t + 2(i-1)\varphi) + b_3\cos(3\omega t + 3(i-1)\varphi) + \cdots \quad (1)$$

where $b_0, b_1, b_2, b_3, \ldots$ are constants. From (1), it can be seen that the phase of the kth harmonic at the output of the nonlinear circuit rotates by k times the input phase $(i-1)\phi$. The phase shifters, $-(i-1)\phi$, after the nonlinear blocks are required to align the fundamental components at ω in phase again. The signals at the output of these phase shifters can be written as

$$y_i(t) = b_0 + b_1\cos(\omega t) + b_2\cos(2\omega t + (i-1)\varphi) + b_3\cos(3\omega t + 2(i-1)\varphi) + \cdots \quad (2)$$

In (2), the phase of the fundamental component is identical for all the paths, but the phases of the harmonics are different for each path. If the phase φ is chosen such that $\varphi = 360^\circ/n$, then all the higher harmonics are cancelled [6], except for the harmonics satisfying

$$k = j\times n + 1, \quad \text{where } j = 0,1,2,3,\ldots \quad (3)$$

B. Polyphase 2-Path and 3-Path Circuit Examples

Fig. 3 shows a polyphase 2-path circuit which is nothing but a well-known differential circuit driven with balanced (anti-phase) input signals. Since the upper path has a phase shift of 0°, all the harmonics generated by the nonlinear block as well as the fundamental component will have a phase of 0° at the output of the nonlinear block. In the lower path, the input of the nonlinear block has an opposite phase i.e., 180°. At the output, the harmonics that are created by even power terms have a phase of 0° while the odd powers have a phase of 180°. This difference in phase is exploited to cancel the even harmonics by providing a phase of -180° to the lower path and then adding. At the output, the fundamental and the odd harmonics arrive in phase, and so add up, while the even harmonics arrive in anti-phase and are cancelled.

A system with three paths is shown in Fig. 4. In this case, phase shifts of 0°, 120°, and 240° are added before and equal but opposite phases after the nonlinear circuit to path 1, 2, and 3, respectively. Due to the nonlinearity, the phase rotation for the kth harmonic is k times the input phase, so the fundamental component, the second harmonic, and the third harmonic will have phase shifts of $[0^\circ, 120^\circ, 240^\circ]$, $[0^\circ, 240^\circ, 120^\circ]$ and $[0^\circ, 0^\circ, 0^\circ]$, respectively, at the output of the nonlinear blocks of paths 1, 2, and 3. Fig. 5(a) shows how the phases of the harmonics at the output of each path combine. The fundamental components add up in phase, while the vectors for the second and third harmonics create a "balanced structure" at the output, resulting in a zero sum (cancellation). However, the fourth harmonic components align in phase again, and will add up like the fundamental. Fig. 5(b) shows that the DC, second, third, fifth, sixth, etc., harmonics are cancelled and the first noncancelled is the fourth with a 3-path system. Similarly, for a 4-path system the first noncancelled harmonic will be the fifth harmonic and in general for the n-path system the $(n+1)$th harmonic is the first noncancelled harmonic. In other words, the higher the number of paths, the higher will be the number of harmonic cancellations. Theoretically, an infinite number of paths are needed to cancel all the harmonics. However, in practice higher order harmonics are weaker than low-order harmonics and need not all be cancelled. Also, some filtering will in practice always be present, e.g., due to the limited bandwidth of an antenna or the speed limitations in a circuit. Moreover, mismatches will put a practical limit on what is feasible (see Section III-D).

C. Generalization to Intermodulation Distortion

If the nonlinear system as described in Fig. 2(a) is excited by a two-tone input signal $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$, besides harmonics the output will also contain intermodulation products at new frequencies $\omega = p\omega_1 + q\omega_2$, where p and q identify harmonics of ω_1 and ω_2, respectively, and can be positive or negative integer numbers. It is interesting to see whether the multipath technique also cancels such intermodulation products. To examine this, the phase relationship with the input frequency

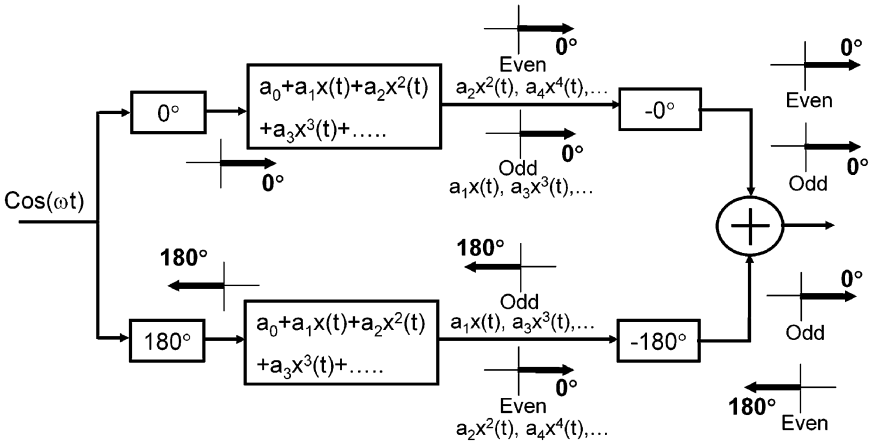

Fig. 3. Polyphase 2-path circuit cancelling even-order harmonics.

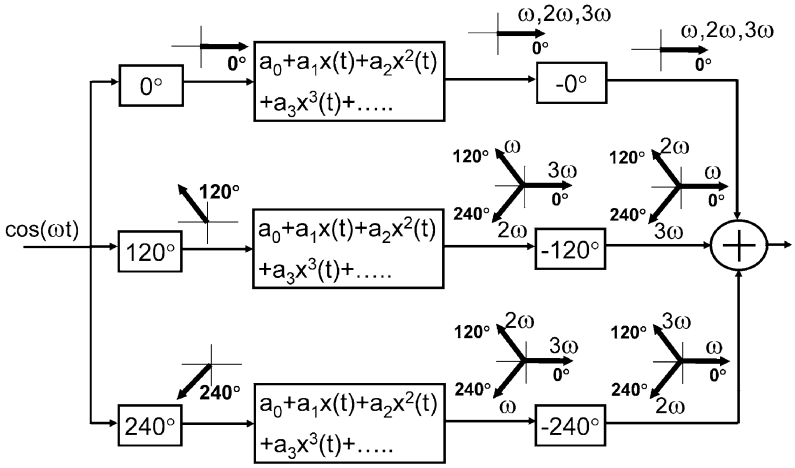

Fig. 4. Polyphase 3-path circuit cancelling 2ω and 3ω harmonics.

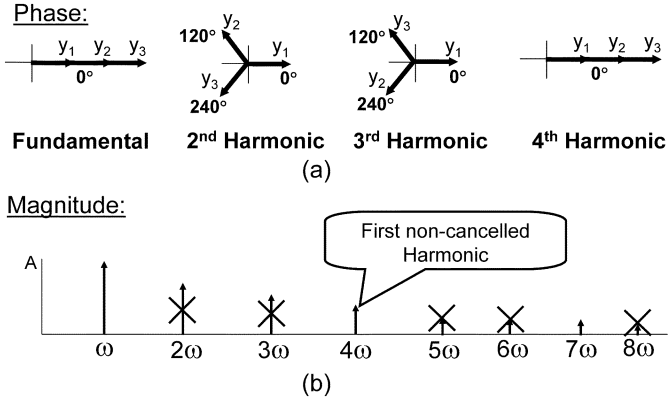

Fig. 5. Output of the 3-path circuit in Fig. 4. (a) Phasor diagrams. (b) Spectral plot.

is important. In Fig. 2(b), the phase shift of the kth harmonic at the output of the ith path is $(k-1)(i-1)\varphi$ for a single-tone test. Similarly, in case of two tones, the phase shift of the $p\omega_1 + q\omega_2$ products at the output of the ith path will be $(p+q-1)(i-1)\varphi$. So the products which satisfy (4) will not be cancelled.

$$p+q = j \times n+1 \quad \text{where } j = 0,1,2,3,\ldots \tag{4}$$

In particular, the third-order intermodulation products ($2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$) satisfy (4) for $j = 0$ because $p+q = 1$. These products always appear in phase at the output of each path and hence they are not cancelled with the multipath technique. However, other intermodulation products can be cancelled. In general, if $p+q = k$ and the kth harmonic is cancelled, then $p\omega_1 + q\omega_2$ is also cancelled.

D. Mixer as a Phase Shifter and Frequency Shifter

Polyphase filter circuits for image filtering are often implemented using linear *R-C* networks or *L-C* networks to realize the required phase shift. Although these circuits are sometimes referred to as wideband, the fractional bandwidth of such circuits seldomly exceeds 50% [9]. For harmonic rejection, we need circuits with a constant phase shift over a much wider range. This is because all phase shifters need to have a constant phase shift over all relevant frequencies involved in the cancellation process. In a DSP intensive radio transmitter, digital signal processing techniques can be exploited to realize phase shifters before digital-to-analog conversion and nonlinear power amplification. Therefore, a good solution can be to shift this phase generation problem to the digital domain, and use a DSP followed by multiple DACs to generate multi-phase baseband signals. However, behind the nonlinear element we are in the

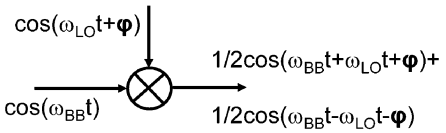

Fig. 6. Mixer used as a wideband phase shifter.

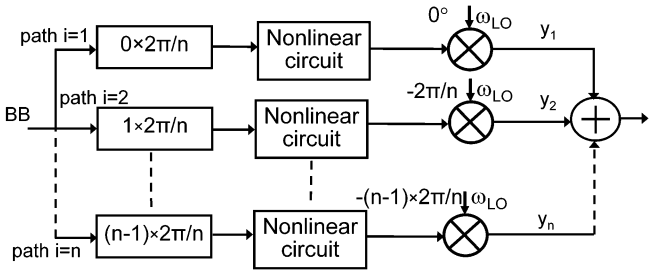

Fig. 7. Phase shifter after the nonlinear circuit is replaced by a mixer.

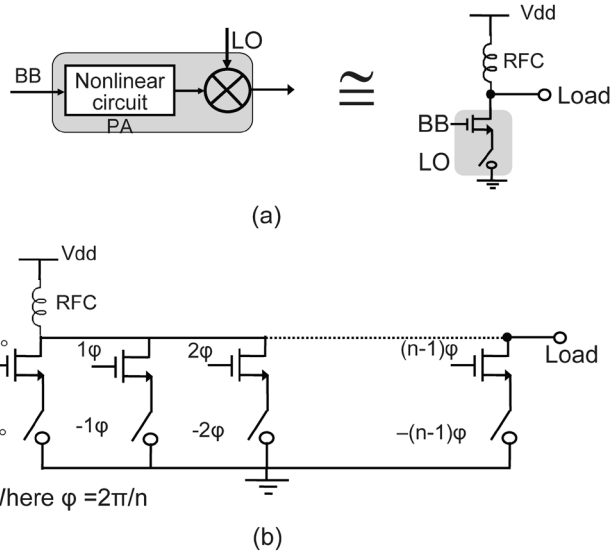

Fig. 8. (a) Basic power upconverter. (b) n-path power upconverter.

analog domain, and there can be many harmonics. In that case, cancellation of a multitude of harmonics requires a constant phase shift over many octaves of frequency.

A very wideband phase shifter can be implemented with a mixer, since a mixer conveys phase information of both the baseband (BB) and local oscillator (LO) port to the output (RF) port as shown in Fig. 6. Whatever phase is added to the LO signal, it will appear at the output of the mixer.[1] So by replacing the second set of phase shifters with mixers (Fig. 7), we can achieve a wideband phase shift, but simultaneously we will have upconversion. As upconversion is desired in a wireless transmitter circuit anyway, this fits very nicely to our goal. The first set of phase shifters can be implemented in the digital domain as explained above.

However, a mixer produces both a sum frequency and a difference frequency, and usually only one of these is the wanted signal, while the other (the "image") needs to be suppressed. Moreover, flexible frequency synthesizers rely on digital dividers and generally produce square-wave signals, while for power efficiency reasons it is highly desired to use a switching mixer and a large BB-signal swing. Therefore, the output spectrum will now contain a forest of harmonics and sidebands at frequencies $k_{\rm LO}\omega_{\rm LO} \pm m\omega_{\rm BB}$, where $k_{\rm LO}$ and m are integers, due to the multiplication of the square-wave LO with the baseband input signal BB, and the nonlinearity of the circuit. In the next section, we will see how we can exploit the polyphase multipath technique to cancel almost all the unwanted components.

III. Filterless Power Upconverter Design

A. Basic Power Upconverter

A power upconverter (PU) combines the functionality of a power amplifier (PA) and an upconversion mixer. The PA and mixer can be combined in the circuit of Fig. 8(a), which is equivalent to first amplification and then mixing. Here the PA is a single transistor operating as a transconductor (*V–I*) converter, which is switched on and off by the LO signal via a switch. Thus, the *V–I* conversion and upconversion is done in the same circuit, via a switched transconductor mixer [7]. With respect to efficiency this circuit resembles a single transistor (class A) power amplifier. However, due to the polyphase multipath technique distortion products are cancelled and larger signal swings can be tolerated, improving efficiency. A disadvantage of the PU is the power dissipation in practical switches (transistors). On the other hand, a narrowband filter behind a traditional power amplifier would also cause power loss.

B. n-Path Power Upconverter

To get an idea of spectral products generated with the power upconverter circuit, the basic [Fig. 8(a)] and the multipath power upconverter were simulated in Matlab. Nonlinear circuits were modeled by a power series expansion, while ideal phase shifters were used. Fig. 9(a) shows the spectral components (at $k_{\rm LO}\omega_{\rm LO} \pm m\omega_{\rm BB}$) generated by a single-path PU for a single-tone BB signal, i.e., the case where the polyphase multipath technique is not used. Clearly, nonlinearities and switching behavior result in a forest of strong harmonics and sidebands. To clean up the spectrum by using the multipath technique, we divide the PU into n identical smaller pieces, driven by BB and LO signals having equal but opposite phases, and then simply add their output currents at the output node as shown in Fig. 8(b). The phase shift at the baseband input is $0, 1\phi, 2\phi, \ldots, (n-1)\phi$ and its opposite phase is applied via the LO signals.

Fig. 9(b) shows the output of a polyphase 18-path circuit (see Section III-C for a motivation for the choice of the number of paths): most of the harmonics and sidebands are cancelled now. Unfortunately, a few are still present at the output. Since we have two input ports now (BB and LO), and mixing produces a sum and a difference frequency, a slightly different condition for noncancelled products is found [6]:

$$k_{\rm LO} = j \times n + m \quad \text{where } j = \cdots -2, -1, 0, 1, 2 \ldots \qquad (5)$$

and m is a positive or negative integer number. The most important noncancelled products are at $3\omega_{\rm LO} + 3\omega_{\rm BB}$, $5\omega_{\rm LO} +$

[1]This also holds for higher harmonics of the LO signal and baseband input-signal, as long as speed limitations in the mixer play no significant role.

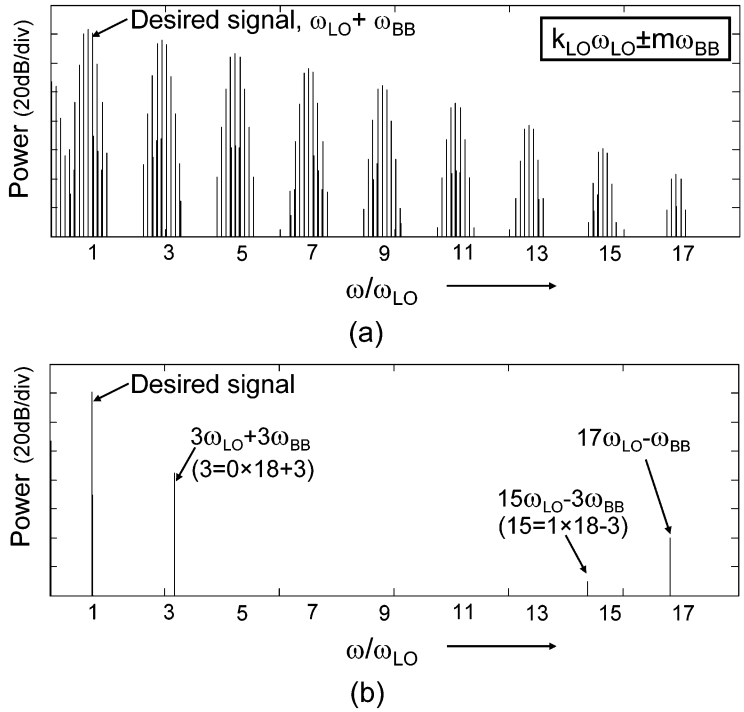

Fig. 9. Output spectrum. (a) Basic power upconverter. (b) 18-path power upconverter.

$5\omega_{\rm BB}$, $7\omega_{\rm LO}+7\omega_{\rm BB}$ $(j=0)$, and $15\omega_{\rm LO}-3\omega_{\rm BB}$, $13\omega_{\rm LO}-5\omega_{\rm BB}$ $(j=1)$. The product of the magnitudes of the respective harmonics of $\omega_{\rm LO}$ and $\omega_{\rm BB}$ determines the strength of these products. For a unity magnitude LO square wave, harmonic $k_{\rm LO}$ is $k_{\rm LO}$ times smaller than the fundamental. If we assume that the nonlinear circuit operates at its 1-dB compression point (to obtain high output power and efficiency) for an input signal $A\cos(\omega_{\rm BB}t)$, and a_1, a_5, a_7 are the coefficients of the nonlinearity, the magnitude of the $5\omega_{\rm LO}+5\omega_{\rm BB}, 7\omega_{\rm LO}+7\omega_{\rm BB}$ products are $(A^4a_5/(5\times 16a_1)), (A^6a_7/(7\times 64a_1))$, respectively, lower than the magnitude of the wanted signal at $\omega_{\rm LO}+\omega_{\rm BB}$. These higher order terms are much smaller than the wanted signal. Similar conclusions hold for the $j=1$ products. As a result, these products are typically smaller than residual products caused by inaccuracies like device and phase mismatch and it does not make much sense to cancel them. Still, the $3\omega_{\rm LO}+3\omega_{\rm BB}$ is troublesome because the third-order distortion term is usually much stronger than higher order distortion components [10] and is also close to the desired signal. It cannot be cancelled with any number of paths because in (5) $j=0$ for this case, so independent of n. To eliminate the strong $3\omega_{\rm LO}+3\omega_{\rm BB}$ terms, the duty cycle of the LO was chosen to be 1/3. By doing so, the 3rd, 6th, 9th, 12th, 15th, etc. harmonic term disappears from the Fourier series expansion. Thus, the troublesome terms at $3\omega_{\rm LO}+3\omega_{\rm BB}$ and $15\omega_{\rm LO}-3\omega_{\rm BB}$ are also rejected, while other terms are small enough. However, a 1/3 duty cycle also means that there will be harmonics with even coefficients like $2\omega_{\rm LO}, 4\omega_{\rm LO}$, etc. So other distortion products like $2\omega_{\rm LO}+2\omega_{\rm BB}, 4\omega_{\rm LO}+4\omega_{\rm BB}, 14\omega_{\rm LO}-4\omega_{\rm BB}, 16\omega_{\rm LO}-2\omega_{\rm BB}$ appear instead. Fortunately, it is quite easy to cancel these products by using a differential baseband input (balancing). This is desired anyway for rejecting common-mode interference like substrate and supply bounce. Fig. 10 and Table I give an overview of how different unwanted products are cancelled with the various techniques. The first significant noncancelled product for an 18-path system with 1/3 duty cycle and balanced BB-signals is $17\omega_{\rm LO}-\omega_{\rm BB}$.

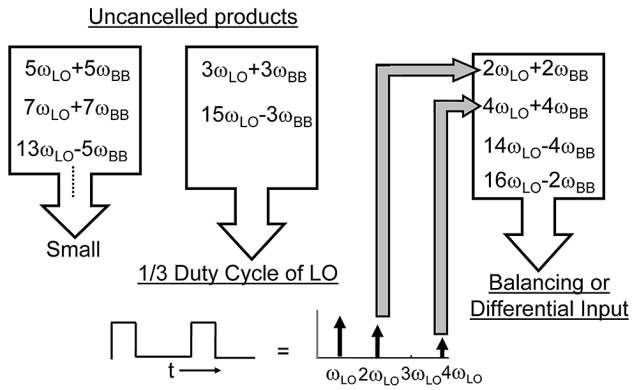

Fig. 10. Overview of solutions for the noncancelled product: the use of a square-wave LO with 1/3 duty cycle.

C. Circuit Implementation

To demonstrate the feasibility of a highly flexible multipath upconverter, we designed a PU in a 0.13-μm CMOS process, covering all radio bands between DC and 2.4 GHz. Assuming a signal swing in the order of the standard supply voltage of 1.2 V, it is possible to deliver about 10 mW power directly to a differential 100-Ω load, which is sufficient for many short-range communication links. If more output power is needed, the PU can act as predriver for one or more external power amplifiers.

TABLE I
CANCELLATION OF UNWANTED PRODUCTS IN AN 18-PATH PU WITH DIFFERENT TECHNIQUES

m ⟶	-4	-3	-2	-1	0	1	2	3	4
$1\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M		BM	M	BM
$2\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	B	M	BM
$3\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	D	BMD
$4\omega_{LO}+m\omega_{BB}$	BM	M	B	M	M	M	BM	M	B
$5\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$6\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$7\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$8\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$9\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$10\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$11\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$12\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$13\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$14\omega_{LO}+m\omega_{BB}$	B	M	BM	M	M	M	BM	M	BM
$15\omega_{LO}+m\omega_{BB}$	BMD	D	BMD	MD	M	MD	BMD	MD	BMD
$16\omega_{LO}+m\omega_{BB}$	BM	M	B	M	M	M	BM	M	BM
$17\omega_{LO}+m\omega_{BB}$	BM	M	BM		M	M	BM	M	BM

M=cancelled by multi-path, D=cancelled by 33% duty cycle, B=cancelled by balancing

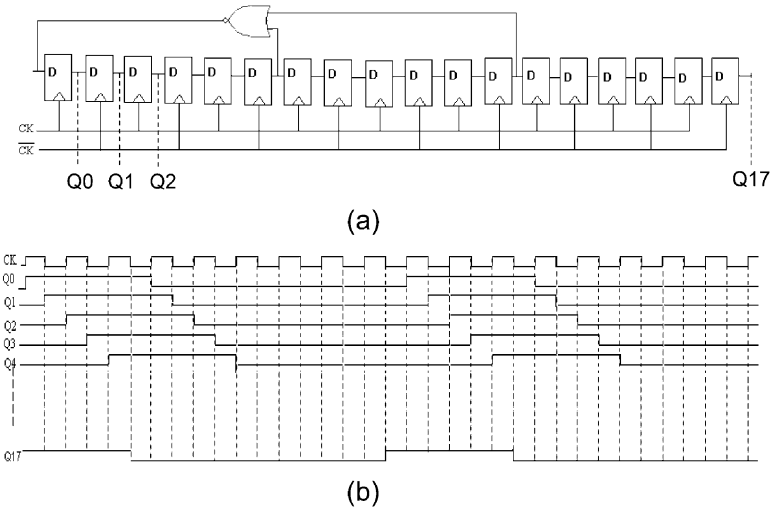

Fig. 11. (a) LO phase generation circuit. (b) Output: 18 phase LO signals.

To maximize the experimental flexibility and frequency range, we implemented the LO phase generation "brute force" via a shift register running at 9 times the LO frequency in our test chip. This enabled us to evaluate the circuit for an arbitrary LO frequency between DC and a maximum given by the speed limitation of the logic used to realize the shift register. A delay-locked loop (DLL) could be used to achieve even higher LO frequencies, provided it has enough phase accuracy. Moreover, other frequency synthesis techniques might be more appropriate and use less power. However, the key aim of this chip was to demonstrate the feasibility and RF performance of a polyphase multipath PU core. For experimental freedom, also the baseband polyphase signal generation was done off-chip.

The number of paths n was chosen because of the following reasons. To generate square-wave signals with 1/3 duty cycle and with the desired phase shifts from a high-speed clock, multiples of 3 are best suited for n. Furthermore, to utilize both the positive and negative edges of the clock, an even number of paths is desired so that the clock frequency needed will only be a factor of $n/2$ higher than the output frequency. The resulting suitable values of n are 6, 12, 18, etc., and we have chosen 18 paths in our test chip to demonstrate that the technique can cancel a large number of harmonics and sidebands. To show that it can also work for LO frequencies in the gigahertz region, we added the option to use 6 paths as well and designed the logic to run at 7.2 GHz, resulting in 2.4-GHz maximum LO frequency (and maximally 800 MHz in 18-path mode).

For 18 paths, we need LO signals of 18 different phases (0°, 20°, 40°, . . ., 340°) with 1/3 duty cycle. Applying a positive and a negative clock edge alternately to successive latches in a chain of 18 D latches [Fig. 11(a)], 18 different phases are produced [Fig. 11(b)]. The feedback through the NOR gate is used to

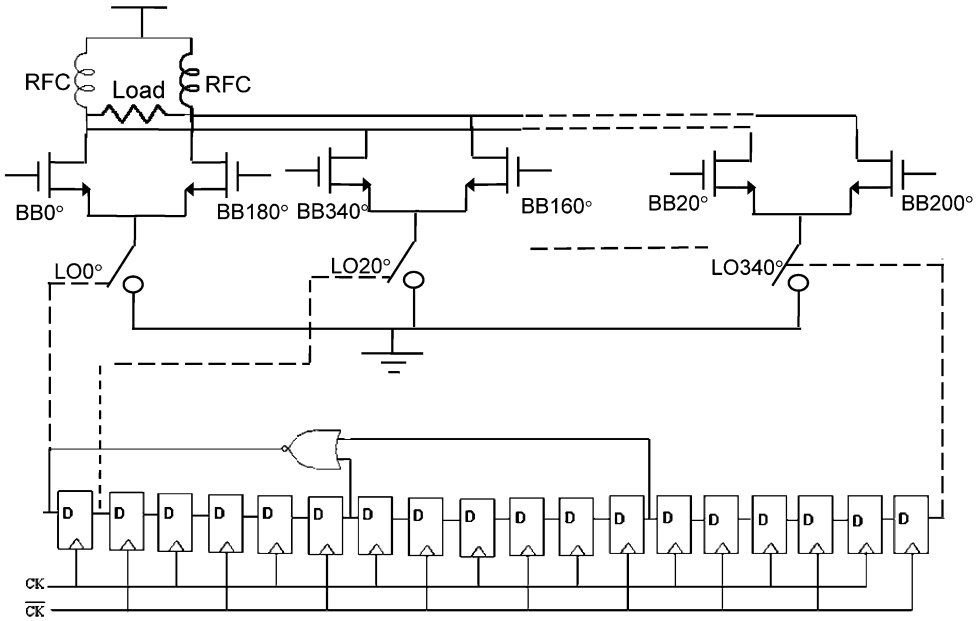

Fig. 12. Power upconverter using polyphase 18-path architecture.

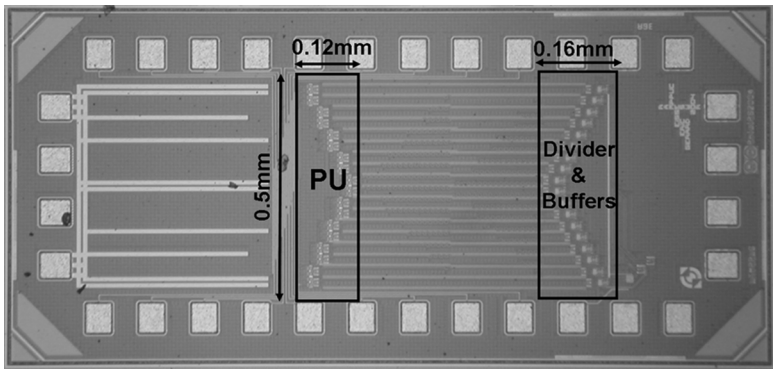

Fig. 13. Demonstrator chip micrograph.

make the duty cycle 1/3. To minimize the phase mismatch, the load of all the latches is made equal by adding dummy loads appropriately. Two sets of buffers are used in between the latches and the PU, one to drive the long wires between them and another to drive the switches of the PU. Note that the long wires are needed due to the bond-pad limitation of the chip (see Fig. 13).

To minimize cross-talk generation of the digital components of the divider chain to the PU, the latches, gates, and buffers are designed using current-mode logic (CML). The buffers that drive the PU switches have an output swing of approximately 850 mV (0.35–1.2 V), sufficient to switch the PU. The latches, NOR gate, and remaining buffers all have an input/output swing of approximately 600 mV (0.6–1.2 V). Dimensioning of the CML circuits, especially the latches, was done to maximize the speed. Increasing the tail current and the size of these CML cells simultaneously will result in an increase in speed as long as the load capacitance dominates the cell's own output capacitance [11].

In our experimental setup, the nine differential baseband voltages with different phases are generated off-chip. The signals were generated via a vector modulator, by weighted addition of a sine and cosine wave. Since the baseband signals are at much lower frequency compared to the LO, it is easier to realize sufficient phase accuracy (see the next section) and no tuning was required on our baseband signal-generation board. More work has to be done to explore the most effective way to generate multi phase baseband signals on-chip via DSP techniques and multiple DACs.

Fig. 12 shows the 18-path power upconverter. Each path consists of a switched transconductor mixer with a baseband signal applied to a differential pair, acting as the transconductor, and an LO signal driving a grounded switch. The wanted output signals from all paths add up in phase, so the total area and power of the power upconverter core is not increased by splitting it into 18 paths. Since all the paths are identical, the design of the PU is quite straightforward. The complete PU is biased at the supply voltage through RF chokes to increase the output swing and efficiency, as commonly done in power amplifier design. The inductance of the chokes puts a lower limit to the RF frequency, but the chip can work at arbitrarily low frequency. Operating each individual mixer at the 1-dB compression point, the PU is designed for a large output swing of 2.54 $V_{pp\text{-}diff}$ to get a good

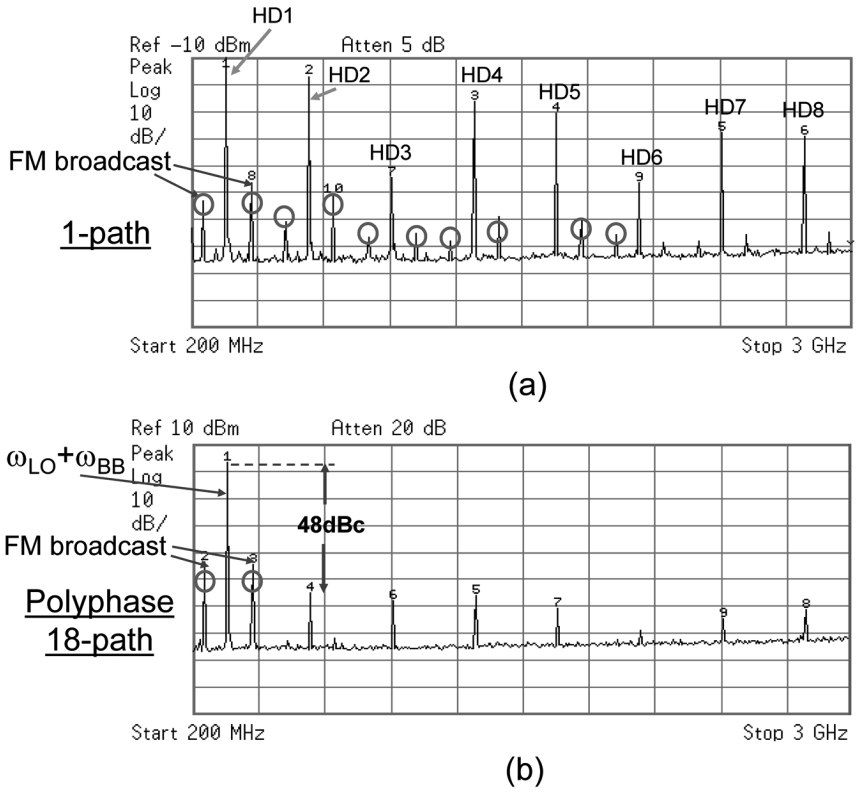

Fig. 14. Output spectrum. (a) Before cancellation. (b) After cancellation.

efficiency. This is close to the maximum swing that can be achieved from 1.2-V supply while keeping the upper transistor (transconductance transistor) of the PU in saturation. To further increase the output power without adding an external power amplifier, wider output transistors in combination with a transformer could be added for broadband impedance transformation.

Wide switch transistors are beneficial to reduce the static power dissipation in the switches but require more power in the driver buffers. This tradeoff is one factor that determines the size of switch. On the other hand, it is beneficial to choose the size of the transconductance and switch transistors roughly equal to maximize the amplification for minimal total width (area). The W/L ratio that was chosen for each transconductance- and switch transistor is $64/0.13$ and $50/0.13$, respectively. The resulting voltage conversion gain of the PU with the 1/3 duty cycle of the LO will be approximately $\sqrt{3}G_mR_L/\pi$, where G_m is the overall transconductance of the PU. Biasing is another important issue in a PU design. The bias voltage was chosen as low as possible, but still high enough to to keep the transconductance transistor in strong inversion and saturation for the full cycle of the input voltage (if the switch is ON). This helps to minimize the DC current and hence improve efficiency.

D. Mismatch

In practice, perfect cancellation of harmonics and sidebands is not possible due to the presence of mismatch between the paths. The effect of gain and phase mismatch on the cancellation of harmonics will be discussed in this section. If θ and δ are the phase mismatch in the baseband and LO signals, respectively, and ε is the gain mismatch between the paths, then the suppression of the $k_{\rm LO}\omega_{\rm LO} \pm m\omega_{\rm BB}$ harmonic in the presence of mismatch is given by [6]

$$E(\mathrm{HRR}_{k,m}) = \frac{P_{k,m,\mathrm{reference}}}{P_{k,m,\mathrm{rejected}}} = \frac{N^2}{(N-1)\left(\dfrac{\sigma_\varepsilon^2}{a_1^2} + k_{\rm LO}^2\sigma_\theta^2 + m^2\sigma_\delta^2\right)} \quad (6)$$

where $\sigma_\theta^2, \sigma_\delta^2$, and σ_ε^2 are the variances of the stochastic variables θ, δ, and ε, respectively, and $E()$ is the expectation operator. This equation predicts that the effect of phase mismatch is higher for higher harmonics because of the $k_{\rm LO}^2$ and m^2 terms. However, higher order harmonics are relatively weak. Interestingly, a higher number of paths is beneficial to suppress the harmonics more effectively in the presence of mismatch. Equation (6) also shows that the effect of device mismatch is constant for all the harmonics. Since a power upconverter uses large devices to produce sufficient output power, the device mismatch term is typically less important than the phase mismatch. Different design measures were taken to keep the phase of the various paths equal. For example, the loads of all the latches and buffers in the divider chain are made equal by adding dummy loads and the path length from dividers to PU for all paths was kept equal. A thorough mathematical analysis of the mismatch can be found in [6].

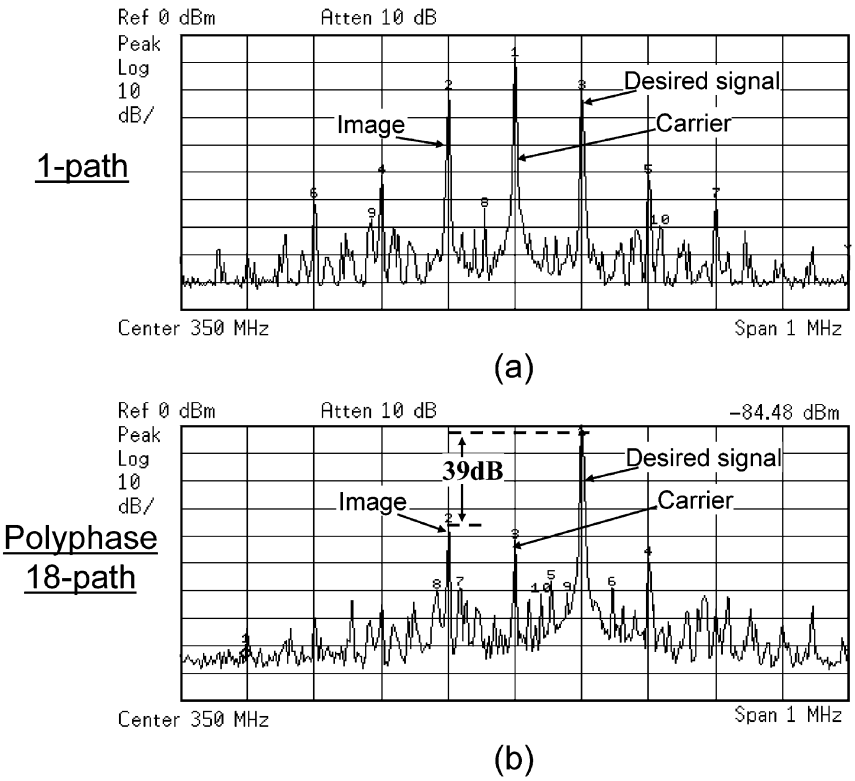

Fig. 15. The LO leakage and image rejection performance. (a) Before cancellation. (b) After cancellation.

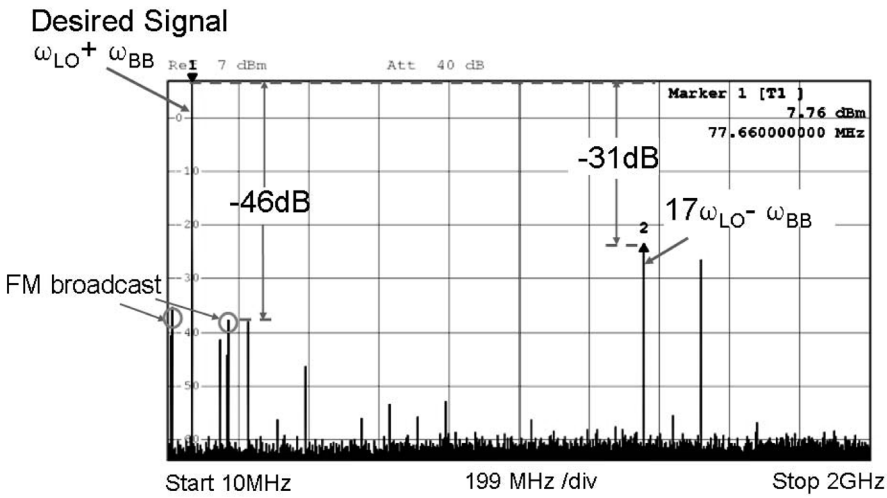

Fig. 16. Output spectrum for 80-MHz carrier.

IV. Experimental Results

A demonstrator chip of the proposed polyphase multipath power upconverter was designed and fabricated in a 0.13-μm CMOS process. The chip has a standard supply voltage of $1.2V$ and has an option to select a 6-path or 18-path operation mode. The die micrograph is shown in Fig. 13. The chip is clearly bond-pad limited for reasons of experimental flexibility. The active area of the two rectangular blocks, PU and dividers and buffers, shown in the Fig. 13, is only 0.14 mm^2. Between them are just wires to connect them. The baseband bandwidth is 0–50 MHz. During evaluation, the input baseband signal was arbitrarily chosen at 100 kHz, while varying the LO frequency between 0 and 2.4 GHz. No filters are used at the output. The RF choke (RFC in Fig. 12) and load are off chip. Operating each individual mixer at the 1-dB compression point, the PU delivers 8-mW power to the 100-Ω load.

Fig. 14(a) shows the measured output spectrum of a single-path power upconverter, which means without using the polyphase multipath technique. The frequency of the LO is 350 MHz. Please note that the unfortunate FM radio broadcast spurs that are modulated with our output signal are due to a 100.0 MHz, 10 kW FM radio broadcast transmitter on the roof of our building. The suppression of the 3rd, 6th, etc.,

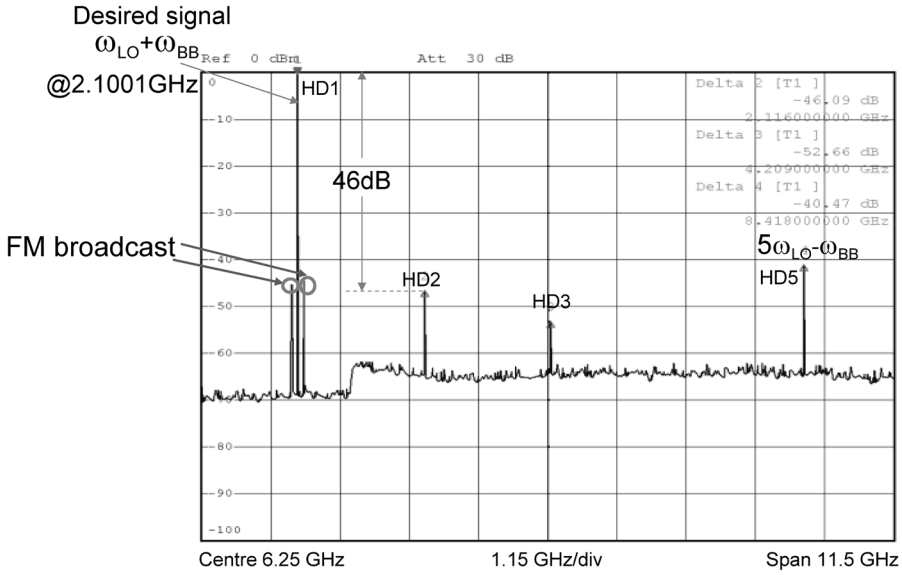

Fig. 17. Output spectrum with 6-path for 2.1-GHz carrier.

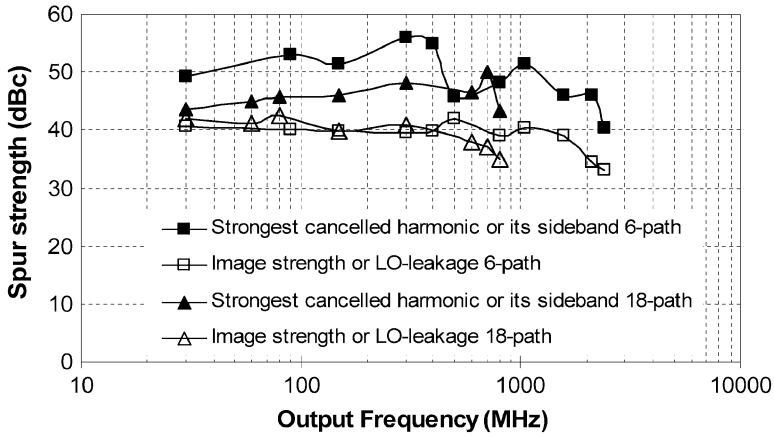

Fig. 18. Measured suppression of undesired products over the full output frequency range.

harmonics is due to the 1/3 duty cycle of the LO. Because of the large frequency scale, the sidebands around the fundamental and harmonic are not visible in this figure. Fig. 14(b) shows the measured spectrum after the cancellation by a polyphase 18-path circuit. All the harmonic products are effectively suppressed to -48 dBc.

Fig. 15(a) shows the measured upconverted signal (desired signal), its image and LO feed-through (carrier) with only one path. The suppression of the image and the LO feed-through due to the polyphase 18-path circuit is shown in Fig. 15(b). All the sideband products are suppressed to 39 dB below the desired signal.

In order to demonstrate the wideband cancellation property, we used a relatively low-frequency LO of 80 MHz. Now all harmonics up to 2 GHz are visible without attenuation in Fig. 16. The figure shows the first noncancelled harmonic $17\omega_{\rm LO}-\omega_{\rm BB}$ at 1.3599 GHz as predicted by the theory. The output spectrum is cleaned up to the 17th harmonic of the LO, with a worst case spur at -46 dBc. Fig. 17 shows the spectrum for a high output frequency of 2.1 GHz with a 6-path circuit. It shows a first noncancelled harmonic $5\omega_{\rm LO}-\omega_{\rm BB}$ (10.4999 GHz) as predicted by the theory and a worst case spur at -46 dBc up to this frequency.

Fig. 18 shows results of the harmonic rejection over the entire 2.4-GHz band of LO frequencies, and also for image rejection and LO leakage. The LO frequency is varied from 30 to 800 MHz for the 18-path PU and the strongest cancelled harmonics or sidebands are measured and plotted. For the 6-path PU this was also done, but now by varying the LO frequency from 30 MHz to 2.4 GHz. This figure shows that the worst case harmonic spur is smaller than -40 dBc in the entire frequency range. As the LO frequency reaches its limit, the spurs increase, most probably due to an increase in phase mismatch. But still the harmonic spurs remain below -40 dBc. The maximum clock frequency at which the circuit works is 7.2 GHz. The maximum LO frequency is thus 2.4 GHz for 6-path mode and 800 MHz for 18-path mode, as the clock frequency is divided 3 and 9 times, respectively. We did not test the PU using any particular standard. However, in simulation we did test the PU with a two-tone signal, and a detailed mathematical analysis of it can be found in [6].

TABLE II
OTHER PERFORMANCE

Technology		0.13μm CMOS
Supply Voltage		1.2V
Output Power		8mW
Output Swing		$2.54V_{pp\text{-}diff}$
Load		100Ω (diff)
Power Consumption	Digital circuits	156mW
	PU core	72mW
	Total	228mW
Worst case Harmonic Rejection (20 samples)		-40dBc

We also measured 20 samples of the IC at 350-MHz carrier frequency. All the harmonic spurs were smaller than −46 dBc for all the samples. $2\omega_{\rm LO} + \omega_{\rm BB}$ and $2\omega_{\rm LO} - \omega_{\rm BB}$ were the dominant harmonic spurs as these products are close to the fundamental and hence the strongest (just 6 dB below the carrier before cancellation). So the harmonic rejection for those products is better than 40 dB for 20 samples with a polyphase 18-path PU. From mismatch equation (6), this corresponds to 1.3° of phase mismatch in the LO path, neglecting the phase mismatch in the BB signals (since they are at low frequency) and the device mismatch (since large devices are used in the PU).

We tried to measure the output noise of the PU, but it was lower than the spectrum analyzer (ROHDE & SCHWARZ FSP 40 GHz) noise floor for the required dynamic range. Simulation result predict a thermal output noise voltage of -166 dBV/$\sqrt{\rm Hz}$ in 100 Ω (assuming the phase noise of the LO is negligible) and a $1/f$ corner frequency of 10 MHz from the LO. The G_m of the PU is 28 mS, rendering about 6 dB noise figure for the power upconverter. It is worth noting that the switched transconductor mixer has better thermal noise performance compared to a Gilbert mixer [7].

The performance parameters of the PU are summarized in Table II. The PU delivers 8 mW of output power to a 100-Ω load with a drain efficiency of 11%. The output swing is 2.54 $V_{\rm pp\text{-}diff}$. The total power consumption is 228 mW. The power consumption of the digital circuits, divider and buffers is currently high, i.e., 156 mW. One reason for this is the power consumption in driving the long wires between PU and LO generation circuits. In retrospect, it would have been better to keep this much shorter, which would save one set of drivers (34 mW). Another reason is the use of current-mode logic circuits for multiphase signal generation that are pushed for high operating frequency with high bias currents. By using standard logic gates or other smarter clock generation architectures, we believe that the power consumption can be reduced significantly. Future CMOS processes with faster transistors will help to increase the frequency range in the current clock generator and reduce its power consumption.

V. CONCLUSION

A polyphase multipath technique in combination with an LO with 1/3 duty cycle results in a power upconverter with a clean output spectrum up to the 17th harmonic of the LO (18-path mode) or 5th harmonic of the LO (6-path mode). It operates from DC to 2.4 GHz with worst case harmonic rejection of 40 dB over 20 samples. It uses no dedicated filters, but only digital blocks and switched transconductor mixers, making the design suitable for future software-defined radio architectures in CMOS. Further downscaling of CMOS processes is expected to relax the frequency range limitation in the current clock generator and reduce its power consumption.

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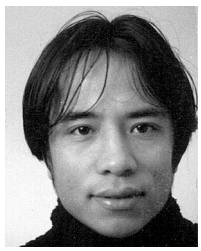

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