# Low-Frequency Noise Phenomena in Switched MOSFETs

Arnoud P. van der Wel, *Member, IEEE*, Eric A. M. Klumperink, *Member, IEEE*, Jay S. Kolhatkar, Eric Hoekstra, Martijn F. Snoeij, *Student Member, IEEE*, Cora Salm, *Member, IEEE*, Hans Wallinga, and Bram Nauta, *Senior Member, IEEE* 

*Abstract*—In small-area MOSFETs widely used in analog and RF circuit design, low-frequency (LF) noise behavior is increasingly dominated by single-electron effects. In this paper, we review the limitations of current compact noise models which do not model such single-electron effects. We present measurement results that illustrate typical LF noise behavior in small-area MOSFETs, and a model based on Shockley–Read–Hall statistics to explain the behavior. Finally, we treat practical examples that illustrate the relevance of these effects to analog circuit design. To the analog circuit designer, awareness of these single-electron noise phenomena is crucial if optimal circuits are to be designed, especially since the effects can aid in low-noise circuit design if used properly, while they may be detrimental to performance if inadvertently applied.

Index Terms—CMOS, flicker noise, large-signal excitation, low-frequency noise, low-noise circuit design, MOSFET, noise reduction, RTS noise, switched biasing, 1/f noise.

## I. INTRODUCTION

**M**OSFETs are notorious for their significant low-frequency (LF) noise. Constant downscaling makes the speed of the MOSFETs higher, lowers the power consumption and enables an ever-increasing level of integration. For digital circuits, this is all good news. Though analog circuits benefit from the higher speed, the reduced voltage headroom makes it increasingly difficult to maintain a sufficient signal to noise ratio, making low-noise design increasingly important [1]. Downscaling does not automatically reduce LF noise [2], and for speed and functional density reasons it is attractive to use small-area devices. Unfortunately, small devices have worse low-frequency noise, which means that LF noise performance is a dominant issue in ever more circuits. There are several

A. P. van der Wel was with the University of Twente. He is now with the Mixed-Signal Circuits and Systems Group, NXP Research, 5656 AE Eindhoven, The Netherlands (e-mail: arnoud.van.der.wel@nxp.com).

E. A. M. Klumperink, E. Hoekstra, and B. Nauta are with the IC-Design Group, Faculty of EEMCS, University of Twente, 7500 AE Enschede, The Netherlands.

J. S. Kolhatkar was with the University of Twente. He is now with the NXP Semiconductors/CTO/Process and Library Technology, 6534 AE Nijmegen, The Netherlands.

M. F. Snoeij is with the Electronic Instrumentation Laboratory, Faculty of EEMCS, Delft University of Technology, 2628 CD Delft, The Netherlands.

C. Salm is with the Semiconductor Components Group, Faculty of EEMCS, University of Twente, 7500 AE Enschede, The Netherlands.

H. Wallinga was with the Semiconductor Components Group, Faculty of EEMCS, University of Twente, 7500 AE Enschede, The Netherlands.

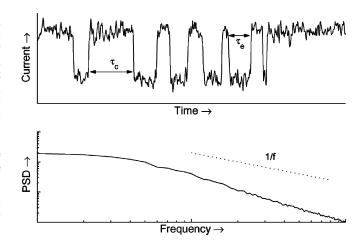


Fig. 1. LF noise of a MOSFET with a  $0.18 \cdot \mu m^2$  gate area. Upper: time domain. The abrupt jumps are caused by single electrons. Superimposed on this are other types of noise. Lower: frequency domain. The PSD has a Lorentzian shape: flat at low frequencies and decaying with -20 dB/dec at high frequencies.

issues that compound the problem, the most important of which are the following:

- 1) Due to the ever decreasing gate area, the number of charge carriers in a MOSFET channel is continually going down, and single-electron low-frequency noise phenomena quite different from 1/f are becoming visible. This means that classical noise with a Gaussian amplitude distribution and a 1/f-type power spectrum is replaced by Random Telegraph Signals (RTS) with a two-level amplitude distribution and a Lorentzian power spectrum (Fig. 1) [3].
- LF noise in small devices shows extreme variability; measured LF noise can vary by several orders of magnitude between different nominally identical devices [4].
- 3) MOSFET LF noise is reduced when the device is subjected to large signal excitation (LSE) [5]–[7]. In other words, turning a MOSFET off for some time before turning it on reduces its noise when it is on. This means that *the LF noise* of the device not only depends on the present bias state of the device but also on the bias history of the device. This effect is associated with the emptying of traps that cause RTS noise [6]. Application of this effect was demonstrated in oscillators [8]–[10], operational amplifiers [11] and various other circuits [12]–[15].

All these noise phenomena may show up in circuit measurements, while they are currently (2006) *not incorporated in any circuit simulator*. As a result, measured upconverted LF noise in oscillators is often not directly compared to simulations (e.g.,

Manuscript received March 20, 2006; revised November 3, 2006. This work was supported by the Technology Foundation STW, Applied Science division of NWO and the Technology Programme of the Ministry of Economic Affairs.

Digital Object Identifier 10.1109/JSSC.2006.891714

[16], [17]), and if comparisons are made at all, correspondence within a few dB is usually considered quite acceptable (e.g., [18]). For better circuit design, awareness of the LF noise phenomena described in this paper is vital.

In this paper, we treat these LF noise phenomena from a circuit design viewpoint. In Section II, an overview of current LF noise models along with their capabilities and limitations is presented. These models do not address single electron effects and are best applied to large-area devices. Bias dependence and scaling predictions made by the models are briefly reviewed in terms familiar to circuit designers. In Section III, we present recent measurement results on small area MOSFETs whose LF noise is dominated by single-electron effects. These new results highlight the limitations of existing models, and illustrate the requirement for an alternative, which is subsequently presented. The model, based on Shockley-Read-Hall statistics, explains several macroscopically visible noise phenomena such as the LF noise decrease when a MOSFET is subjected to switched biasing. In Section IV, we present two examples of new circuit techniques which use the physical effects described to improve the LF noise performance of the circuits in question. We also show how inadvertent degradation of the LF noise performance of circuits can occur if the phenomena described in this paper are insufficiently understood, thus highlighting the relevance of this work to analog circuit design. Finally, we sum up the most important conclusions of this work.

#### II. OVERVIEW OF EXISTING LF NOISE MODELS

The physical origin of LF noise in MOSFETs has long been unclear. One school of thought states that mobility fluctuations  $(\Delta \mu)$  cause LF noise. In 1969, Hooge showed that homogenous semiconductor samples suffer from bulk 1/f noise [19], which was later related to mobility fluctuations. The other view is that it is the number of free carriers in the device that is fluctuating  $(\Delta N)$ , an idea first postulated by McWhorter in 1955 [20]. Whereas p-channel MOSFETs are reported to show behavior in accordance with the  $\Delta \mu$  model [21], n-channel MOSFETs more often behave according to the  $\Delta N$  model. In 1990, Hung [22], [23] proposed a unified model that includes  $\Delta N$  and  $\Delta \mu$  fluctuations but also  $\Delta \mu$  fluctuations that are caused by (and correlated to)  $\Delta N$  fluctuations. When provided with suitable parameters, Hung's model yields results in excellent agreement with measurement results (for large devices), and it has since become the de-facto standard for modern circuit simulators [24].

#### A. Large Devices/Current Noise Models

To better understand the different noise models and how they appear to the circuit designer, it is instructive to provide a brief review. In literature, many different LF noise measures are encountered, for example  $S_{I_{\rm D}}$ ,  $S_{I_{\rm D}}/I_D^2$ , or  $S_{V_{\rm G}}$ . This often leads to confusion as to what dependencies should be expected, especially since there are three different LF noise mechanisms in a MOSFET.

If a conducting element exhibits LF noise, what is observed is that the conductivity is fluctuating and that the spectrum of conductivity fluctuations has a particular shape. We know that the

TABLE I OVERVIEW OF LF NOISE MODELS FOR LARGE DEVICES

Noise source	Scaling of $S_{I_{\rm D}}/I_{\rm D}^2$		Scaling of $S_{V_{ m G}}$
Noise source	with n	with $C_{\mathrm{ox}}^{\Box}$ & $V_{\mathrm{GT}}$	with $C_{\mathrm{ox}}^{\Box}$ & $V_{\mathrm{GT}}$
$\Delta \mu$	$n^{-1}$	$C_{\mathrm{ox}}^{\Box - 1} V_{\mathrm{GT}}^{-1}$	$C_{\mathrm{ox}}^{\Box - 1} V_{\mathrm{GT}}$
$\Delta N$	$n^{-2}$	$C_{\mathrm{ox}}^{\Box-2}V_{\mathrm{GT}}^{-2}$	$C_{\mathrm{ox}}^{\Box - 2}$
Correlated $\Delta N \& \Delta \mu$	$n^0$	$C_{ m ox}^{\Box 0}V_{ m GT}^{0}$	$V_{ m GT}^2$

conductivity  $\sigma$  is given by  $\sigma = nq\mu$ , in which n is the free carrier concentration and  $\mu$  is the mobility of the carriers. A fluctuation in  $\sigma$  does not in itself reveal whether the free carrier concentration (n) or the mobility  $(\mu)$  is fluctuating. To ascertain which mechanism is dominant, we look at the dependence of the relative conductivity fluctuation on the free carrier concentration n. This is sensible, since it is easy to vary n and hence the total number of free carriers N in a MOSFET by varying the effective gate overdrive voltage  $V_{\rm GT}(V_{\rm GT} = V_{\rm GS} - V_{\rm T})$ :

$$N = \frac{WLC_{\rm ox}^{\Box}V_{\rm GT}}{q} \tag{1}$$

where W and L are the effective device dimensions, and  $C_{ox}^{\Box}$ is the oxide capacitance per unit area [25]. Assuming a uniform channel (deep triode), N is proportional to n. For each of the three types of LF fluctuations we may encounter in a MOSFET, we will now derive their dependency on the free carrier concentration n and, consequently, their dependence on  $C_{ox}^{\Box}$  and  $V_{GT}$ . The results are summarized in Table I; note that all models scale inversely with device area:  $S_{I_D}/I_D^2$  and  $S_{V_G} \propto W^{-1}L^{-1}$ . Use has been made of the square-law MOSFET model for insight and to allow comparison with existing noise literature, in which use of the square law model is still quite common. Clearly, a more realistic model can be used if more accurate results are desired.

1)  $\Delta \mu$  Fluctuations: Hooge observed 1/f noise in homogenous semiconductor samples and observed that the PSD of the noise had an inverse dependence on N, the number of free carriers in the sample [19]. This led to his formulation of an empirical relation:

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H}{fN}.$$
(2)

The inverse relation between  $S_{I_D}/I_D^2$  and N yields the insight that whatever the electrons are doing when they are generating 1/f noise, they are doing it independently of one another. This is because (a) N independent noise sources (carriers) will produce total noise proportional to N and (b) the current  $I_D$ is also proportional to N, resulting in the observed 1/N dependence of (2). Later it was shown by other experiments that the fluctuations observed by Hooge were mobility fluctuations  $(\Delta \mu)$ .<sup>1</sup> The inverse dependence on N (and n since a constant

<sup>&</sup>lt;sup>1</sup>Note that this means that it is not *the macroscopic mobility of the semiconductor* which is varying, but rather, it must be the *individual* mobility of *individual* electrons which is varying. See also [26].

geometry is assumed) leads to a dependence on  $C_{\text{ox}}^{\Box}$  and  $V_{\text{GT}}$  as shown in Table I.

2)  $\Delta N$  Fluctuations: A MOSFET also exhibits number fluctuations ( $\Delta N$ ). The number fluctuations in a MOSFET are caused by trapping-detrapping at the interface. The process is rate-limited by the number of available traps, not the number of available electrons, which means that the spectrum of number fluctuations is independent of n and the relative noise current spectrum is inversely proportional to the square of the carrier concentration:

$$\frac{S_{I_D}}{I_D^2} \propto \frac{1}{n^2}.$$
(3)

This fluctuation is a variation of the charge trapped in the oxide, so using Q = CV for the MOS capacitor, this leads to a  $C_{\text{ox}}^{\Box}$  and  $V_{\text{GT}}$  dependence for the triode region as shown in Table I.

3) Correlated Fluctuations: Finally, a third type of LF noise may exist in a MOSFET. Trapping and detrapping of carriers in traps causes local changes in the electrical field, causing electrons to experience Coulomb scattering, a mobility fluctuation correlated to the trapping event. This gives rise to a relative current fluctuation that is independent of n:

$$\frac{S_{I_D}}{I_D^2} = S_{\Delta N} \left(\frac{d\mu}{dn}\right)^2. \tag{4}$$

The resulting  $C_{\text{ox}}^{\Box}$  and  $V_{\text{GT}}$  dependencies are given in Table I. Note that contrary to common belief, this correlated type of noise does not exhibit an n (and therefore  $C_{\text{ox}}^{\Box}$  and  $V_{\text{GT}}$ ) dependency that is somewhere halfway between  $\Delta N$  and  $\Delta \mu$ .

# B. Spectral Shape

Traditionally, the LF noise spectrum has had a 1/f shape over a very large frequency range. The  $\Delta\mu$  model does not explain the shape of the spectrum and only states that the  $\Delta\mu$  fluctuations must logically have a 1/f shape as well.

The  $\Delta N$  model, on the other hand, explains the origin of the 1/f spectrum by assuming that it is a summation of a large number of uncorrelated Lorentzian spectra, each caused by a single trap. A trap produces a Lorentzian PSD [27]:

$$S_{\rm RTS}(\omega) = 2(\Delta I)^2 \frac{\beta}{(1+\beta)^2} \frac{1}{\omega_{\rm 0RTS}} \frac{1}{1+\frac{\omega^2}{\omega_{\rm 0RTS}^2}} \quad [{\rm A}^2 {\rm Hz}^{-1}]$$
(5)

where  $\beta$  is a symmetry factor for the trap and  $\omega_{\text{ORTS}}$  is the corner frequency of the Lorentzian. If a device contains a large number of traps, and their corner frequencies are exponentially distributed, a 1/f spectrum will result (Fig. 2). Mobility fluctuations caused by number fluctuations inherit the PSD of the number fluctuations they are caused by.

# C. Process Downscaling and 1/f Noise

To analyze the influence of process scaling on 1/f noise, different approaches may be followed. One possibility is to use a simple model for CMOS scaling and derive the expected LF noise scaling rules. Even though the outcome depends on the boundary conditions chosen, the general trend is clear: 1/f

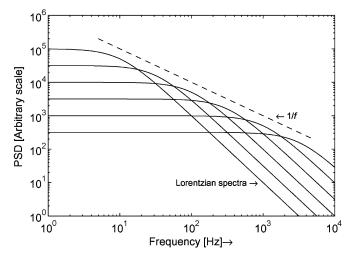


Fig. 2. Addition of Lorentzian spectra resulting in a 1/f spectrum.

noise is becoming a more significant limitation in future analog CMOS circuit design as device sizes (W and L) go down faster than  $C_{\text{ox}}^{\Box}$  goes up, thus reducing the number of carriers in a device ((1) and [28]). Simulation-based analysis [2], supported by measurements, predicts a similar trend.

#### III. RANDOM TELEGRAPH SIGNAL NOISE IN MOSFETS

The models discussed in the previous section work well for large-area devices. For small devices, they break down because the number of mobile charge carriers is no longer large and behavior of individual charge carriers becomes visible and significant.

Theory [29] predicts that as soon as the number of free carriers in a device decreases far enough, it will be possible to observe behavior of individual carriers at the terminals of the device. This is in line with measurements: as active device area became smaller and smaller, it became possible to observe Random Telegraph Signals (RTS) in MOSFETs at room temperature [3]. Nowadays, RTS noise is the dominant noise mechanism in small-area MOSFETs, typically with active areas of less than 1  $\mu$ m<sup>2</sup> [30].

In this section, we will examine the RTS time constants and how they influence RTS visibility. This will be done for steadystate bias conditions and also for transient bias conditions.

### A. Steady-State Behavior of RTS Noise

An RTS (Fig. 1) is caused by the capture and emission of a mobile charge carrier in a so-called trap, a localized energy state somewhere in the bandgap. Physically, traps are caused by defects at the Si-SiO<sub>2</sub> interface (impurities or dangling bonds). Electrically, a trap modulates the drain current of a MOSFET in two ways. First, the charge carrier that is captured no longer takes part in conduction ( $\Delta N$ ). Second, the trap that captures a carrier becomes charged by doing so, and this may modulate the position of the channel in the vicinity of the trap, thereby changing the macroscopic mobility of the device (correlated mobility fluctuations). If the trap is strategically placed [31], it may cause a relatively large conductivity fluctuation.

It is instructive to briefly review steady-state RTS behavior. The important parameters of an RTS are its mean high and low

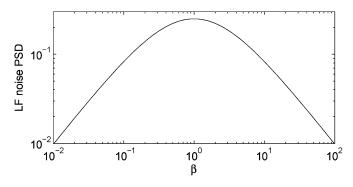


Fig. 3. RTS noise power as function of the asymmetry of the RTS.  $\omega_{\text{ORTS}} = 1$ , amplitude = 1. Maximum power for  $\beta = 1$  (symmetrical RTS).

time and its amplitude. The high current state of the device is associated with the untrapped state of the carrier, and the low current state is associated with the trapped state of the carrier (Fig. 1). The time constants  $\tau_e$  and  $\tau_c$  are named to correspond to the emission and capture *process*, respectively, so that  $\tau_e$  is the mean time before emission occurs, i.e., corresponding to the *trapped* state of the carrier. The converse holds for  $\tau_c$ .

The PSD of an RTS has a Lorentzian shape [27], described by (5). The relation between the trap time constants  $\tau_e$  and  $\tau_c$ and the RTS parameters  $\beta$  and  $\omega_{ORTS}$  is given by

$$\beta = \frac{\tau_{\rm c}}{\tau_{\rm e}} \text{ and } \omega_{\rm 0RTS} = \frac{1}{\tau_{\rm e}} + \frac{1}{\tau_{\rm c}} \text{ [rad/s]}.$$
 (6)

The PSD of (5) is proportional to  $\beta/(1+\beta)^2$ . If  $\beta = 1$ , the RTS is symmetrical, and the PSD has maximum power. If the RTS is asymmetrical, the noise power of the RTS drops. This is illustrated in Fig. 3. Intuitively, this is clear as a symmetrical RTS has a maximum transition probability and hence a maximum variance.

### B. Bias Dependence of RTS Noise

Having determined how RTS behavior depends on the RTS time constants, the next step is to determine how the RTS time constants depend on the bias of the device. For an n-channel MOSFET, according to basic theory [32],  $\tau_c$  is bias dependent via the bias dependency of n. If the trap is situated some distance in the oxide,  $\tau_e$  may also be bias dependent [33]. Measurements of the bias dependency of  $\tau_e$  and  $\tau_c$  are given in [3] and [34]–[38]. For n-channel devices, it is found in all cases that as  $V_{\rm GS}$  is decreased,  $\tau_c$  increases and  $\tau_e$  decreases. The change in  $\tau$  is commonly up to two orders of magnitude, though even more is observed in certain devices [35].

#### C. Transient Behavior of RTS Noise

The RTS time constants  $\tau_e$  and  $\tau_c$  are instantaneous functions of the bias ( $V_{GS}$ ) of the device. The occupancy, on the other hand, can only change in response to a change in  $\tau_e$  and  $\tau_c$  and will therefore necessarily lag behind.

This can be seen by turning a device on at t = 0 and subsequently observing the occupancy of a trap in the device. Measurements for three different devices are given in Fig. 4. An exponential fit to the data is included. The measurement technique employed is described in detail in [39] and [40].

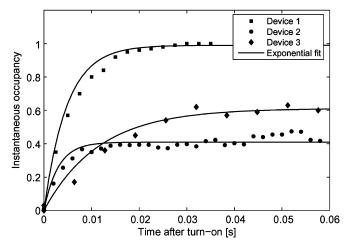


Fig. 4. Transient behavior of RTS noise in three different MOSFETs. Exponential occupancy change indicates that  $\tau_{\rm e}$  and  $\tau_{\rm c}$  are instantaneous functions of the bias of the device.

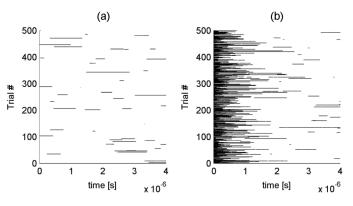


Fig. 5. View of an RTS under steady-state and transient conditions. Black corresponds to an empty trap, white to a full trap. (a) Steady-state measurement; (b) transient measurement.

In the measurements, the traps reach their steady-state occupancy in an exponential fashion, indicating that the time constants do indeed change instantaneously with the bias ( $V_{\rm GS}$ ) of the device.<sup>2</sup> An alternate view (of a different RTS) is given in Fig. 5, which shows steady-state and transient behavior of an RTS. In Fig. 5(b), the device is switched on at time t = 0 after having been off for a time much longer than the RTS time constants. Turning the device off has clearly emptied the RTS (the "black" state), and steady-state behavior is only resumed after several microseconds.

## D. Modelling of Transient RTS Behavior

If a MOSFET is subjected to a rapidly changing bias, its LF noise can change significantly, as seen for example in Fig. 6. A state-of-the-art circuit simulator is unable to predict or reproduce such behavior, instead predicting a simple 1/f-type LF noise PSD ("Model prediction" in the figure), which only changes by 6 dB when the device is subjected to the biasing conditions shown. In contrast, this device has LF noise that is dominated by a single RTS, and when it is turned on and off much faster than  $\tau_e$  and  $\tau_c$  by making  $V_{GS}$  a square wave, the

<sup>&</sup>lt;sup>2</sup>Measurements show that it does not matter whether the device is turned off by pulling the gate down or by pulling the source up [28].

Fig. 6. Steady-state noise and noise under large signal excitation.

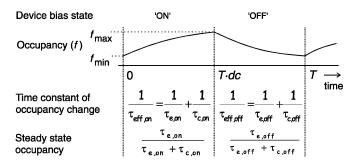


Fig. 7. Occupancy of trap.

RTS disappears because the trap in the device never reaches its steady-state occupancy and instead adopts some sort of average occupancy. As will be shown, this means the effective RTS time constants  $\tau_{e,eff}$  and  $\tau_{c,eff}$  will change. The derivation below is given in more detail in [28] and [41].

The occupancy of a trap f(t) at any given moment is [32]

$$f(t) = \frac{\tau_{\rm e}}{\tau_{\rm e} + \tau_{\rm c}} + K \mathrm{e}^{-\left(\frac{1}{\tau_{\rm e}} + \frac{1}{\tau_{\rm c}}\right)t} \tag{7}$$

where K depends on the initial condition. We treat the case where the bias voltage alternates abruptly and periodically between two states; reference is made to Fig. 7 where dc is the duty cycle. From t = 0...Tdc, the device is on; during this time, RTS behavior is governed by  $\tau_{e,on}$  and  $\tau_{c,on}$ , and from t = Tdc...T, the device is off, and RTS behavior is governed by  $\tau_{e,off}$  and  $\tau_{c,off}$ . The occupancy is given by (7) at all times; the steady-state occupancy is never reached because the switching frequency is high. Instead, the occupancy varies between  $f_{min}$ and  $f_{max}$ .

Substituting

$$\tau_{\rm eff,on} = \left[\frac{1}{\tau_{\rm e,on}} + \frac{1}{\tau_{\rm c,on}}\right]^{-1} \text{ and } \tau_{\rm eff,off} = \left[\frac{1}{\tau_{\rm e,off}} + \frac{1}{\tau_{\rm c,off}}\right]^{-1}$$
(8)

and equating f(0) and f(T), we may derive an expression for  $f_{\min}$  and  $f_{\max}$  [41]. If the switching frequency is made very high compared to the RTS corner frequency (T much smaller than  $\tau_{\rm e}$  and  $\tau_{\rm c}$ ),  $f_{\min}$  and  $f_{\max}$  converge to the same value,  $f_{\rm eff}$ ,

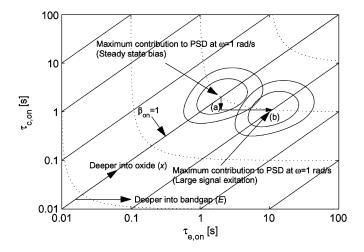


Fig. 8. Contribution to PSD at  $\omega = 1$  rad/s for different RTSs.

and the RTS becomes stationary. This effective stationary RTS has time constants  $\tau_{c,eff}$  and  $\tau_{e,eff}$  which can be found to equal

$$\tau_{\rm c,eff} = \left[\frac{dc}{\tau_{\rm c,on}} + \frac{1 - dc}{\tau_{\rm c,off}}\right]^{-1} \text{ and } \tau_{\rm e,eff} = \left[\frac{dc}{\tau_{\rm e,on}} + \frac{1 - dc}{\tau_{\rm e,off}}\right]^{-1}.$$
(9)

Experimental verification of this result is given in [40].

In summary, a cyclostationary RTS with a constant amplitude and two states, an on state from  $t = 0 \dots Tdc$ , (time constants  $\tau_{e,on}$  and  $\tau_{c,on}$ ), and an off state from  $t = Tdc \dots T$  (time constants  $\tau_{e,off}$  and  $\tau_{c,off}$ ), can, if the switching frequency is sufficiently large, be described by an effective stationary RTS with parameters  $\tau_{e,eff}$  and  $\tau_{c,eff}$ , for which the expressions are given above. If the effective RTS time constants are strongly asymmetric, the PSD of the RTS will decrease.

#### E. Generalisation to Trap Distribution

In order to predict noise performance of large devices or large numbers of small devices, we can now generalise single-trap behavior to trap distributions. To do so, we identify the dominant traps both in the steady-state and under transient conditions.

The PSD of an RTS is given by (5); the same holds for the effective stationary RTS, the time constants of which were are given by (9).

To illustrate which RTS are the dominant contributors to LF noise at the output, the PSD of the RTS at a particular frequency (in this example,  $\omega = 1$  rad/s) is plotted in Fig. 8 as a function of  $\tau_{e,on}$  and  $\tau_{c,on}$ . Contour lines denote the  $\tau$ 's of RTSs with a relative noise power contribution of 80% and 60% compared to the dominant RTS which is at the heart of the contours. The dominant contribution to output noise always comes from traps with  $\beta$  close to 1 and  $\omega_{0RTS}$  close to the frequency of interest. Traps with large or small  $\beta_{on}$  are mostly empty or full respectively and do not contribute significantly to the noise. If the RTS corner frequency, the contribution of this RTS will be insignificant as well.

To examine RTS behavior when the device is periodically turned on and off, bias dependence of  $\tau_{\rm e}$  and  $\tau_{\rm c}$  is modelled in a very simple and insightful way:  $\tau_{\rm e,off} = \tau_{\rm e,on}/m_{\rm e}$  and

 $\tau_{\rm c,off} = \tau_{\rm c,on} \cdot m_c$ , respectively. Combining this with (9), it follows for  $dc = 0.5^3$  that  $\tau_{\rm e,eff} = (2/(m_{\rm e} + 1))\tau_{\rm e,on}$  and  $\tau_{\rm c,eff} = (2m_c/(m_c+1))\tau_{\rm c,on}$ . This changes the effective time constants of all RTSs in the device in such a way that for  $m_{\rm e} = m_c = 10$  (a)  $\tau_{\rm c}$  has decreased by a factor 1.8 and (b)  $\tau_{\rm e}$  has increased by a factor 5.5 compared to the steady-state situation. The main contribution to the PSD is therefore now from different traps. Traps that were mostly full in the steady-state case now have an occupancy closer to 50%, and they dominate output noise.

The shape of the noise contribution curve in Fig. 8 does not change; it has only been shifted along the  $\log \tau_e$  and  $\log \tau_c$  axes. Hence, the noise PSD will not change at all if the distribution of  $\tau$ 's is uniform in  $\log t$ . Such a uniform distribution in  $\log t$ results if two conditions are satisfied. First, the distribution of trap depth in the oxide, x, should be uniform. (This is the basis of McWhorter's model [20] and responsible for the emergence of a 1/f spectrum.<sup>4</sup>) Second, the energy level of traps, E, should be uniformly distributed throughout the bandgap. If these conditions are satisfied, a uniform distribution of traps in  $\log \tau_e$  and  $\log \tau_c$  results.

To explain that turning a device on and off periodically leads to a decrease in the LF noise PSD [5]–[7], [42], we must conclude that the distribution of trap  $\tau$ 's is *not* uniform in log t. This can be the distribution of  $\tau$ 's in a large device with very many traps, but it can also be the distribution of  $\tau$ 's over an ensemble of small devices, each with a limited number of traps.<sup>5</sup> One likely scenario [43] is that the trap density deeper in the bandgap is lower.<sup>6</sup> Fig. 8 shows that traps deeper in the bandgap are the ones contributing LF noise when the device is periodically turned on and off, and if the trap density is lower there as is often observed [43], this explains why turning the device on and off lowers the LF noise.

In conclusion, we have shown that when a MOSFET is periodically and rapidly turned on and off, traps deeper in the bandgap dominate the LF noise performance of the device. Since trap densities in MOSFETs are commonly U-shaped in energy [43], [44], this explains that LF noise in MOSFETs decreases when the device is periodically turned on and off [5]–[7], [42]. A circuit designer may expect a large MOSFET to behave predictably in this way. Small MOSFETs behave in a slightly more complex fashion: an individual device may show a noise increase or a decrease depending on the traps the device happens to contain, but for a group of devices, the average noise will decrease.

## IV. IMPACT ON CIRCUIT DESIGN

The study of RTS noise under large signal excitation (LSE) has important practical circuit design consequences. In this section, existing work is reviewed, and subsequently some exam-

<sup>4</sup>Direct tunnelling is assumed, making the capture cross section a negative exponential function of x.

<sup>6</sup>The trap depth distribution in the oxide may still be uniform: Nonuniformity in E does not preclude the emergence of a 1/f spectrum.

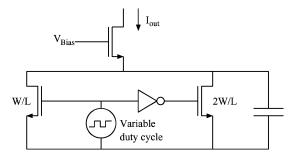


Fig. 9. Switched current source. Filtering at the output allows this to be used as a DC current source.

ples are presented of how LF noise under LSE influences the design of analog circuits.

#### A. Existing Work

A number of circuits have been presented by other authors that make use of or purport to make use of LSE to improve the LF noise performance [11]–[15]. Unfortunately, there appears to be a widespread belief that LF noise reduction through LSE is modelled in current circuit simulators, and consequently, circuit effects are mistaken for device-physical effects. Furthermore, considering the wide latitude of results and the very significant spread in LF noise performance between nominally identical devices [4], it is very important to distinguish between measurement results on a single "golden sample" and measurements on a statistically significant group of nominally identical devices. Nevertheless, it is clear that a reduction of LF noise in analog CMOS circuits by LSE is both desirable and feasible.

#### B. A Switched Current Source

One example of where classic LF noise modelling clearly shows its limits is the switched current source of Fig. 9. This is a current source that alternately activates a transistor with width W and one with width 2W. By changing the duty-cycle from 0 to 100% the current can be varied by a factor 2. A filter is placed at the output to suppress the obvious HF fluctuations in current. As an added bonus, the LF noise of the current source decreases when the duty cycle of the driving square wave is not 0 or 100% as can be seen from the shape of the "Traditional model" curve in Fig. 10. This is due to the LF noise of both devices being uncorrelated. The measured LF output noise of the circuit, however, is much lower than predicted by traditional models. This is caused by the decrease of the LF noise of the devices as a result of the large signal square wave they are subjected to. The LF noise model of Section III ("Proposed model" in Fig. 10), when coupled with a U-shaped distribution of traps, is seen to provide a fit that is in qualitative agreement with the measurement results.

### C. Correlated Double Sampling

Another example in which the importance of this work is highlighted is a correlated double sampling circuit. Correlated double sampling is commonly used to reduce LF noise. It is very effective, but it does not remove all the LF noise. Subjecting the device to LSE seems to be a possibility to further reduce the LF noise, as it would appear to be an orthogonal technique. As we

<sup>&</sup>lt;sup>3</sup>Other duty cycles can be treated similarly.

<sup>&</sup>lt;sup>5</sup>An individual small device will behave according to the traps it happens to contain, but the ensemble average of the noise performance will be the same as for a single large device with many traps, assuming that individual traps make uncorrelated contributions to the output noise.

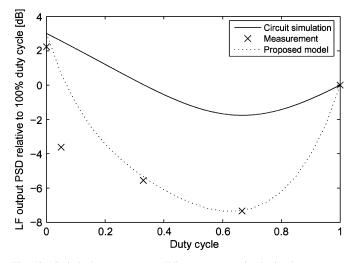


Fig. 10. Switched current source: Whereas current circuit simulators cannot correctly predict LF output noise, the model of Section III, coupled with a coarse approximation of a U-shaped trap distribution provides a much better fit.

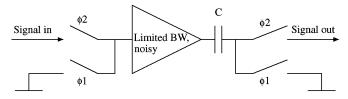


Fig. 11. Correlated double sampling.

will show in this section, this is not necessarily the case, and if carelessly applied, CDS in conjunction with LSE will make the LF noise performance of the circuit worse, not better.

A generic CDS system is shown in Fig. 11. We assume a signal source, followed by a preamp of limited bandwidth that suffers from additive white and 1/f noise. A two-phase clock allows us, in phase  $\phi_1$ , to make the input "0" and store a sample of the noise in capacitor C. In phase  $\phi_2$ , the input signal is connected to the preamp, and the noise sample of phase  $\phi_1$  is effectively subtracted from the output. Intuitively, the principle of operation is obvious: If the noise is strongly correlated in time, the noise from phase  $\phi_1$  and  $\phi_2$  will be almost identical and the noise will be largely cancelled by the CDS operation. If, on the other hand, the two noise samples are uncorrelated in time, subtracting them is equivalent to adding their powers. Because of this, the CDS operation will double the output noise power if the noise is white.

Despite the attenuation of LF noise by CDS, LF input noise may still be dominant at the output. Conditions for which this is the case are derived in [28]. In such a case, LF components of the 1/f noise are adequately suppressed, but the HF part of the 1/f noise contributes noise at the output. One example of a circuit where 1/f noise is typically the dominant noise source despite the use of CDS is an CMOS imager pixel [45], which is treated in more detail here.

A CMOS imager pixel is shown in Fig. 12. After a certain integration period during which light is incident on the photodiode, transistor M1 is switched on and resets the floating diffusion to a high potential. This reset voltage is read out by asserting the Row Select line, which connects transistor M2 to

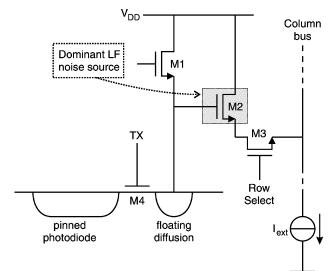


Fig. 12. CMOS imager pixel.

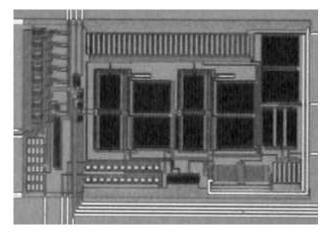


Fig. 13. Test structure for noise measurement using correlated double sampling and large signal excitation to reduce LF noise.

the current source  $I_{\text{ext}}$  that is external to the pixel. After the read-out of this reset voltage, the photo-charge is transferred to the floating diffusion via transfer gate M4, and read-out in the same way. By subtracting both read-out signals a correlated double sampling operation is performed, allowing removal of offset of M2 and kT/C noise of the floating diffusion. M1 to M4 have to be very small to maximise the photosensitive area in the pixel. M1, M3 and M4 are switches and do not exhibit much LF noise, leaving the noise of M2 as the dominant LF noise source in the front-end, despite the correlated double sampling.

LSE is applied at the source of M2 via the column bus since LSE at the gate is not possible in this circuit. Measurements [28] show that this is equivalent in terms of LF noise to applying LSE at the gate. Performing the LSE at the source has the advantage that the circuitry to pull up the column bus only needs to be replicated once per column, not once per pixel.

To investigate this noise reduction method, a test structure (Fig. 13) was designed and processed in a mature industrial 0.35- $\mu$ m process in which a device is subjected to identical bias conditions as M2 would be in a real circuit. In the noise measurements, CDS operation of the actual circuit is replicated. This

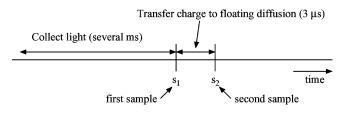


Fig. 14. Sample positions for CDS in imager.

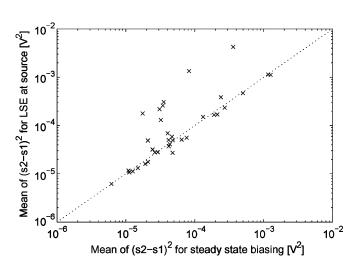


Fig. 15. Noise measurement when applying CDS.

is illustrated in Fig. 14. The simplest way to apply LSE is to first keep the device off for a relatively long time, and take a first sample of the noise 0.5  $\mu$ s after its turn-on transient  $(s_1)$ . Three  $\mu$ s later, a second sample of the noise is taken  $(s_2)$ . The mean square difference between these two samples is calculated:  $(s_2 - s_1)^2$ . This is the output noise power of the CDS, and by measuring it directly and comparing it to  $(s_2 - s_1)^2$  in the steady-state, a judgement can be made on whether subjecting M2 to LSE in this manner is useful.

In Fig. 15, measurement results obtained in this way for 35 devices with areas between 0.175  $\mu$ m<sup>2</sup> and 1.75  $\mu$ m<sup>2</sup> are given. In the figure, the noise under steady-state bias conditions is plotted along the *x*-axis, and the noise when the device is turned off briefly before the sampling instants by pulling the source terminal up to  $V_{\rm DD}$  is plotted along the *y*-axis. The diagonal line is the boundary between those devices showing more (above the line), and those showing less (below the line) noise when subjected to LSE. The majority of devices in this plot lie above the diagonal: on average,  $(s_2 - s_1)^2$  rises from  $1.5 \times 10^{-4}$  to  $3.2 \times 10^{-4}$  when the devices are subjected to LSE. Spread in the results is considerable; over two orders of magnitude for both the steady-state and the LSE measurement.

The increase in LF noise observed when the devices are subjected to LSE+CDS is rather disappointing, especially in view of the measurement results of Fig. 16, in which the same devices are subjected to LSE only, and the majority of devices show a strong noise decrease.

Analysis shows that the problem is caused by the combination of LSE and correlated double sampling. Though LSE on average reduces the LF noise of the device, the bias history of

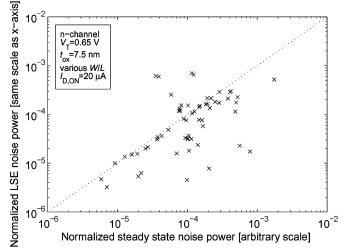


Fig. 16. Large signal excitation decreases LF noise of devices.

both sample moments is not the same, and the LF noise at both sample moments is not the same either. Because of this, the CDS operation aggravates the LF noise of the device despite the fact that the LF noise itself at each sample instant has decreased.

This is a very important observation: if CDS is to be used to good effect, not only should the bias at the sample instants be as identical as possible, but the bias history of both sample instants also needs to be identical. If CDS is carelessly applied, it is clear that this condition will not always be satisfied, and CDS may make the LF noise worse rather than improving it.

A detailed quantitative explanation of this effect is given in [28]. Obviously, an LSE biasing scheme can be devised that gives an LF noise benefit in combination with CDS. From the results above, one characteristic of such a biasing scheme is clear, namely that it should *ensure that the bias history of both sample instants is the same*. A square wave sequence with a duty cycle that is as low as possible would satisfy this requirement, where the two samples for the CDS are taken in subsequent on periods of the square wave, long after the start of the sequence.

The transient Shockley–Read–Hall model of Section III-D explains the measurement results. Applying correlated double sampling if the bias history of both sample instants is not identical will make the LF noise worse.

# D. RF Circuit Design

RF circuits can suffer from LF noise, much as baseband circuits do. Whereas in baseband circuits LF noise is in direct competition with the signal, it is upconversion of LF noise that limits the performance of many RF circuit blocks. Close-to-carrier phase noise of PLLs and VCOs, for example, is commonly dominated by LF noise. Though measures have successfully been proposed to limit upconversion of LF noise, a further reduction in LF noise is always desirable. There are two important factors that point to application of the LSE noise reduction effect in RF designs. First, it is not possible in many RF designs to apply baseband techniques such as correlated double sampling. Second, devices in many RF-CMOS circuits are operated with very large voltage swings, i.e., the devices are already being subjected to LSE by the operation of the circuit.

To ascertain whether LF noise reduction is present in RF circuits, i.e., when the devices are turned off and on at a very high frequency, measurements were performed. Results up to 3 GHz [46] indicate that the frequency of excitation does not influence the LF noise reduction and that a useful reduction of LF noise may therefore be expected in RF circuits. This again is in accordance with the theory presented in Section III.

### V. CONCLUSION

In this paper, we have tried to give circuit designers some insight into RTS noise phenomena. The common models used in circuit simulators have significant limitations when applied to small-area devices with a low number of free carriers, as the LF noise performance of these devices is dominated by Random Telegraph Signals (RTS).

The observation that in large devices, LF noise decreases when the device is subjected to large signal excitation is explained by the bias dependency of the RTS time constants coupled to the U-shaped distribution of interface states. In small devices, though the noise will go down on average, it is not possible to predict the behavior of each individual device in advance.

For circuit designers, awareness of non-steady-state LF noise phenomena is important because in many circuits, the devices are operated in a switched fashion. Under these conditions, LF noise of the devices will not be the same as during steady-state biasing. In a switched current source, this was shown to result in a significant LF noise reduction. For a correlated double sampling circuit, this means that the bias history for both sample instants must be identical if the noise reduction is to function as intended. For RF circuits where devices are rapidly switched on and off, improved LF noise performance may be expected.

The important overall conclusion is that the LF noise characteristics of a MOSFET depend not only on the present bias state of the device, but also on the bias history of the device, an effect not modelled in current (2006) circuit simulators.

#### ACKNOWLEDGMENT

Philips Research is gratefully acknowledged for providing many of the devices in this work. L. Vandamme, H. de Vries, G. Wienk, and R. Woltjer are acknowledged for their contributions to this work.

#### REFERENCES

- A. J. Annema, "Analog circuit performance and process scaling," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 711–725, Jun. 1999.
- [2] P. H. Woerlee, M. J. Knitel, R. van Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Zegers-van Duijnhoven, "RF-CMOS performance trends," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1776–1782, Aug. 2001.
- [3] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: a new perspective on individual defects, interface states and low-frequency (1/f) noise," *Advances in Physics*, vol. 38, no. 4, pp. 367–468, 1989.
- [4] R. Brederlow, W. Weber, D. Schmitt-Landsiedel, and R. Thewes, "Fluctuations of the low frequency noise of MOS transistors and their modeling in analog and RF-circuits," in *IEDM Tech. Dig.*, 1999, pp. 159–162.

- [5] I. Bloom and Y. Nemirovsky, "1/f noise reduction of metal-oxide semiconductor transistors by cycling from inversion to accumulation," *Appl. Phys. Lett.*, vol. 58, no. 15, pp. 1664–1666, Apr. 1991.
- [6] B. Dierickx and E. Simoen, "The decrease of random telegraph signal noise in metal-oxide-semicondutor field-effect transistors when cycled from inversion to accumulation," *J. Appl. Phys.*, vol. 71, no. 4, pp. 2028–2029, Feb. 1992.
- [7] A. P. van der Wel, E. A. M. Klumperink, S. L. J. Gierkink, R. F. Wassenaar, and H. Wallinga, "MOSFET 1/f noise measurement under switched bias conditions," *IEEE Electron Dev. Lett.*, vol. 21, no. 1, pp. 43–46, Jan. 2000.
- [8] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad, A. J. M. van Tuijl, and B. Nauta, "Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 1022–1025, Jul. 1999.
- [9] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van der Wel, and B. Nauta, "Reducing MOSFET 1/f noise and power consumption by switched biasing," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 994–1001, Jul. 2000.
- [10] G.-Y. Tak, S.-B. Hyun, T. Y. Kang, B. G. Choi, and S. S. Park, "A 6.3–9-GHz CMOS fast settling PLL for MB-OFDM UWB applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1671–1679, Aug. 2005.
- [11] J. Koh, R. Thewes, D. Schmitt-Landsiedel, and R. Brederlow, "A circuit design based approach for 1/f-noise reduction in linear analog CMOS IC's," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2004, pp. 222–225.
- [12] D. Baek, T. Song, E. Yoon, and S. Hong, "8-GHz CMOS quadrature VCO using transformer-based LC tank," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 446–448, Oct. 2003.
- [13] C. C. Boon, M. A. Do, K. S. Yeo, J. G. Ma, and X. L. Zhang, "RF CMOS low-phase-noise LC oscillator through memory reduction tail transistor," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 51, no. 2, pp. 85–90, Feb. 2004.
- [14] P. Larsson, "A 2-1600 MHz CMOS clock recovery PLL with low-Vdd capability," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1951–1960, Dec. 1999.
- [15] S. Ye and I. Galton, "Techniques for phase noise suppression in recirculating DLLs," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1222–1230, Aug. 2004.
- [16] T. Maeda, N. Matsuno, S. Hori, T. Yamase, T. Tokairin, K. Yanagisawa, H. Yano, R. Walkington, K. Numata, N. Yoshida, Y. Takahashi, and H. Hida, "A low-power dual-band triple-mode WLAN CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2481–2490, Nov. 2006.
- [17] C. Changhua and K. K. O, "Millimeter-wave voltage-controlled oscillators in 0.13 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1297–1304, Jun. 2006.
- [18] P. Andreani and H. Sjöland, "Tail current noise suppression in RF CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 342–348, Mar. 2002.
- [19] F. N. Hooge, "1/f noise is no surface effect," *Physica*, vol. 29A, no. 3, pp. 139–140, Apr. 1969.
- [20] A. L. McWhorter, "1/f noise and related surface effects in Germanium," Ph.D. dissertation, MIT, Cambridge, MA, 1955.
- [21] J. Chang, A. A. Abidi, and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1965–1971, Nov. 1994.
- [22] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990.
- [23] —, "A physics-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1323–1333, May 1990.
- [24] A. J. Scholten and D. B. M. Klaassen, "New 1/f noise model in MOS Model 9, Level 903," Philips Research Nat. Lab., Unclassified Report 816/98, 1998 [Online]. Available: http://www.nxp.com/ Philips\_Models/mos\_models/model9/
- [25] Y. Tsividis, Operation and Modeling of the MOS Transistor. Oxford, U.K.: Oxford Univ. Press, 2003.
- [26] A. van der Ziel, "Unified presentation of 1/f noise in electronic devices: fundamental 1/f noise sources," *Proc. IEEE*, vol. 76, no. 3, pp. 233–258, Mar. 1988.
- [27] S. Machlup, "Noise in semiconductors: spectrum of a two-parameter random signal," J. Appl. Phys., vol. 25, no. 3, pp. 341–343, Mar. 1954.

- [28] A. P. van der Wel, "MOSFET LF noise under large signal excitation: Measurement, modelling and application," Ph.D. dissertation, Univ. Twente, Enschede, Netherlands, 2005 [Online]. Available: http://purl. org/utwente/50425
- [29] T. G. M. Kleinpenning, "On 1/f noise and random telegraph noise in very small electronic devices," *Physica B*, vol. 164, pp. 331–334, Apr. 1990.
- [30] M. Toita, L. K. J. Vandamme, S. Sugawa, A. Teramoto, and T. Ohmi, "Geometry and bias dependence of low-frequency random telegraph signal and 1/f noise levels in MOSFETS," *Fluctuation Noise Lett.*, vol. 5, no. 4, pp. L539–L548, 2005.
- [31] M. Schulz and H. H. Mueller, "Single-electron trapping at semiconductor interfaces," *Adv. Solid State Phys.*, vol. 35, pp. 229–241, 1996.
  [32] W. Shockley and W. T. Read, Jr., "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.
- holes and electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952.
  [33] Z. Çelik-Butler, P. Vasina, and N. V. Amarasinghe, "A method for locating the position of oxide traps responsible for random telegraph signals in submicron MOSFETs," *IEEE Trans. Electron Devices*, vol. 47,
- [34] N. B. Lukyanchikova, M. V. Petrichuk, and N. P. Garbar, "Asymmetry of the RTSs capture and emission kinetics in nMOSFETs processed in a 0.35 μm CMOS technology," in *Proc. 14th Int. Conf. Noise in Physical*
- Systems and 1/f Fluctuations (ICNF), 1997, pp. 232–235.
  [35] E. Hoekstra, "Random telegraph noise in MOSFETs—Time domain analysis under transient conditions," Master's thesis, Univ. Twente, En-
- schede, Netherlands, Aug. 2004.
  [36] Z. Shi, J. Miéville, and M. Dutoit, "Random telegraph signals in deep submicron n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 41, no. 7, pp. 1161–1168, Jul 1994.
- 7, pp. 1161–1168, Jul. 1994.
   [37] J. S. Kolhatkar, A. P. van der Wel, E. A. M. Klumperink, C. Salm, B. Nauta, and H. Wallinga, "Measurement and extraction of RTS parameters under switched biased conditions in MOSFETS," in *Proc. 17th Int. Conf. Noise and Fluctuations (ICNF)*, Aug. 2003, pp. 237–240.
   [38] J. S. Kolhatkar, "Steady-state and cyclo-stationary RTS noise in MOS-
- [38] J. S. Kolhatkar, "Steady-state and cyclo-stationary RTS noise in MOS-FETs," Ph.D. dissertation, Univ. Twente, Enschede, Netherlands, 2005 [Online]. Available: http://www.purl.org/utwente/48261
- [39] E. Hoekstra, "Large signal excitation measurement techniques for RTS noise in MOSFETs," in *Proc. EUROCON*, Nov. 2005, vol. 2, pp. 1863–1866.
- [40] J. S. Kolhatkar, E. Hoekstra, C. Salm, A. P. van der Wel, E. A. M. Klumperink, J. Schmitz, and H. Wallinga, "Modelling of RTS noise in MOSFETs under steady-state and large-signal excitation," in *IEDM Tech. Dig.*, Dec. 2004, pp. 759–762.
  [41] A. P. van der Wel, E. A. M. Klumperink, E. Hoekstra, and B. Nauta,
- [41] A. P. van der Wel, E. A. M. Klumperink, E. Hoekstra, and B. Nauta, "Relating random telegraph signal noise in metal-oxide-semiconductor transistors to interface trap energy distribution," *Appl. Phys. Lett.*, vol. 87, no. 18, Oct. 2005.
- [42] A. P. van der Wel, E. A. M. Klumperink, and B. Nauta, "Effect of switched biasing on 1/f noise and random telegraph signals in deepsubmicron MOSFETs," *Electron. Lett.*, vol. 37, no. 1, pp. 55–56, Jan. 2001.
- [43] X. L. Xu, R. T. Kuhn, J. J. Wortman, and M. C. Öztürk, "Rapid thermal chemical vapor deposition of thin silicon oxide films using silane and nitrous oxide," *Appl. Phys. Lett.*, vol. 60, no. 24, pp. 6063–6065, Jun. 1992.
- [44] K. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete resistance switching in submicrometer silicon inversion layers: individual interface traps and low-frequency (1/f) noise," *Phys. Rev. Lett.*, vol. 52, no. 3, pp. 228–231, Jan. 1984.
- [45] A. El Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 6–20, May-Jun. 2005.
  [46] A. P. van der Wel, E. A. M. Klumperink, and B. Nauta, "Measurement of the sensor of the se
- [46] A. P. van der Wel, E. A. M. Klumperink, and B. Nauta, "Measurement of MOSFET LF noise under large signal RF excitation," in *Proc. 32nd Eur. Solid-State Device Research Conf. (ESSDERC)*, Sep. 2002, pp. 91–95.



He is presently working for NXP Research (Formerly Philips Research) in Eindhoven, The Netherlands, in the mixed-signal circuits and systems group.



**Eric A. M. Klumperink** (M'98) was born on April 4, 1960, in Lichtenvoorde, The Netherlands. He received the B.Sc. degree from HTS, Enschede, The Netherlands, in 1982. After a short period in industry, he joined the Faculty of Electrical Engineering of the University of Twente in 1984, where he was mainly engaged in analog CMOS circuit design and research. This resulted in several publications and a Ph.D. thesis, in 1997, on the subject of "Transconductance Based CMOS Circuits".

He is currently an Associate Professor at the

IC-Design Laboratory and also involved in the CTIT Research Institute. He holds four patents and has authored or co-authored more than 50 journal and conference papers. His research interest is in design issues of high-frequency CMOS circuits, especially for front-ends of integrated CMOS transceivers.

Since 2006, Dr. Klumperink has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS. He is a correcipient of the IEEE ISSCC 2002 Van Vessem Outstanding Paper Award.



Jay S. Kolhatkar received the B.E. degree in electronics from University of Bombay (now Mumbai), India, and the M.Tech. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1999. In January 2005, he received the Ph.D. degree from the University of Twente, Enschede, The Netherlands, in the Semiconductor Components group, on the subject of steady-state and cyclostationary RTS noise in MOSFETs. Prior to his Ph.D., he was with Mentor Graphics (India) Private Limited, Hyderabad, India, in the Design for

Test group.

Currently, he is in the Process and Library Technology group at NXP Semiconductors, Nijmegen, The Netherlands. His areas of research interest include semiconductor device modeling and analog (RF) circuit design.



Eric Hoekstra was born in Wirdum, The Netherlands, in 1979. He received the B.Sc. degree in electrical engineering from the Noordelijke Hogeschool Leeuwarden in 2001. In 2004, he received the M.S. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, The Netherlands. During his study, he investigated the effect of hot-carrier stress on the low-frequency noise in hydrogen- or deuterium-passivated MOSFETs. His Master assignment focused on the time domain analysis of random telegraph noise in MOSFETs

under transient conditions. Currently, he is working towards the Ph.D. degree at the same university, in the IC-Design group of the CTIT Research Institute.

His research focuses on the measurement of local performance parameters in advanced digital circuits.



**Martijn F. Snoeij** (S'99) was born in Zaandam, The Netherlands, in 1977. In 2001, he received the M.Sc. degree in electrical engineering (*cum laude*) from Delft University of Technology. The title of his M.Sc. thesis was "A Low Power Sigma-Delta ADC for a Digital Microphone". From August to December 2000, he did an internship at National Semiconductor, Santa Clara, CA, where he worked on precision comparators and amplifiers. Since 2002, he has been a Research Assistant at Delft University, where he is working towards the Ph.D. degree.

The main focus of his work is on the design of improved analog-to-digital converters for CMOS image sensors, leading to higher sensor performance and lower power consumption. His research interests include analog and mixedsignal circuit design and sensors.



**Cora Salm** (M'99) received the M.Sc. degree in applied physics and the Ph.D. degree in electrical engineering at the University of Twente, Enschede, The Netherlands, in 1993 and 1997, respectively. Her Ph.D. dissertation dealt with the materials and electrical properties of poly-crystalline silicon-germanium for advanced CMOS technologies.

In 1998, she joined the Semiconductor Components group of the MESA+ Research Institute of the University of Twente as an Assistant Professor with specialization in device reliability and novel

technologies. She has authored or co-authored 25 papers and 30 international conference contributions. Her research interests include dielectric reliability, failure physics and the technological and physical aspects of novel device concepts. She lectures on advanced semiconductor devices and reliability engineering.

Dr. Salm is a member of the IEEE Electron Device Society and is presently regional editor of the EDS newsletter.



Hans Wallinga received the M.Sc. degree in applied physics from the University of Utrecht and the Ph.D. degree from the University of Twente, Enschede, The Netherlands.

He started his career at the University of Twente with research on the physics of semiconductor devices, in particular MOS transistors. He was involved in discrete time analog signal processing and basic analog circuits. He taught courses on semiconductor devices and on discrete-time signal processing. He subsequently headed the group on IC-technology and

electronics and the group on Semiconductor Components in the Faculty of Electrical Engineering of the University of Twente. The research activities of these groups were incorporated in the MESA Research Institute. In the last years of his active career, he was Dean of the Faculty of Electrical Engineering and the Faculty of Computer Science of the University of Twente. He now enjoys his retirement.



**Bram Nauta** (M'91–SM'03) was born in Hengelo, The Netherlands, in 1964. In 1987, he received the M.Sc. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991, he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high-speed AD converters and analog key modules.

In 1998, he returned to the University of Twente, as full Professor heading the IC-Design group, which is part of the CTIT Research Institute. His current research interest is high-speed analog CMOS circuits. He is also a part-time consultant in industry, and in 2001 he co-founded Chip Design Works. His Ph.D. thesis was published as a book: *Analog CMOS Filters for Very High Frequencies* (Springer, 1993).

Dr. Nauta received the Shell Study Tour Award for his Ph.D. work. From 1997 to 1999, he served as Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, ANALOG AND DIGITAL SIGNAL PROCESSING, and in 1998 he served as Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. From 2001 to 2006, he was Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is a member of the technical program committees of ISSCC, ESS-CIRC, and Symposium on VLSI Circuits. He is co-recipient of the ISSCC 2002 Van Vessem Outstanding Paper Award.