

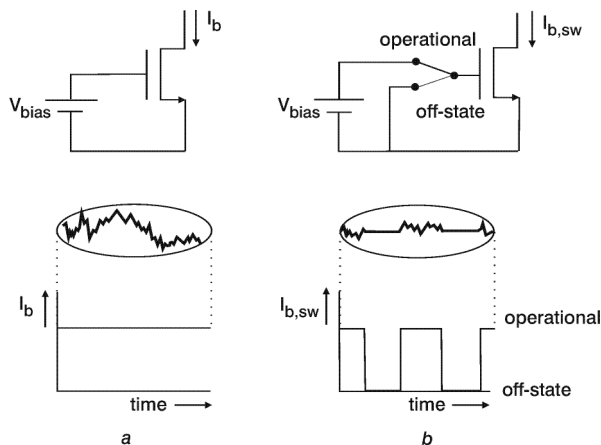
Effect of switched biasing on $1/f$ noise and random telegraph signals in deep-submicron MOSFETs

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Switched bias noise measurements on relatively large ($> 0.8\mu\text{m}$) n -channel MOSFETs have been reported in the literature. Measurements are presented on $0.2/0.18\mu\text{m}$ n -channel MOSFETs the noise performance of which seems to be dominated by the effect of a small number of interface states. Switched biasing is seen to influence the dynamic behaviour of these states, and reduce the noise of the devices.

Introduction: $1/f$ noise is an important problem in analogue circuits, and may dominate over thermal noise at frequencies far into the MHz region in current CMOS processes. In many situations, the $1/f$ noise limits the noise performance of the analogue circuit. Since $1/f$ noise scales with the inverse of the area of the device, newer, smaller devices make the study of $1/f$ noise ever more relevant. Common $1/f$ noise reduction techniques such as chopping [1] or correlated double sampling [2] reduce the effect of the $1/f$ noise; the noise source itself is left alone. In contrast, switched biasing (switching between strong inversion and accumulation) interferes with the physical noise generation process to reduce the low-frequency noise coming from the device [3, 4]. Other $1/f$ noise reduction techniques can only be applied in baseband, while switched biasing might be used to reduce $1/f$ noise in RF systems, where $1/f$ noise is upconverted to appear as sidebands of the desired spectrum [5].

Measurements: In this Letter, switched bias measurements of a $0.18\mu\text{m}$ process ($t_{\text{ox}} = 4\text{nm}$) are given. Measurements were performed on 21 minimum-size n -channel devices, with a W/L of $0.2\mu\text{m}/0.18\mu\text{m}$. V_i was $\sim 0.35\text{V}$.



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Fig. 1 Switched bias compared to constant bias: periodic switching to 'rest-state' close to accumulation reduces intrinsic low frequency $1/f$ noise [3, 4, 6]

a Constant bias
b Switched bias

To carry out the switched bias measurements, the method and setup from [6] were used. This setup enabled us to measure the noise power spectrum of the device in both the steady state and under switched bias conditions (see Fig. 1).

A probestation was used to allow on-wafer measurements of the samples to be taken. For each device, normal functionality was first verified, as was the absence of excess gate leakage current. The MOSFETs were operating in strong inversion and in saturation. V_g was $\sim 1.2\text{V}$; V_{ds} was 1V . In all cases, I_d was $80\mu\text{A}$.

We measured the output current noise power density. This is referred to input by dividing by g_m^2 . To simplify the comparison of a large number of devices, an empirical measure for the 'noisiness' of each device is needed. To this end, the measured noise power spectrum is integrated from 10 to 150Hz. This gives an empirical measure of the LF noise power coming from the device. This integration is performed both for the steady state case and for the switched bias case. The difference between these two averages gives the raw noise reduction for switched biasing. Since one would expect, on mathematical grounds, the raw

switched bias measurement to exhibit 6dB less noise than the steady state case [6], a correction factor is applied: 6dB is subtracted from the raw noise reduction; this gives the net noise reduction. This net noise reduction comes from a change in the noise generation process in the MOSFET.

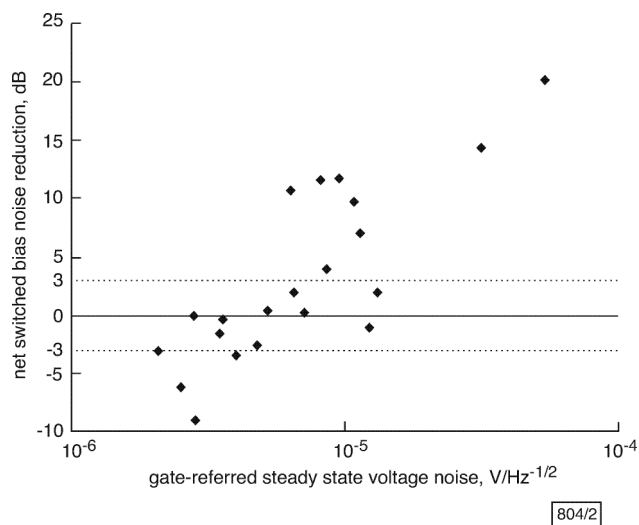


Fig. 2 Switched bias noise reduction against steady-state voltage noise

21 devices, $0.2/0.18\mu\text{m}$ NMOST, $V_{gs,on} = 1.2\text{V}$, $V_{gs,off} = 0\text{V}$, switching frequency = 10kHz , duty cycle = 50%, measurement bandwidth: 10 – 150Hz

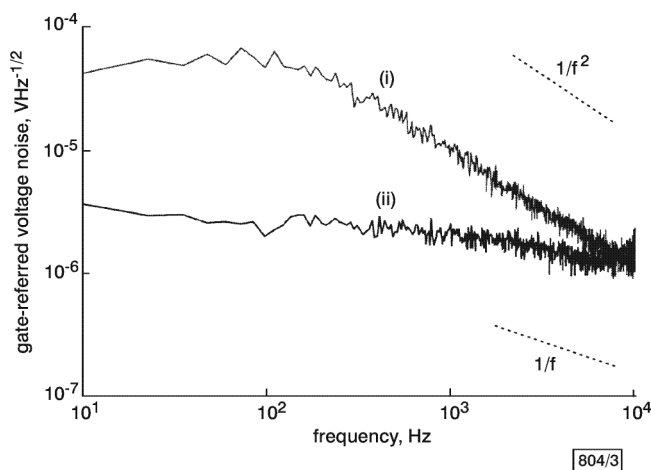


Fig. 3 Device exhibiting strong random telegraph noise shows significant noise reduction under switched biasing

(i) steady state
(ii) switched bias

In Fig. 2, the net noise reduction by switched biasing is plotted against the gate-referred input noise voltage in the steady state. In this Figure, we can identify three classes of MOSFET.

(i) Devices with a significant noise reduction (eight devices with $> 3\text{dB}$ net noise reduction). These devices are those displaying significant steady state $1/f$ noise. Fig. 3 shows such a device which has strong random telegraph (RT) noise with a $1/f^2$ dependence. Switched biasing reduces the noise from this device by $> 20\text{dB}$.

(ii) Three devices with significantly ($> 3\text{dB}$) increased LF noise under switched biasing. In these devices, noise sources that were not present in the steady state case seem to be activated by switched biasing! One might be worried that this precludes application of the switched bias method, but it is the least noisy devices that fall into this category.

(iii) A number of 'average' devices. The noise of these devices does not change significantly. Some show a little reduction, others a slight increase in noise under switched bias conditions. Note that, on average, the noise of the devices falls under switched biasing.

Significance of results: The significance of the results is twofold. From a device physical viewpoint, they are interesting because these are the first measurements of deep submicron MOSFET noise under switched bias

conditions. Also, to the best of our knowledge, we are the first to observe an increase in RT noise when cycling a MOSFET from inversion to accumulation.

From a circuit design standpoint, the results are interesting, because the most noisy devices give the best improvement under switched biasing. This means that the yield improves. Even if some devices show an increase in noise under switched bias conditions, it appears that these are the least noisy devices. More measurements need to be done here, and the present measurements highlight the importance of measuring a significant number of devices.

It is interesting to note that in measurements on large devices, a noise reduction under switched biasing was systematically found [6]. In the submicron measurements presented here, there is a noise reduction on average, though individual devices show large spread. This might be explained by assuming that the $1/f$ noise in the large devices comes from a superposition of the RT noise of many different interface states (the McWhorter model): in large devices with a large number of interface states, the activity of the states is, on average, reduced. In small devices, where typically the activity of one or only a few traps is seen, the RT noise of the device may increase or decrease depending on the precise parameters of the trap. On average, however, the noise still decreases.

Conclusion: 'Switched bias' measurements of modern deep-submicron n -channel MOSFETs are presented. Several interesting conclusions may be drawn from the measurement results: switched bias gives, on average, a decrease in the noise of n -channel MOSFETs. We find that different samples react differently to switched biasing. While most devices show a decrease in LF noise, some devices may show an increase in LF noise. However, switched biasing seems to be useful for circuit design, as the most noisy devices, those limiting circuit yield, show the largest decrease in noise under switched bias conditions.

Apart from being useful to circuit design, switched biasing may yield useful insight into the noise generation process of the transistor, as it

probes dynamic effects that are not evident in steady-state noise measurements.

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References

- 1 ENZ, C., VITTOZ, E.A., and KRUMMENACHER, F.: 'A CMOS chopper amplifier', *IEEE J. Solid-State Circuits*, 1987, **SC-22**, (3), pp. 335–342
- 2 KANSY, R.J.: 'Response of a correlated double sampling circuit to $1/f$ noise', *IEEE J. Solid-State Circuits*, 1980, **SC-15**, (3), pp. 373–375
- 3 BLOOM, I., and NEMIROVSKY, Y.: ' $1/f$ noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation', *Appl. Phys. Lett.*, 1991, **58**, (15), pp. 1664–1666
- 4 GIERKINK, S.L.J., KLUMPERINK, E.A.M., VAN DER WEL, A.P., HOOZGAAD, G., VAN TUIJL, A.J.M., and NAUTA, B.: 'Intrinsic $1/f$ device noise reduction and its effect on phase noise in CMOS ring oscillators', *IEEE J. Solid-State Circuits*, 1999, **34**, (7), pp. 1022–1025
- 5 KLUMPERINK, E.A.M., GIERKINK, S.L.J., VAN DER WEL, A.P., and NAUTA, B.: 'Reducing MOSFET $1/f$ noise and power consumption by switched biasing', *IEEE J. Solid-State Circuits*, 2000, **35**, (7), pp. 994–1001
- 6 VAN DER WEL, A.P., KLUMPERINK, E.A.M., GIERKINK, S.L.J., WASSENAAR, R.F., and WALLINGA, H.: 'MOSFET $1/f$ noise measurement under switched bias conditions', *IEEE Electron Device Lett.*, 2000, **21**, (1), pp. 43–46
- 7 DIERICKX, B., and SIMOEN, E.: 'The decrease of random telegraph signal noise in metal-oxide-semiconductor field-effect transistors when cycled from inversion to accumulation', *J. Appl. Phys.*, 1992, **71**, (4), pp. 2028–2029