Systematic Generation of WideBand Low-Noise Amplifier Topologies for CMOS Transceivers

Federico Bruccoleri, Eric A. M. Klumperink and Bram Nauta

University of Twente,MESA Research Institute,
IC-Design Group
P.O. BOX 217, 7500 AE Enschede The Netherlands
Phone: +31 (0)53 - 489 2643   Fax +31-53-489 2799

E-mail: F.Bruccoleri@el.utwente.nl

WWW: http://icd.el.utwente.nl

Abstract— **In this paper wide band inductorless Low-Noise Amplifier (LNA) topology alternatives for highly integrated CMOS transceivers are investigated. A methodology which systematically generates all the possible LNA topologies with 2 transistors in the signal path is presented. Next to well-known circuits (CG-stage and shunt series-feedback CS-stage), two novel LNA topologies are found. Hand calculations indicate that these topologies have attractive noise and intermodulation properties.**

Fig. 1. The MOS transistor to graph transformation and vv.

I. AIM AND MOTIVATION

On the road towards a complete transceiver on a single CMOS chip, the availability of high performance RF CMOS analogue building blocks is a key issue. The Low-Noise Amplifier(LNA) in the receiver path is one of these blocks. High performance LNAs are typically designed employing inductor-based narrow-band techniques. However, this is not the only design option. Although wide band inductorless LNAs provide a broadband gain and source impedance matching typically at the cost of some increase in noise figure, there are important reasons to consider them too:

- For simultaneous processing of several signal channels in Wired Cable TV Receivers (50-900Mhz), high-data rate communications systems and base stations.
- For short-distance wireless applications like Wireless Integrated Network Sensors[4] and "Blue tooth"[5] where the noise figure requirement can be relaxed avoiding problems associated with integrated inductors: large area, low self-resonance frequency and need of accurate tuning [3].

Many papers on wide band inductorless LNAs have been published. A close look to them reveals *only few essentially different circuit concepts* (e.g. CG-stage and shunt series-feedback CS-stage). The latter are simple topologies which can be modelled as 2 Voltage Controlled Cur-
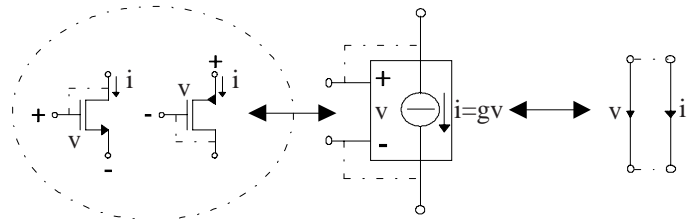
rent Sources (VCCSa and VCCSb) circuits[1,2]. Cascading and cascoding techniques have been used extensively to boost the performance of few consolidated topologies. However, this approach has an important limitation: circuit performance can be improved to a certain extent ultimately bounded by the topology concept itself. Our aim is to find out whether there are others LNA topologies with 2-transitors suitable for highly integrated CMOS transceivers. To do so, a systematic methodology which generates *all the possible* LNA topology alternatives has been developed. This is done using graphs theory to investigate topologic properties. Since a MOS transistor (in saturation) can be seen as a VCCS and the latter as a graph(see Fig.1), a method recently developed[1,2] in which a database with *all the possible* graphs of circuits with 2 VCCSs (VCCSa and VCCSb) a source and a load were generated, is used as starting point. In this database,
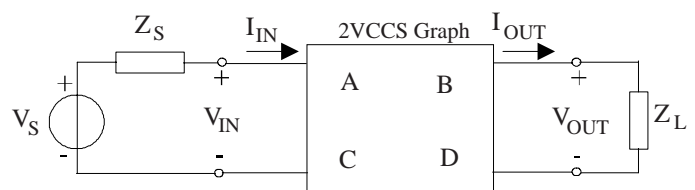

Fig. 2. Two-port model (and transmission parameters definition) representing a 2VCCS graph.

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each 2VCCS circuit is modelled as a two-port and described by transmission parameters {A,B,C,D}(Fig.2). Parameters {A,B,C,D} are function of the transconductance g_a and g_b of VCCSa and VCCSb. The graphs are then classified with respect to: (a) Non-zero Transmission parameters. (b) Transmission parameters expressions of g_a and g_b.

II. METHOD

The generation proceeds along the following steps:

1. Proper source/load impedance conditions (Z_S=50Ω and Z_L=1/SC$_L$) and LNA functional requirements (such as input/output impedance, forward voltage gain and unconditional stability) suitable for highly integrated CMOS transceivers are established.

2. Translate the information of step 1. into requirements for the transmission parameters {A,B,C,D}: (a) Useful combinations of non-zero transmission parameters. (b) Constraints on the value of the transmission parameters.

3. *All the possible* 2VCCS graphs which do not meet the previous two-port parameter requirements are then rejected. The remaining topologies are the output of the generation methodology.

Two crucial figure of merit of the LNA are analysed to highlight different properties of these topologies: the noise Figure(F) and $2^{nd}/3^{rd}$ order Input-referred intermodulation distortion Intercepts Points (IIP2 and IIP3). This is done by means of hand calculations (using a square-law model with a θ-model for the mobility degradation), assuming source impedance matching (Z_{IN}=50Ω) and a common minimum power consumption (corresponding to an input device Mb biased just in strong inversion with V_{GT}=V_{GS}-V_{T0}=0.2 V) as basic comparison conditions.

III. MAIN RESULTS

The output of the generation methodology are the 4 LNA topologies shown in Fig. 3. Next to well-known circuits (ABCD1 and ABCD3 are respectively: CG-stage and shunt series-feedback CS-stage), two alternative LNA topologies (ABC1 and ABCD2) are found. These, as far the authors are aware, are novel LNA topologies which were not previously reported in literature.

In Fig.4 the noise figure is plotted as function of the forward gain. Topology ABCD2 shows the lowest noise figure (3dB) which is also independent on the gain (which may be useful when a variable gain function is required).

Fig.5 shows IIP2 and IIP3 as function of the topology forward gain. Topology ABCD2 exhibits a IIP2 larger than 15 dBm (see figure caption for definition) over the whole gain range. This makes this topology potentially useful for
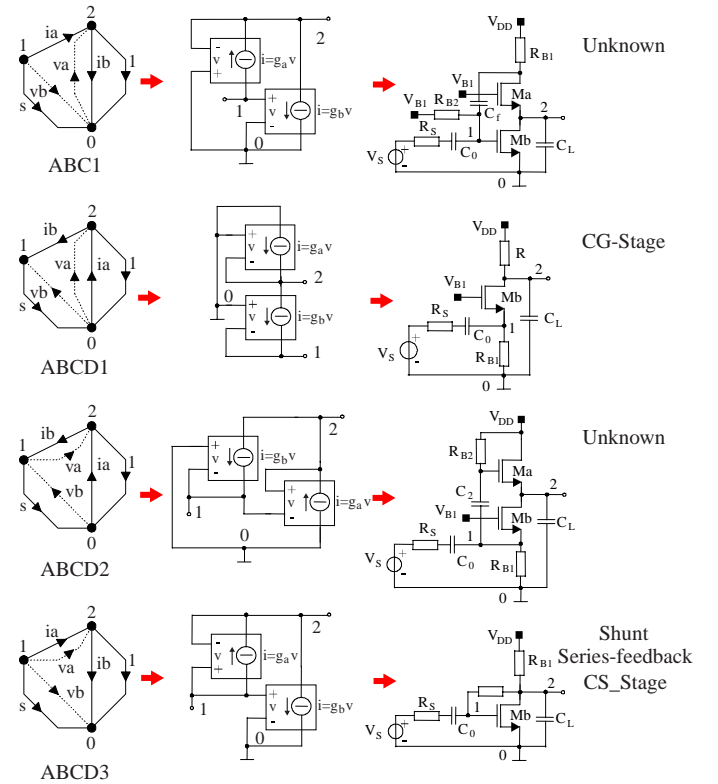

Fig. 3. The Graph, VCCS and nMOST representation of the selected LNA topologies. Relevant components in the biasing path are also shown.
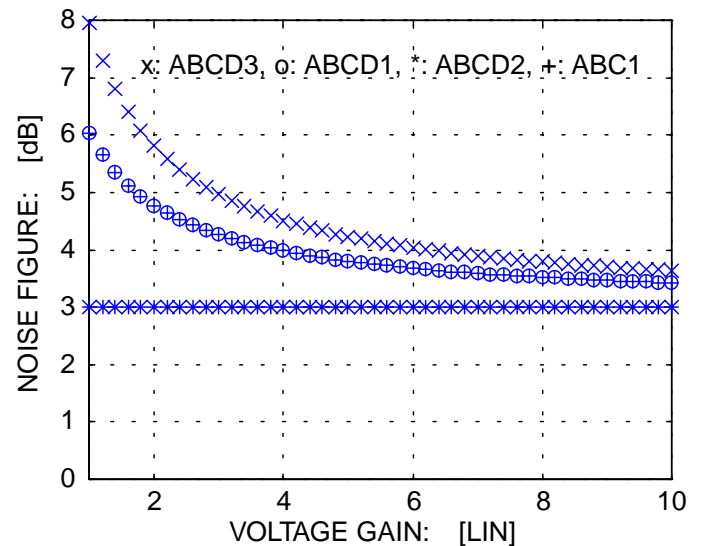

Fig. 4. Noise Figure as function of the forward gain.

zero-IF receiver. Topology ABC1 provides a IIP3 larger than 4 dBm over the whole gain range. Important aspects such as reverse gain and optimal dimensioning have not been taken into account. In the next future this must be investigated.
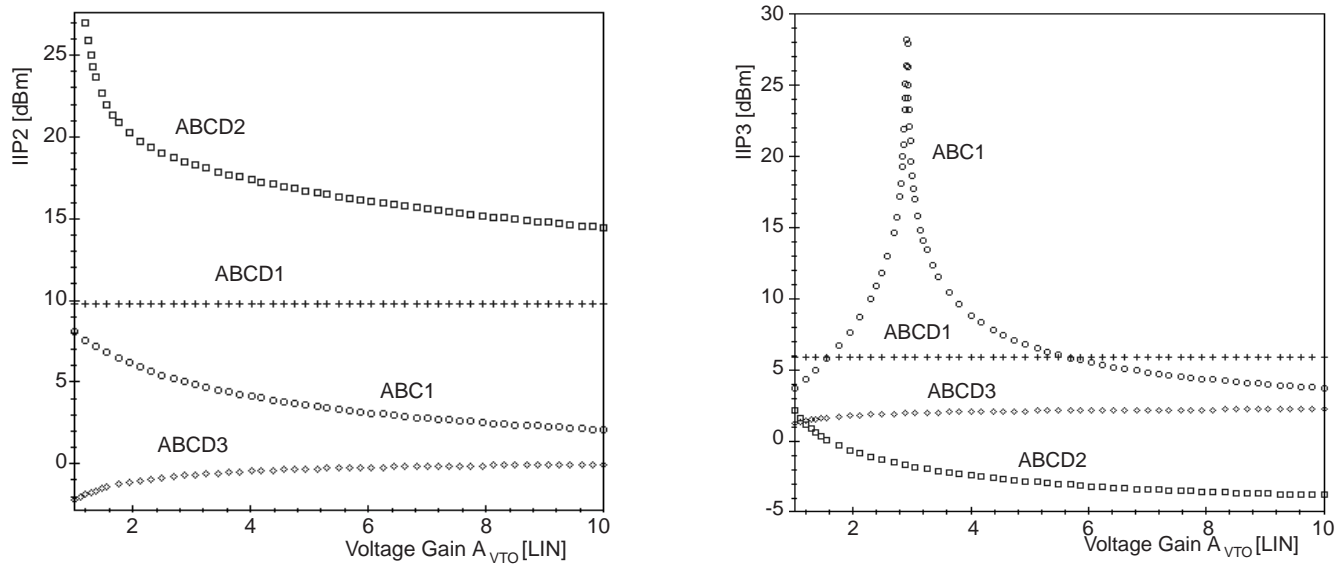
Fig. 5. IIP2 and IIP3 as function of the gain expressed in dBm. The mobility reduction parameter θ=0.7

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