Reduction of Intrinsic 1/f Device Noise in a CMOS Ring Oscillator

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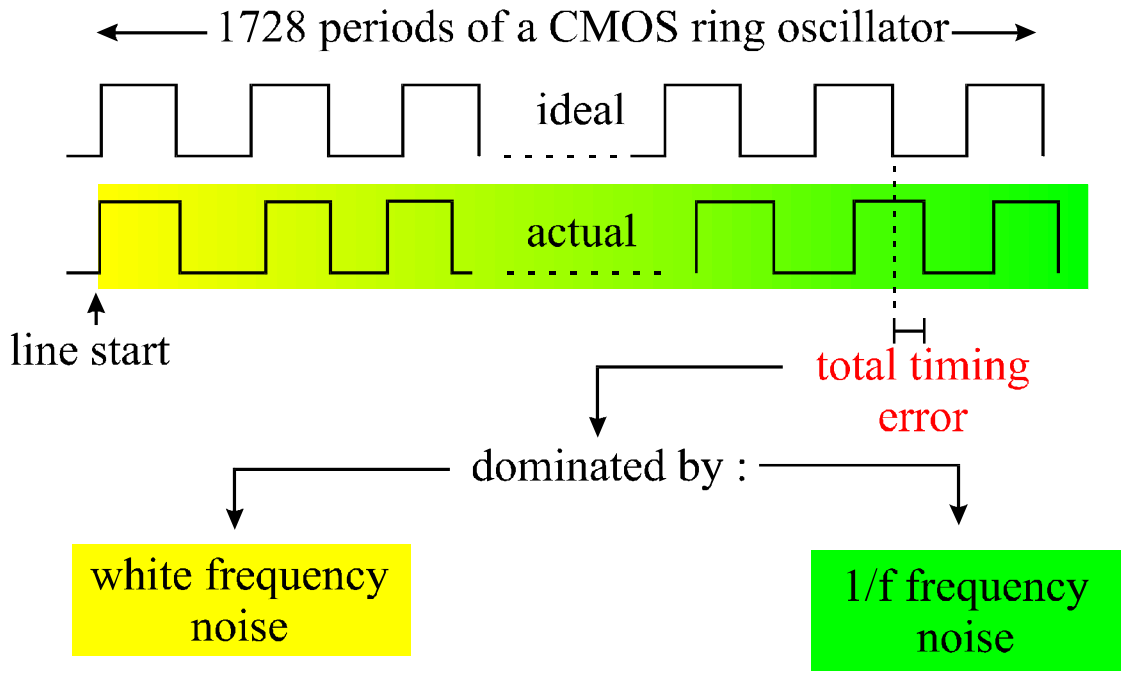
Outline

- Introduction
- 1/f device noise under switched bias conditions $\Rightarrow$ reduction !
- (How) does 1/f noise reduction appear in a ring oscillator ?
- Ring oscillator phase noise measurements
- Conclusions

Introduction

pixel clock generation
in a
100 Hz TV

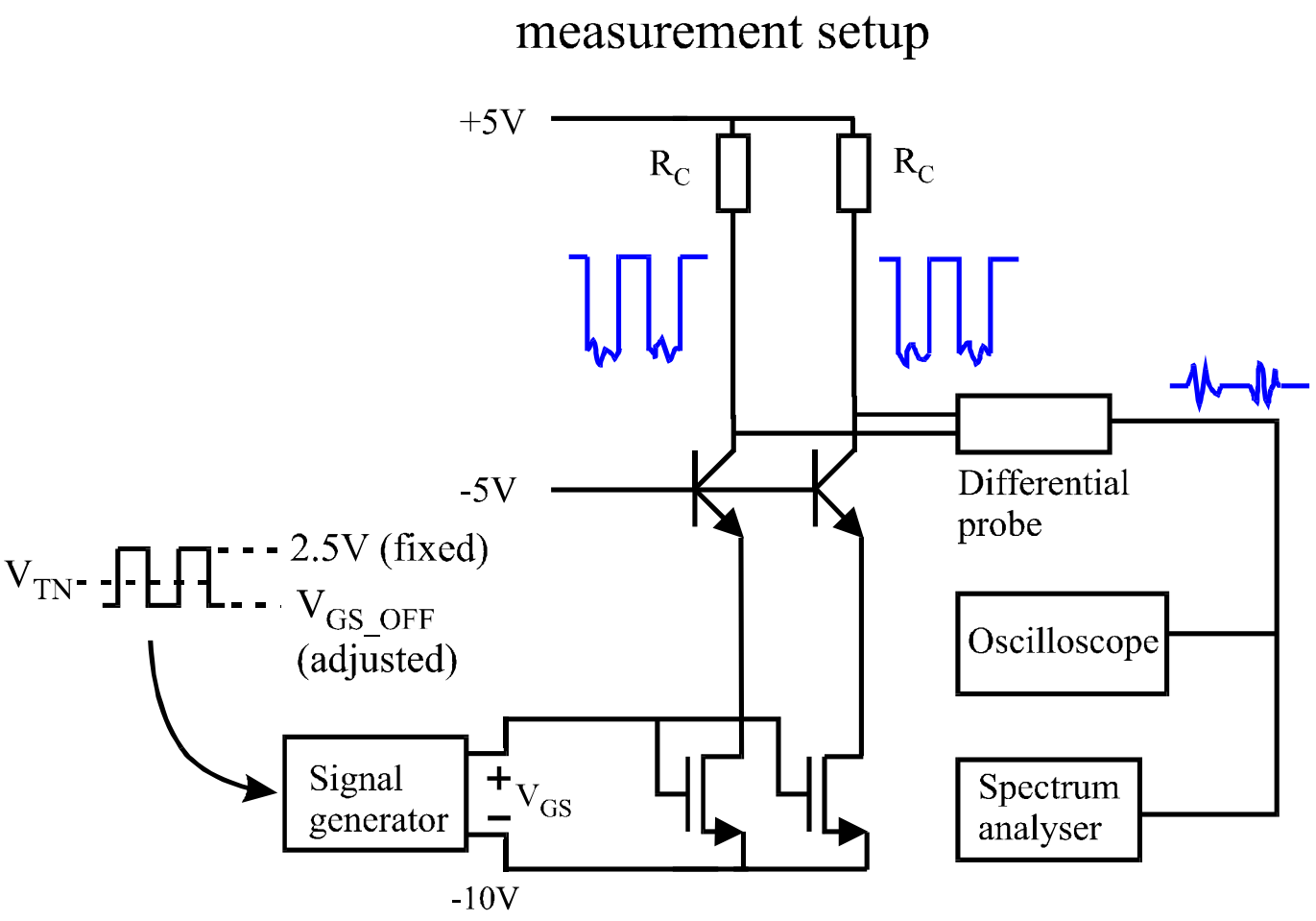


- Jitter measurements : lower 1/f frequency noise contribution than expected

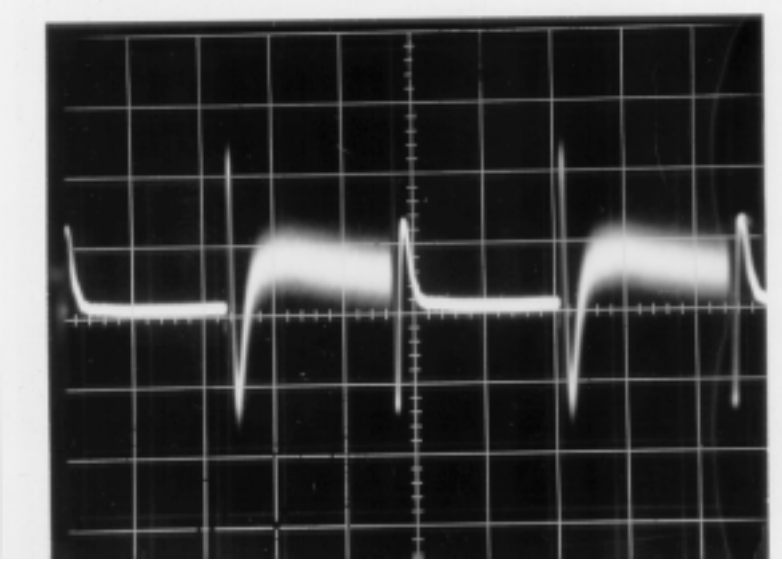
⇒ **does the intrinsic MOS 1/f noise change due to periodical switching ?**

⇒ **(how) does this affect a ring oscillator's phase noise ?**

1/f device noise under switched bias conditions



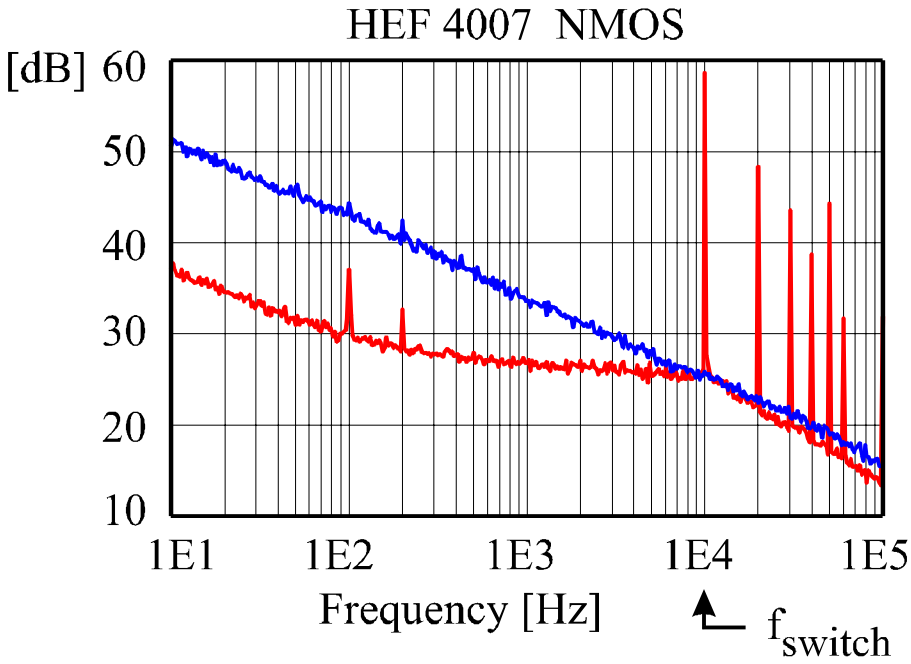
Baseband measurement result



↑ 2mV/DIV → 20µs/DIV

probe gain : 5x

f_{switch} = 10kHz



not switched , V_{GS}= 2.5V

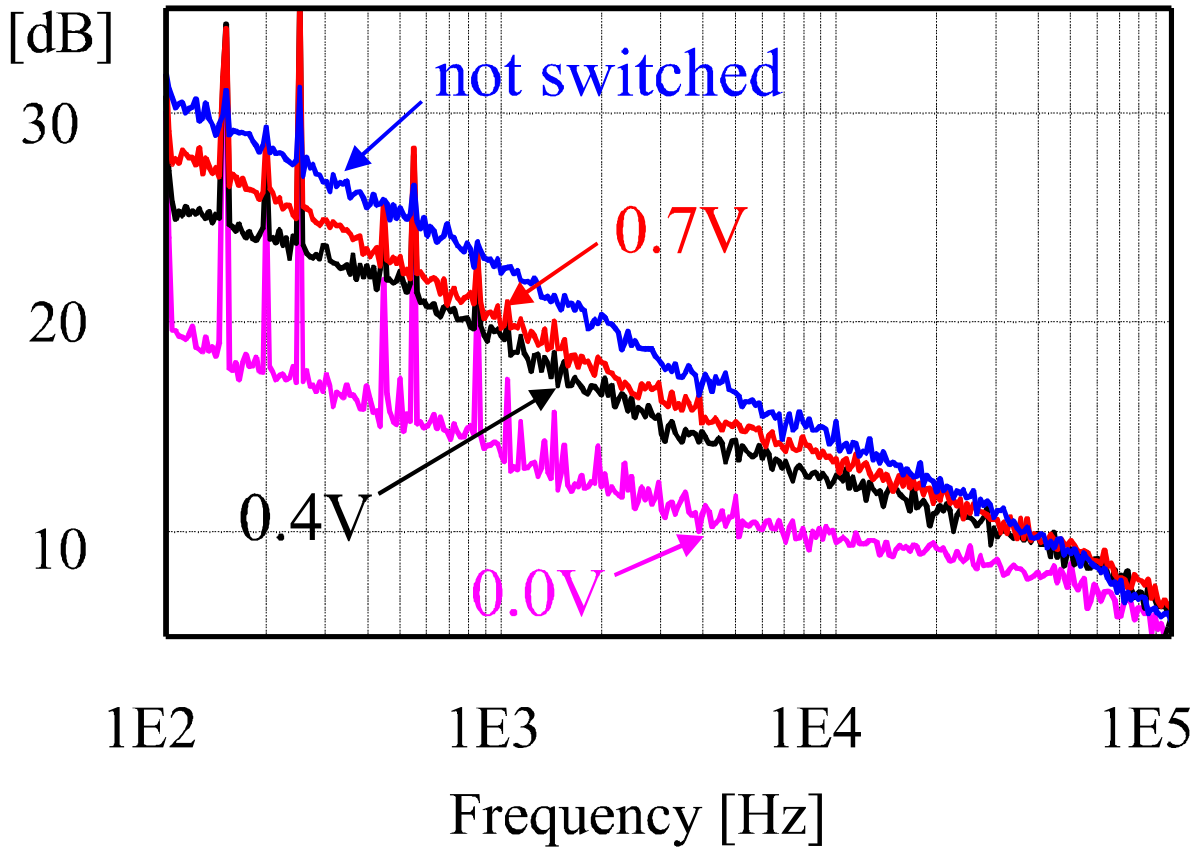
V_{GS_ON} = 2.5V , V_{GS_OFF} = 0V

Duty cycle = 50%

switching of MOS transistor → reduction of *intrinsic* 1/f device noise

[see also : Bloom & Nemirovsky , Applied Physics Letters 1991]

How does V_{GS_OFF} affect the baseband 1/f noise spectrum ?



HEF 4007 NMOS

V_{GS_ON} = 2.5V

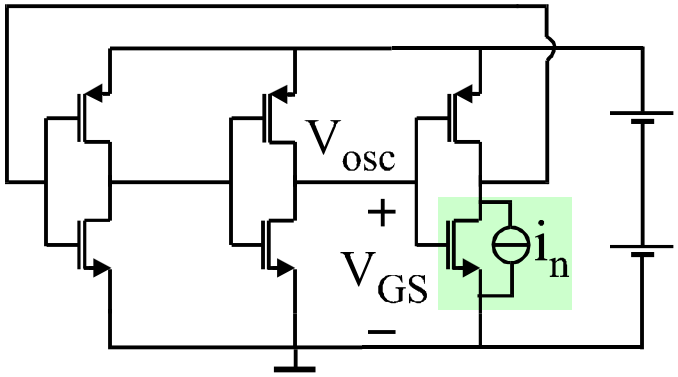
V_T = 1.5V

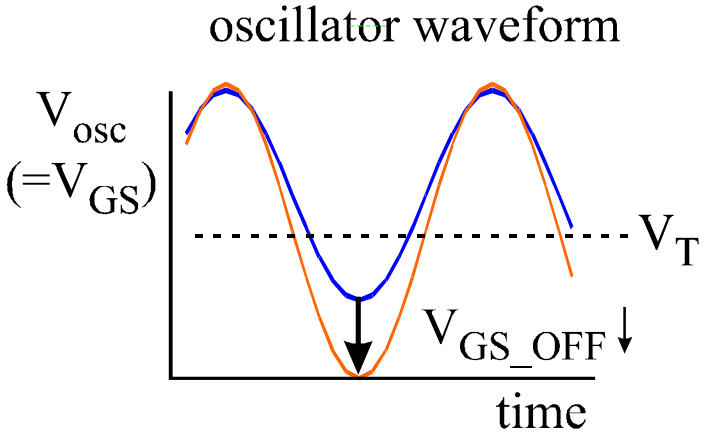
f_{switch} = 2MHz

Duty cycle = 50%

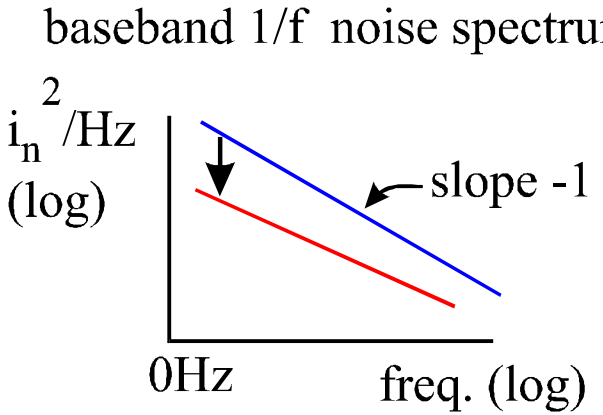
$V_{GS\_OFF} \downarrow \Rightarrow$ intrinsic MOS 1/f noise $\downarrow$

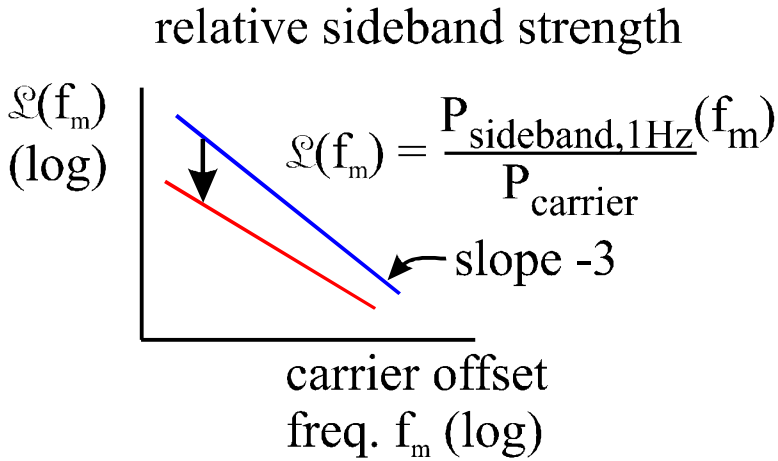
(How) does 1/f noise reduction appear in a ring oscillator ?



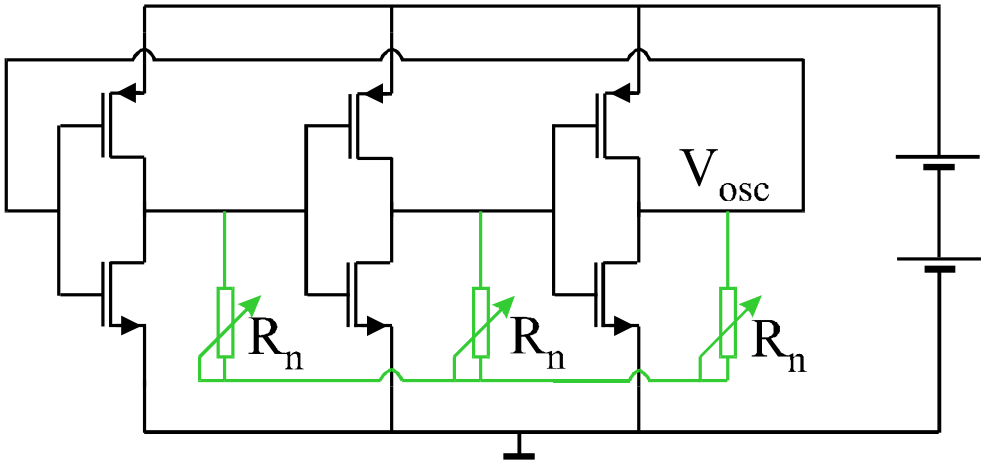


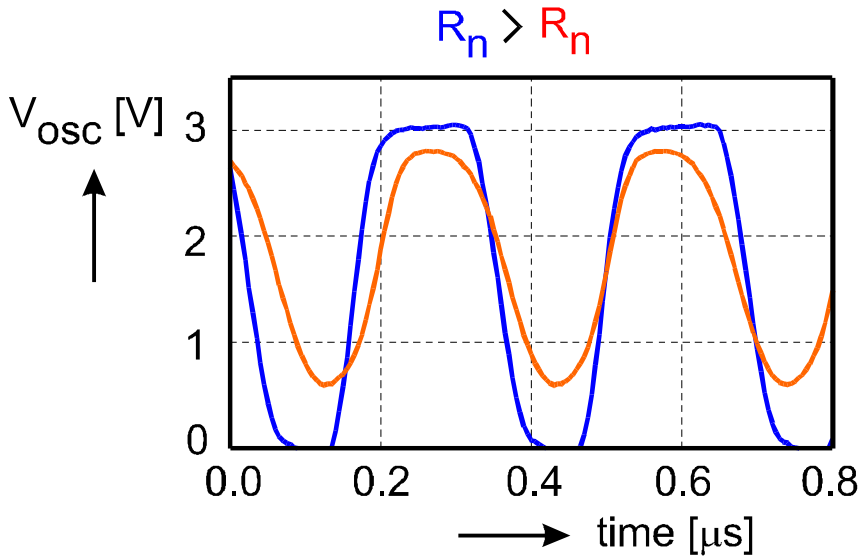
upconversion
(freq. modulation)





How to vary the V_{GS_OFF} of the transistors easily ?



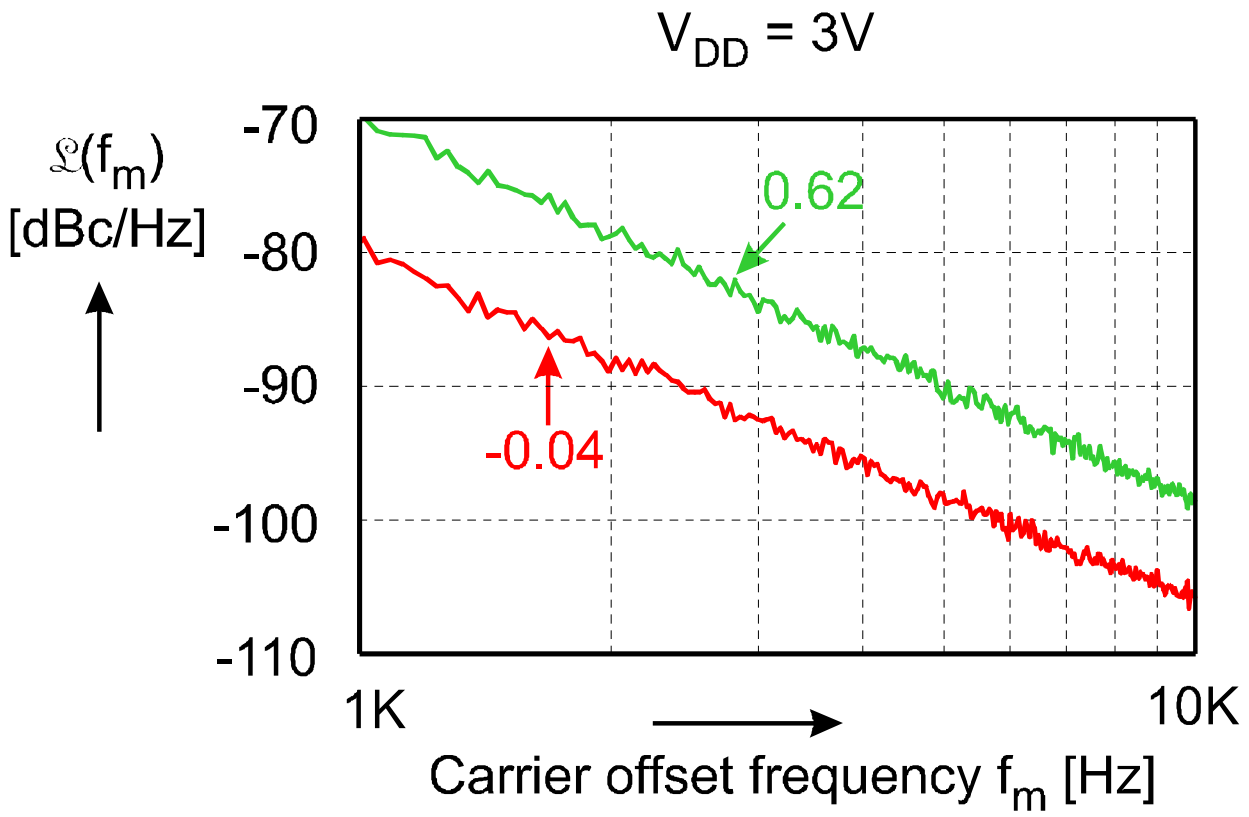


$R_n \uparrow \Rightarrow$ • $V_{GS\_OFF} \downarrow$ $\Rightarrow$ **1/f noise induced phase noise ↓ ?**

• f_{osc} hardly changes

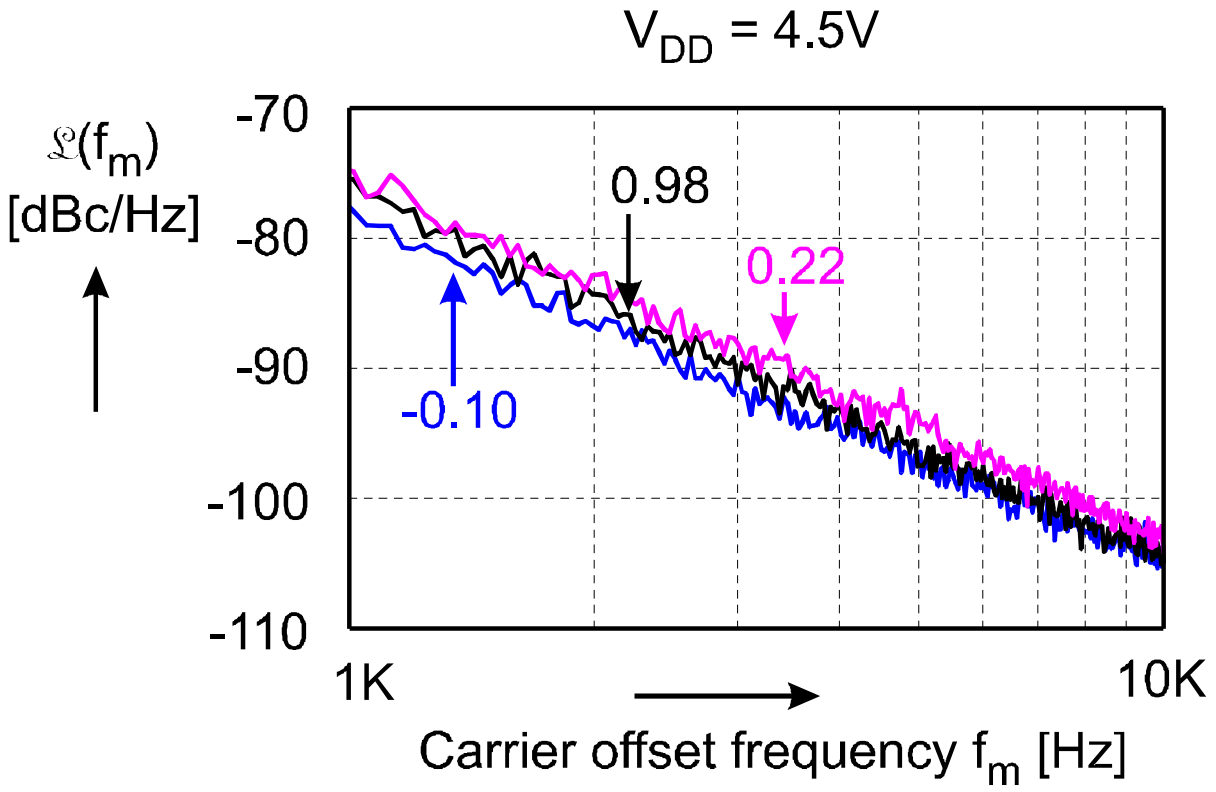
Phase noise measurement results (1)

F_{OSC} [MHz]	V_{MAX} [V]	V_{MIN} [V]
3.016	3.1	-0.04
3.274	2.8	0.62

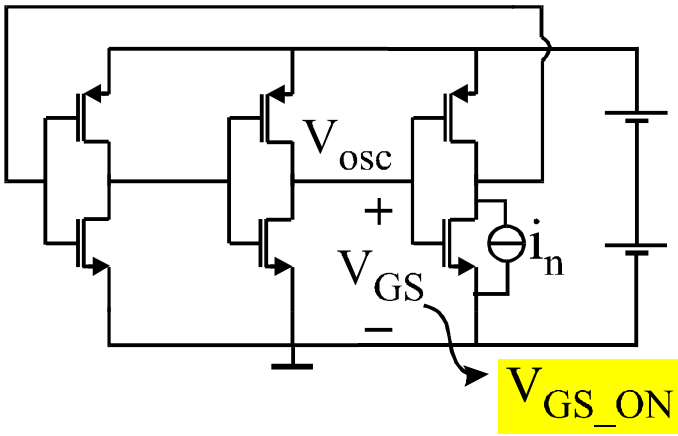


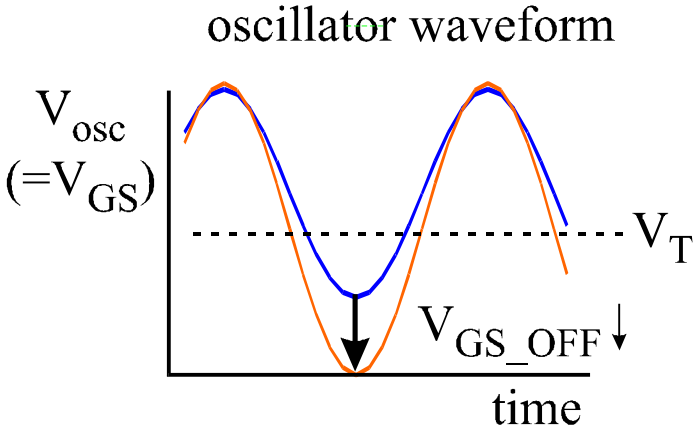
Phase noise measurement results (2)

F_{OSC} [MHz]	V_{MAX} [V]	V_{MIN} [V]
6.17	4.5	-0.10
7.03	4.2	0.22
7.94	3.9	0.98

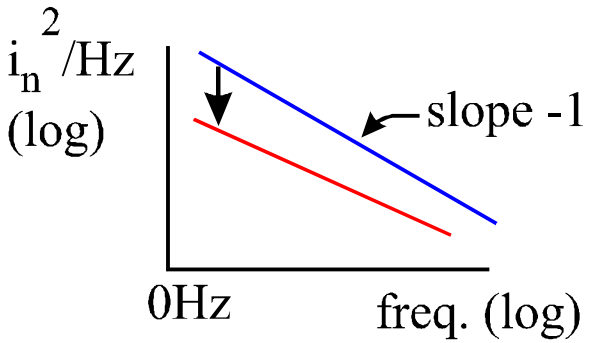


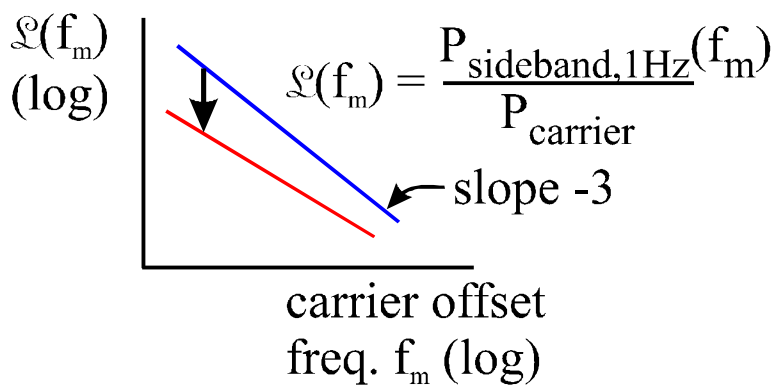
Corrections are needed



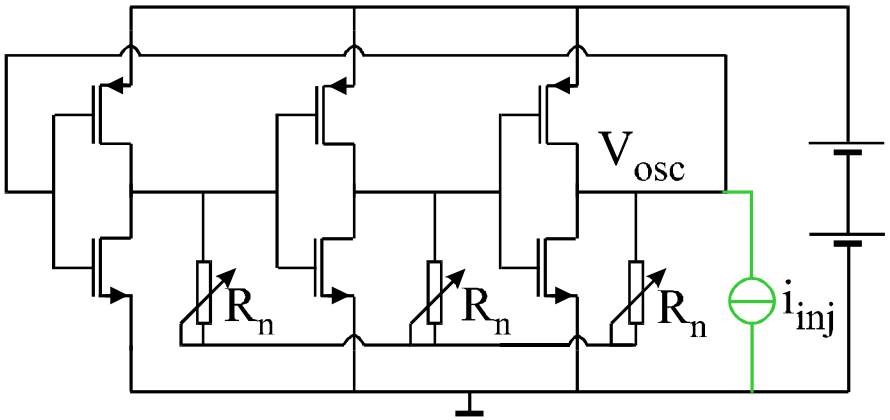


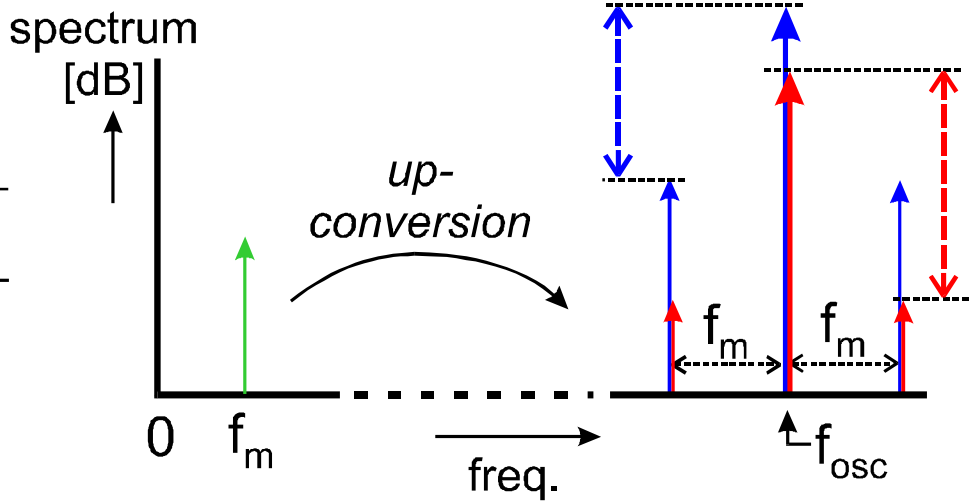
upconversion (freq. modulation)

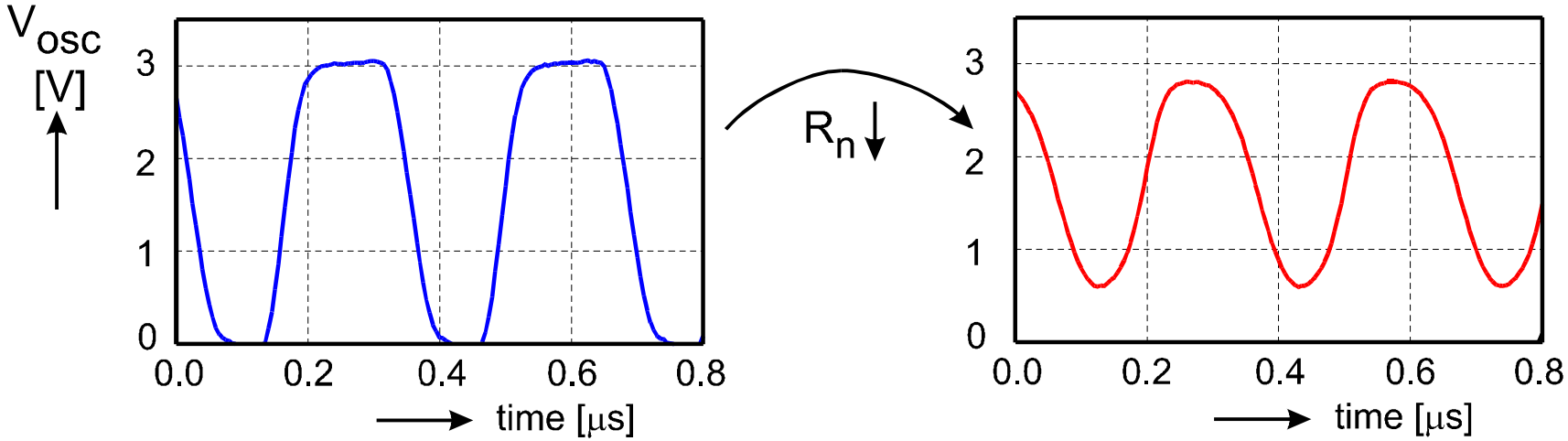




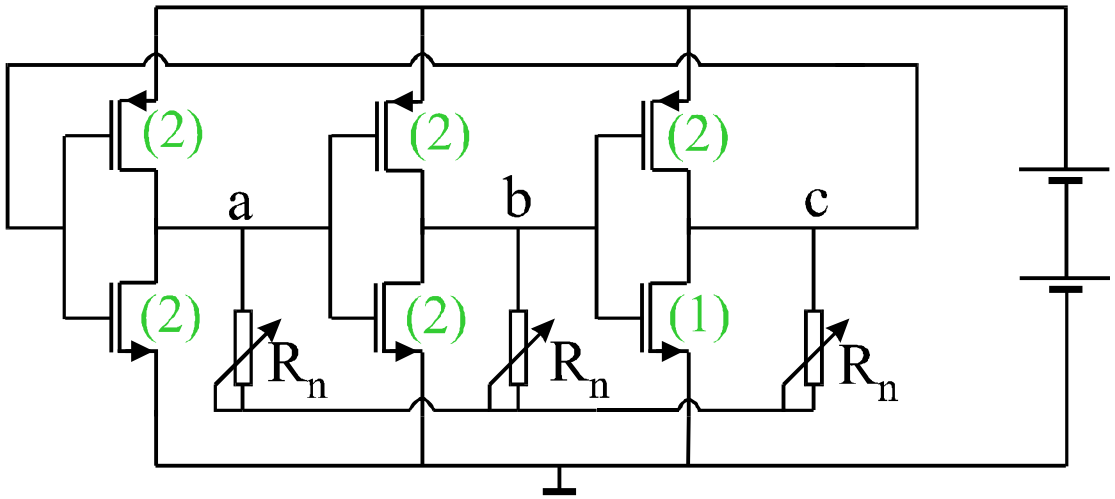
Correction for changes in upconversion





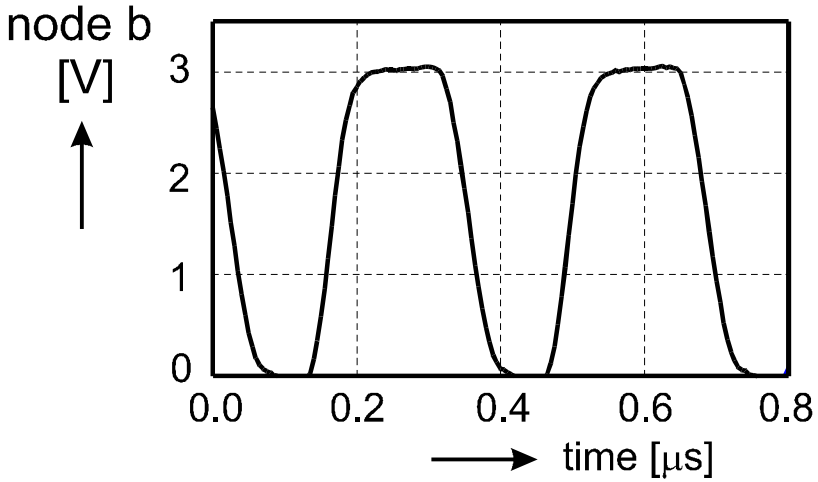


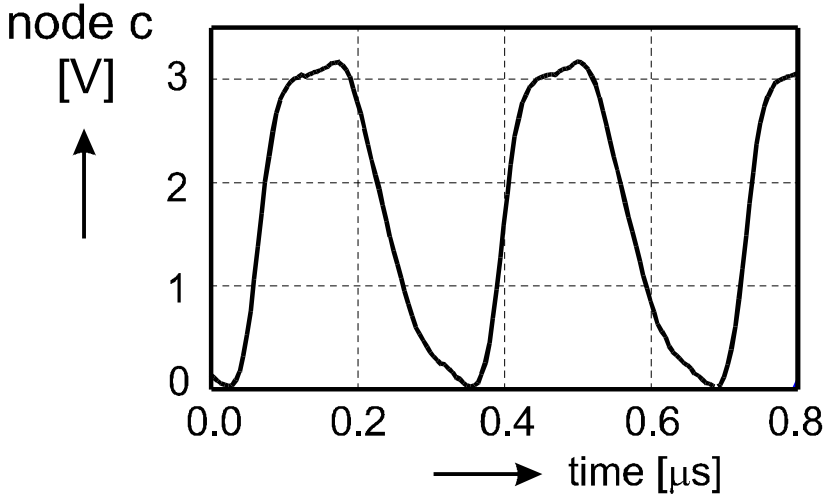
Measurement of upconversion (1)



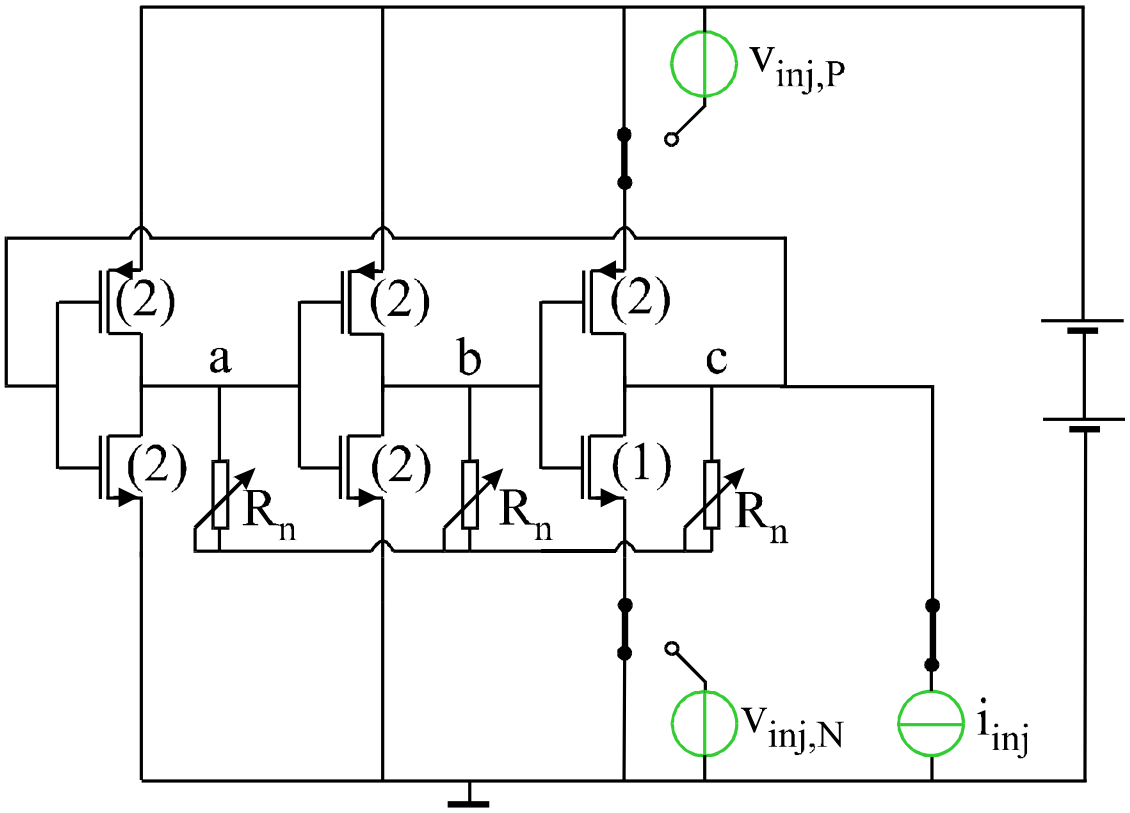
Due to asymmetry of waveform, node c will dominate upconversion

[Hajimiri JSSC feb. 1998]





Measurement of upconversion (2)



Example :

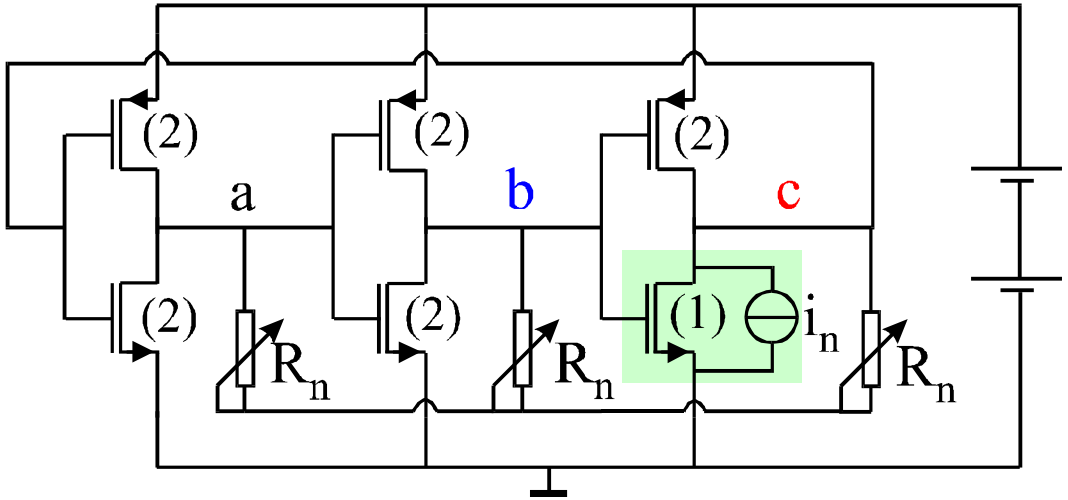
i_{inj} : 1µA @ 10 kHz

injection at node :	upconversion [dB]
a	- 52.96
b	- 69.63
c	- 39.67

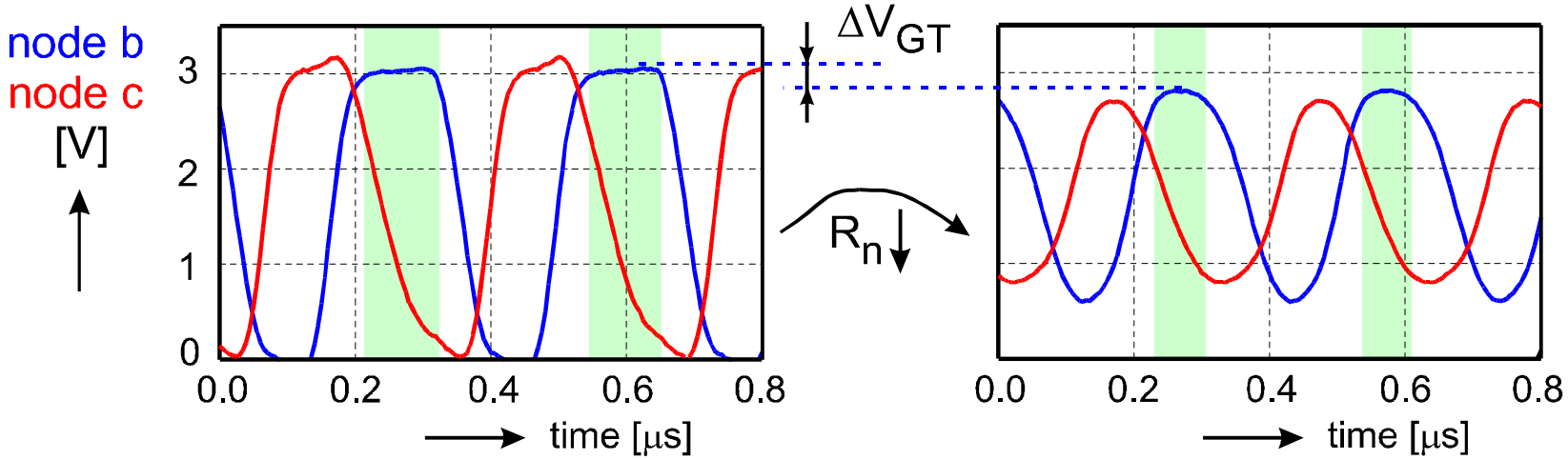
V_{inj} : 0.3mV @ 10 kHz

injection at source :	upconversion [dB]
NMOS	- 39.92
PMOS	- 49.13

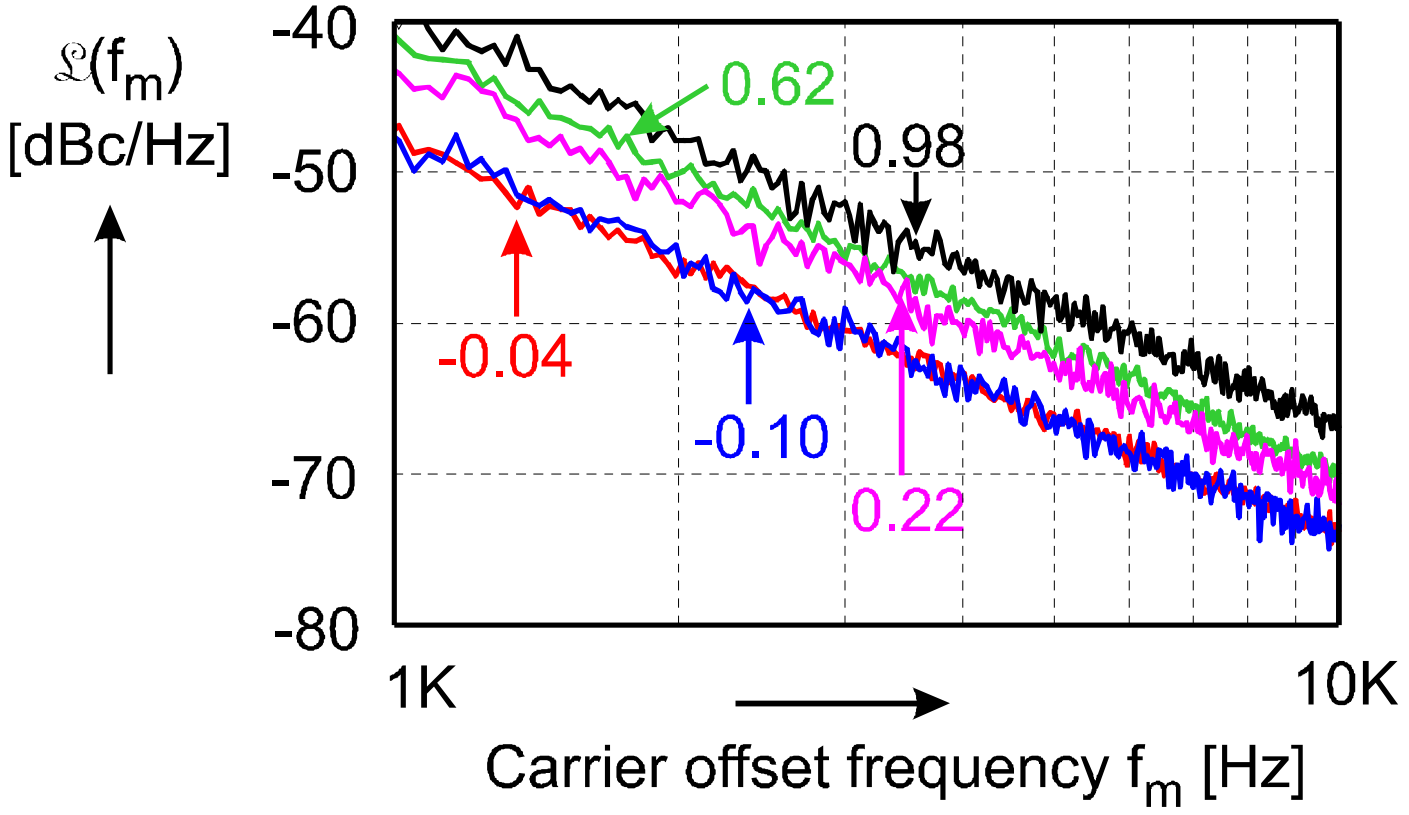
Correction for changes in V_{GS_ON}



$$\frac{i_n^2}{\Delta f} = \frac{K_{fl} \cdot g_m^2}{C_{ox} \cdot W \cdot L \cdot f} \sim (V_{GT})^2$$



Phase noise measurement results after correction



$V_{GS\_OFF} \downarrow \Rightarrow$ 1/f noise induced phase noise $\downarrow$

Conclusions

- phase noise measurements of a CMOS ring oscillator can be related to baseband 1/f device noise measurements :

$V_{GS\_OFF}\downarrow \Rightarrow$ 1/f device noise $\downarrow$

$\Rightarrow$ 1/f noise induced phase noise $\downarrow$ *(design criterium)*

- upconversion should be taken into account