[4] G. Nicollini and D. Senderowicz, "Internal fully-differential operational amplifier for CMOS integrated circuits," U.S. Patent N.918101, June 1987.
[5] G. Nicollini, F. Moretti, and M. Conti, "High-frequency fully differential filter using operational amplifiers without common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp. 803–813, June 1989.

MOS Current Gain Cells with Electronically Variable Gain and Constant Bandwidth

ERIC A. M. KLUMPERINK AND
EVERT SEEVINCK, SENIOR MEMBER, IEEE

***Abstract*—Two MOS current gain cells are proposed that provide linear amplification of currents supplied by several linear MOS $V-I$ converters. The gain is electronically variable by a voltage or a current and can be made insensitive to temperature and IC processing. The gain cells have a constant (gain-independent) bandwidth.**

I. Introduction

A basic problem of the use of negative feedback in amplifiers is the compromise to be made between bandwidth on the one hand and linearity of the transfer function on the other [1]. This trade-off is not necessary if amplifier circuits are available with a linear open-loop transfer characteristic.

The bipolar translinear current gain cell [2] has this property. In addition, it features a wide-band frequency response and electronically variable gain, as well as insensitivity to IC processing and temperature. This makes it a useful building block for applications requiring programmable high-frequency gain (e.g., gain control and signal multiplication).

In this paper, two MOS gain cells with similar features will be proposed, one with a voltage-controlled gain and the other with a current-controlled gain. In Section II it will be shown how linear current gain is obtained in these circuits, using the square-law MOS characteristic. Moreover, in Section III it will be argued that the MOS gain cells have a constant (gain-independent) bandwidth. This is due to the fact that the transconductance of a MOS transistor can be varied without affecting its gate–source capacitance, in contrast to the bipolar case. Section IV presents experimental results demonstrating the feasibility of the concept and Section V ends with the conclusions.

II. Principle of Operation

A. Input-Current Form

The MOS gain cells to be described require input currents of the form supplied by several known linear $V-I$ converters [3]–[5]. Although using different circuit structures, these $V-I$ converters provide output currents of the form

$$I_1 = k_v(V_{\text{bias}} + v_{\text{in}})^2 \tag{1a}$$

$$I_2 = k_v(V_{\text{bias}} - v_{\text{in}})^2 \tag{1b}$$

Manuscript received November 22, 1988; revised April 20, 1989.
E. A. M. Klumperink is with the Faculty of Electrical Engineering, IC Technology and Electronics Group, University of Twente, 7500 AE Enschede, The Netherlands.
E. Seevinck is with the Faculty of Electrical Engineering, IC Technology and Electronics Group, University of Twente, 7500 AE Enschede, The Netherlands, and Philips Research Laboratories, 5600 JA Eindhoven, The Netherlands.
IEEE Log Number 8930110.

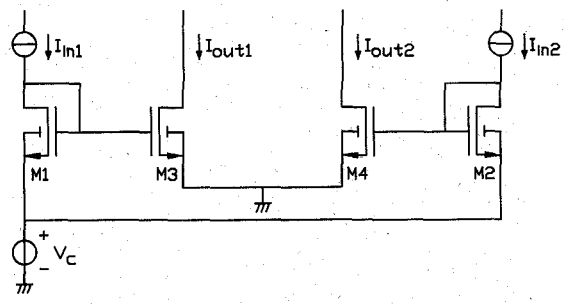

Fig. 1. Voltage-controlled gain cell.

where k_v is a transconductance parameter, V_{bias} is a bias voltage, and v_{in} is the input voltage signal of interest. The currents of (1a) and (1b) are used as input currents I_{in1} and I_{in2} for the MOS gain cells. The difference of these currents ΔI_{in} is linearly dependent on v_{in}:

$$\Delta I_{\text{in}} = I_{\text{in1}} - I_{\text{in2}} = 4k_v V_{\text{bias}} v_{\text{in}}. \tag{2}$$

Since ΔI_{in} is the signal to be amplified, (1a) and (1b) are first rewritten in terms of ΔI_{in} as

$$I_{\text{in1,2}} = I_{\text{in0}}\left[1 \pm \frac{\Delta I_{\text{in}}}{4I_{\text{in0}}}\right]^2 \tag{3}$$

where I_{in0} is the zero-signal value of the input currents. For the linear $V-I$ converters referred to before, it follows from (1a) and (1b) that I_{in0} is given by

$$I_{\text{in0}} = k_v V_{\text{bias}}^2. \tag{4}$$

The operation of the MOS gain cells will now be discussed assuming identical MOS transistors operating in strong inversion and saturation, characterized by

$$I_d = k_g(V_{gs} - V_{th})^2, \qquad \text{for } V_{gs} > V_{th}. \tag{5}$$

B. Voltage-Controlled Gain Cell

The circuit structure of the voltage-controlled gain cell is shown in Fig. 1. The input currents of (3) will develop gate–source voltages across input transistors $M1$ and $M2$ which can be expressed as (using (3) and (5))

$$V_{gs1,2} = V_{th} + \sqrt{I_{\text{in0}}/k_g} \pm \frac{\Delta I_{\text{in}}}{4\sqrt{k_g I_{\text{in0}}}}. \tag{6}$$

From (6), it can be seen that the difference of the gate–source voltages of $M1$ and $M2$ is directly proportional to ΔI_{in}. To achieve linear current gain, this voltage difference must be converted to a current difference in a linear fashion. This is done by two MOS transistors of which the sum of the gate–source voltages is kept constant [3]. From (6) it can be seen that this constant sum condition is already present at the input transistors. The linearity condition is satisfied for the output transistors $M3$ and $M4$ as well, since a constant voltage V_c is added to V_{gs1} and V_{gs2}. This is the key to the operation of the voltage-controlled gain cell. The resulting output currents take the form (using (5) and (6))

$$I_{\text{out1,2}} = k_g\left[V_c + \sqrt{I_{\text{in0}}/k_g} \pm \frac{\Delta I_{in}}{4\sqrt{k_g I_{\text{in0}}}}\right]^2. \tag{7}$$

0018-9200/89/1000-1465$01.00 ©1989 IEEE

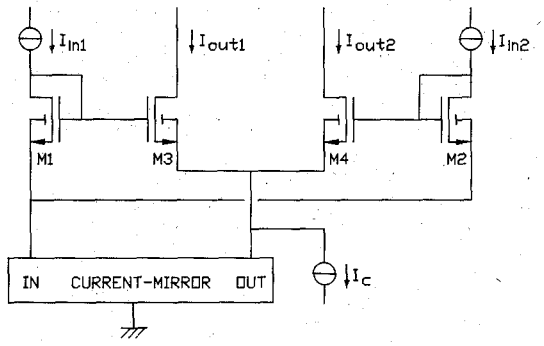

Fig. 2. Current-controlled gain cell.

Therefore the differential output current is given by

$$\Delta I_{\text{out}} = I_{\text{out1}} - I_{\text{out2}} = k_g \frac{V_c + \sqrt{I_{\text{in0}}/k_g}}{\sqrt{k_g I_{\text{in0}}}} \Delta I_{\text{in}} \tag{8}$$

and it follows that the current gain will be

$$A_i = \frac{\Delta I_{\text{out}}}{\Delta I_{\text{in}}} = 1 + \frac{V_c}{\sqrt{I_{\text{in0}}/k_g}}. \tag{9}$$

Linear differential current gain is thus achieved, controllable by voltage V_c. The equations derived so far are valid for large signals, as long as the condition $V_{gs} > V_{th}$ (or $I_d > 0$) is satisfied. Using (6), (7), and (9), the maximum input signal can be calculated as

$$|\Delta I_{\text{in}}|_{\max} = 4I_{\text{in0}}, \qquad \text{for } A_i \geq 1 \tag{10a}$$

$$|\Delta I_{\text{in}}|_{\max} = 4A_i I_{\text{in0}}, \qquad \text{for } A_i \leq 1. \tag{10b}$$

The gain A_i can be made insensitive to temperature and IC-processing variations by suitably generating I_{in0} (see also (4)):

$$I_{\text{in0}} = k_g V_0^2 \tag{11}$$

where V_0 is a dc voltage which depends on temperature and IC processing in the same way as V_c does.

C. Current-Controlled Gain Cell

The basic circuit structure of a current-controlled gain cell is shown in Fig. 2. It differs from the voltage-controlled version by the alternative way in which the linearity of the $V-I$ conversion in the output transistors $M3$ and $M4$ is achieved. Using (5), the transfer function of this differential pair can be expressed in the well-known form [3]

$$\Delta I_{\text{out}} = \sqrt{2k_g}\sqrt{(I_{\text{out1}} + I_{\text{out2}}) - \frac{1}{2}k_g(V_{gs1} - V_{gs2})^2} \cdot (V_{gs1} - V_{gs2}). \tag{12}$$

This $V-I$ conversion can be linearized [3] by making $I_{\text{out1}} + I_{\text{out2}}$ suitably dependent on $(V_{gs1} - V_{gs2})^2$. It follows from (3), (6), and (12) that the desired square-law component is in fact already available in the sum of the input currents:

$$I_{\text{in1}} + I_{\text{in2}} = 2I_{\text{in0}} + \frac{1}{2}k_g(V_{gs1} - V_{gs2})^2. \tag{13}$$

Using a current mirror, this current is added to a control current I_c to form the tail current for $M3$ and $M4$:

$$I_{\text{out1}} + I_{\text{out2}} = I_c + 2I_{\text{in0}} + \frac{1}{2}k_g(V_{gs1} - V_{gs2})^2. \tag{14}$$

Using first (12) and (14) and then (6), this results in a current gain given by

$$A_i = \frac{\Delta I_{\text{out}}}{\Delta I_{\text{in}}} = \sqrt{1 + \frac{I_c}{2I_{\text{in0}}}}. \tag{15}$$

Thus a second linear current gain cell is revealed, having a gain controllable by current I_c. It can be simply shown that the input-current restrictions of (10) also hold for this gain cell. The gain again can be rendered insensitive to temperature and IC technology by making I_c and I_{in0} depend on temperature and IC processing in the same way.

D. Comparison of the Gain Cells

The gain cells described above obtain the same transfer function by different means. Since the individual transistors operate under the same conditions, the circuits have the same linearity properties. In both gain cells the maximum achievable gain is limited by voltage restrictions, necessary to keep all transistors in strong inversion and saturation. The voltage drop across the current-mirror input in the current-controlled gain cell poses an extra voltage restriction. The voltage-controlled gain cell does not have this disadvantage, but it needs a low-impedance V_c source, since the input currents flow through it.

III. Bandwidth Properties

To get an impression of the HF properties of the gain-cell circuits, the small-signal behavior was examined assuming differential current drive at the input. Since small-signal properties are examined, in contrast to (3), the signal parts of I_{in1} and I_{in2} are equal, but have opposite sign, so no ac current will flow into source V_c nor in the current-mirror input. Therefore in both gain-cell circuits the common-source node of transistors $M1$ and $M2$ as well as that of $M3$ and $M4$ can be regarded as ac ground. When $A_i = 1$ (so V_c and I_c are zero), the circuits act as a pair of simple current mirrors, with a bandwidth determined mainly by the transconductance of the input transistors and the capacitance present at the input nodes. By means of V_c or I_c, A_i can be increased without changing this bandwidth, since the transconductance of the input transistors and the input node capacitances remain the same. Thus, in contrast to bipolar gain cells which have a constant GB product when the gain is varied, the MOS gain cells have a constant bandwidth. As a consequence, the MOS gain cells have an A_i-times higher GB product than a pair of simple current mirrors constructed with the same transistors.

IV. Experimental Results

The linearity and bandwidth properties of the circuits of Figs. 1 and 2 were measured on a breadboard realization using CA3600E transistor arrays, having $k_g = 320\ \mu\text{A/V}^2$. Since there were no significant differences, for the sake of brevity only the results of the voltage-controlled gain cell will be given here. The input drive currents of the form of (1) and (3) were supplied by a pair of PMOS transistors. The sources of this pair were connected to a dc bias voltage of 11.95 V. The gates were driven by voltages $+v_{\text{in}}$ and $-v_{\text{in}}$ around 10 V, provided by a signal

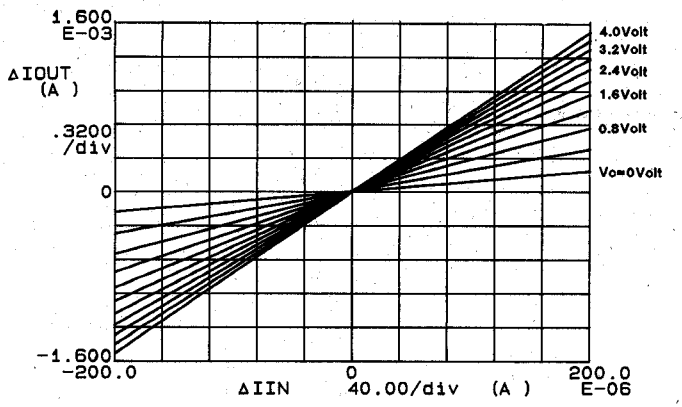

Fig. 3. Transfer function of the voltage-controlled gain cell with input currents according to (3).

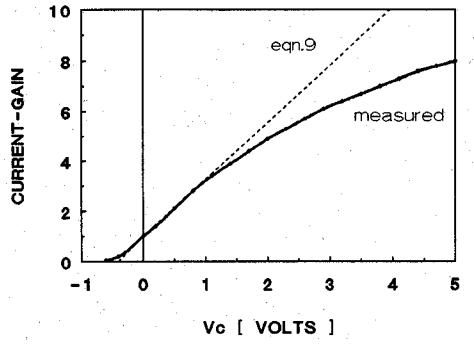

Fig. 4. Relation between the current gain and V_c of the voltage-controlled gain cell.

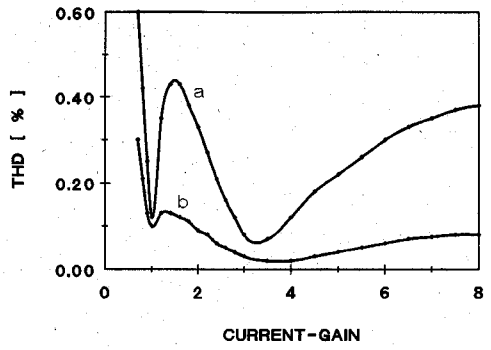

Fig. 5. THD measured at the output of the voltage-controlled gain cell for an ΔI_{in} amplitude of (a) 190 μA and (b) 100 μA.

generator with balanced output. V_c was supplied by a variable power supply. For these biasing conditions $I_{in0} = 50$ μA and $\sqrt{(I_{in0}/k_g)} = 0.4$ V. The output currents of the gain cell were measured by means of 100-Ω load resistors.

The relation between ΔI_{in} and ΔI_{out} for different V_c values is plotted in Fig. 3 and the relation between the current gain and V_c is shown in Fig. 4. The figures demonstrate the linearity and variability of the gain. However, due to the mobility reduction effect, the gain is less than predicted by (9), especially for large V_c values.

Fig. 5 shows the THD of the gain cell for sinusoidal ΔI_{in} having a frequency of 1 kHz and an amplitude of 190 and 100 μA (95 and 50 percent of its maximum value (10)). The THD value was below 0.5 percent. It is determined mainly by third harmonics, due to mobility reduction. To get an impression of the relative merits of the circuit, a MOS implementation of the bipolar gain cell [2] was also realized on breadboard. The THD was measured for input currents of the form of (3) as well as for linear currents of the form

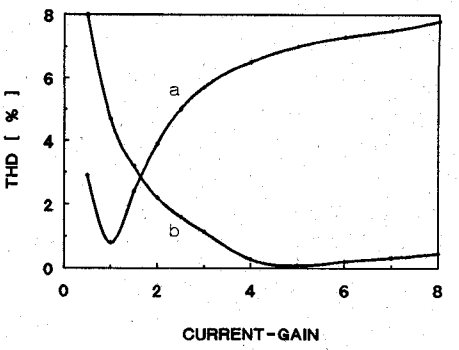

Fig. 6. THD measured at the output of a MOS implementation of a bipolar gain cell with input currents according to (a) (16) and (b) (3) (see text).

$$I_{in_{1,2}} = I_{in0} \pm 1/2\,\Delta I_{in}. \tag{16}$$

Fig. 6 gives the results, again for an ΔI_{in} amplitude of 95 percent of its theoretical maximum. The THD values are substantially larger than for the MOS gain cells proposed in this paper.

To verify the prediction of constant bandwidth, the −3-dB bandwidth of the gain cells was measured, again for $I_{in0} = 50$ μA. It appeared to be 1.1 MHz, indeed independent of A_i for A_i ranging from 1 to 8.

V. Conclusions

Two new MOS gain cells have been proposed in this paper which provide electronically variable linear current gain at a constant bandwidth. The gain cells have an A_i times larger gain–bandwidth product than a current mirror constructed with the same transistors.

Acknowledgment

The authors wish to thank M. G. van Leeuwen, B. Nauta, H. de Vries, and R. F. Wassenaar for their suggestions during discussions. Moreover, they wish to thank the reviewers for their useful comments.

References

[1] R. A. Blauschild, "An open loop programmable amplifier with extended frequency range," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 626–633, Dec. 1981.

[2] B. Gilbert, "A new wide-band amplifier technique," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 353–365, Dec. 1968.

[3] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 891–894, Oct. 1984.

[4] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 357–365, June 1987.

[5] E. Seevinck and R. F. Wassenaar, "A versatile CMOS linear transconductor/square-law function circuit," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 366–377, June 1987.