Reduction of 1/f Noise in MOSFETs by Switched Bias Techniques

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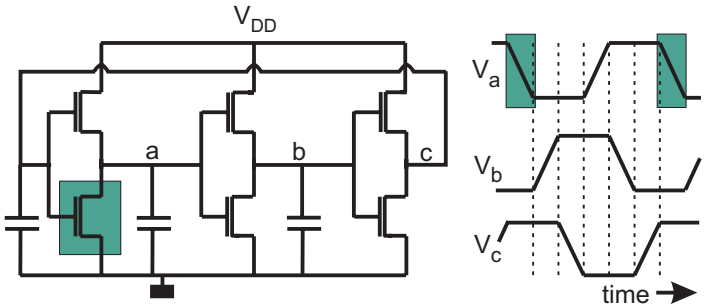
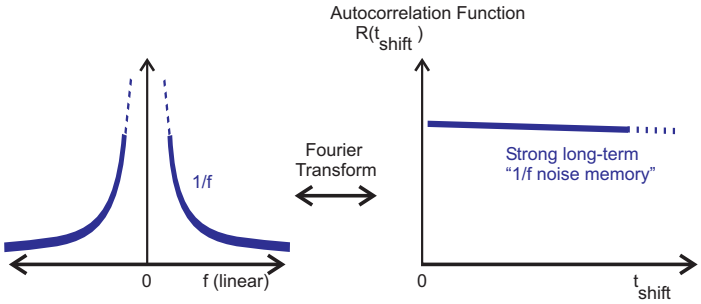
Background

- Timing Jitter Analysis CMOS Ring Oscillator
- Cyclic jitter contribution of individual MOSTs

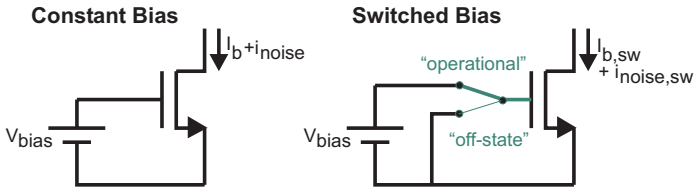


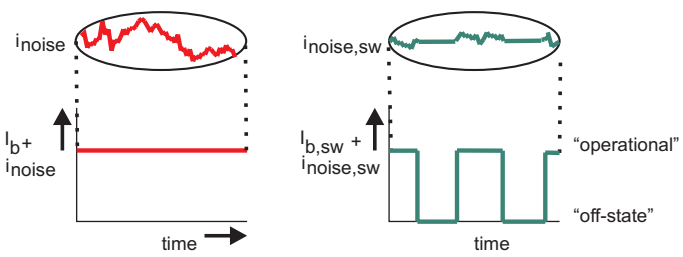
- Strong impact 1/f noise expected (correlation!)



1/f Noise Reduction Hypothesis

- Measurements: low 1/f Noise contribution!!
- Question: could switching affect 1/f noise??
  => Do Switched Bias Experiment

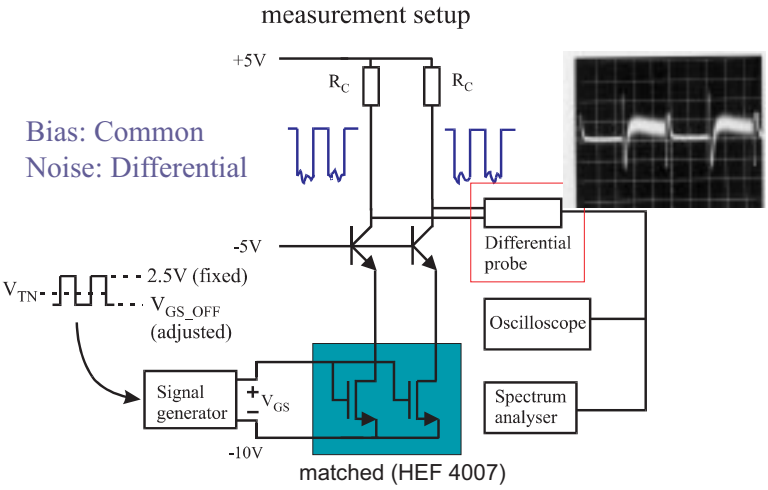




- Problem: $i_{noise,sw} << I_{b,sw}$ (160dB!)

Switched Bias Measurement Setup

- Use matched devices and differential probe
- 60-80dB Common Mode Rejection Ratio!



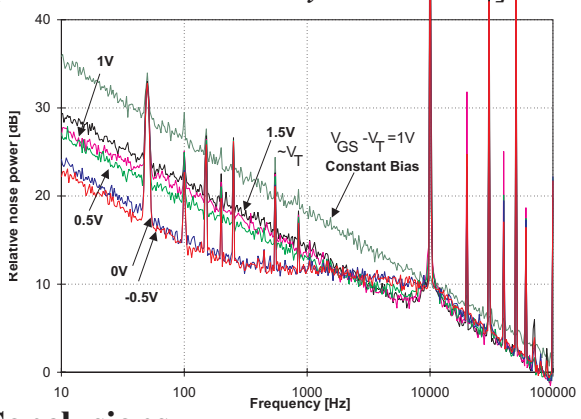
Measurement Results

- -6dB expected due to dutycycle 50%

➔ 6-8dB anamolous noise reduction!!!

- Observed in weaker form before at 100Hz

[Bloom & Nemerovsky, APL, 1991]



Conclusions

- Switched Biasing reduces ***intrinsic*** 1/f Noise
- Significant Effect (6-8dB)
- Useful in circuits and device characterisation

Future Work (STW TEL.4756, 2 PhD cand.)

- Device Characterisation and Modelling
- Exploit effect in circuit design