Reduction of 1/f Noise in MOSFETs by Switched Bias Techniques

Bram Nauta, Eric Klumperink, Sander Gierkink and Arnoud vd Wel

MESA+ Research Institute, University of Twente,
P.O. Box 217, Enschede, The Netherlands. Phone +31-53-489 2655,
email: b.nauta@el.utwente.nl, http://icd.el.utwente.nl

Abstract: Switched Biasing is a new a technique for reducing the 1/f noise in MOSFETS. Conventional techniques, such as chopping or correlated double sampling, reduce the *effect* of 1/f noise in electronic circuits, whereas the Switched Biasing technique reduces the 1/f noise *itself*. It exploits an intriguing physical effect: cycling a MOS transistor from strong inversion to accumulation reduces its 1/f noise. In fact the transistor "forgets" its past and thus these low-frequency noise components. This effect is important, especially in RF circuits where 1/f noise is often being upconverted, and is thus a serious problem. The history of the (re)discovery of the effect and the main experimental results obtained so far will be reviewed.

I. Introduction

CMOS ICs nowadays may contain up to several millions of transistors, mainly used in digital circuits, but also in analog and mixed analog-digital interface circuits (e.g. ADC, DAC, pre- and postamplifiers, up- and downconverters between baseband and RF). As charge transport in electronic devices is fundamentally accompanied by noise, the behaviour of all MOS transistors is subject to these random variations. These random variations ultimately limit the signal processing capability of transistor circuits, as they put a lower limit to the signal that can be processed reliably. Thus noise for instance limits the Signal-to-Noise ratio of analog circuits, resulting in noisy music or noisy TV pictures. In digital transmission systems noise introduces bit errors.

As noise results from device physics, designers generally consider it as something you cannot change and have to live with. In this paper it will be shown that this is *not necessarily true for 1/f noise*: it will be shown that it *is* possible to interact with the physical noise generating processes in a MOS transistor in such a way that the *1/f noise is reduced*. We discovered this in a research project aiming at low timing jitter in a CMOS ring oscillator for TV applications. This paper reviews the history of the project and the main results obtained so far.

II. Timing Jitter in CMOS Ring Oscillators

Figure 1 shows the clock signal generated by a ring oscillator generating the pixel clock for a Picture-in-Picture (PIP) window on a 100Hz TV screen. The time of zero-crossing determines the horizontal positioning of a pixel in the PIP window. Noise of MOS transistors in the oscillator introduces timing uncertainty in the zero-crossings and hence pixel misalignment. In a ring oscillator, subsequent zero-crossings are generated by subsequent oscillator stages. As every stage introduces its own zero-crossing timing uncertainty, while the transition of one stage starts the transition of the next stage, the total standard deviation in the time of zero crossing (total timing jitter or accumulated jitter σ_T)

increases with the number of periods N that has elapsed since the start of a PIP window (see Figure 1).

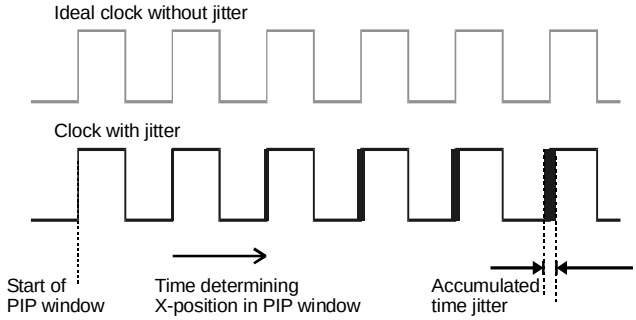

Figure 1: Pixel clock for a Picture-in-Picture (PIP) window on a TV screen determining the horizontal position of pixels. Every clock period adds its own time uncertainty, leading to time jitter accumulation.

The growth of the accumulated jitter strongly depends on the nature of the noise, and especially on its autocorrelation function. Of course, the autocorrelation function for time-shift equal to zero is important, as this renders the variance or rms-value of the noise. For time-shifts other than zero, this autocorrelation function indicates how much correlation exists between a noise signal and a time-shifted version of the same noise signal. If no correlation exists, the total accumulated jitter variance is equal to the sum of the variances. Hence, σ_T increases proportional to $\sqrt{N}$, see Figure 2).

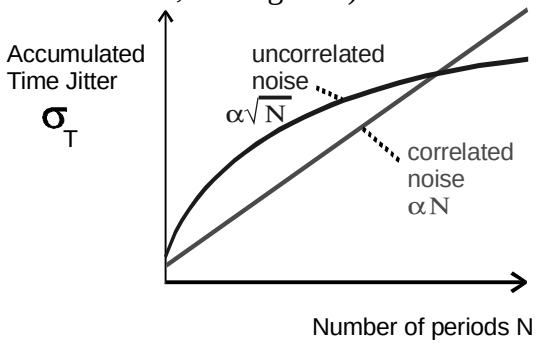

Figure 2: The accumulated time jitter increases with √N for uncorrelated noise contributions and linearly with N for correlated jitter contributions.

However, if timing errors are fully correlated (slow decay of the autocorrelation function with time-shift), the accumulated timing jitter σ_T increases linearly with the number of zero-crossings (see Figure 2). Hence, depending on the number of observed periods, either correlated or uncorrelated noise contributions may dominate the accumulated time jitter.

III. AUTOCORRELATION FUNCTION OF NOISE

As the autocorrelation function of noise plays a crucial role with respect to jitter accumulation, we will examine this function more closely. Noise is commonly characterised using spectrum analyser measurements. For this purpose the average noise power produced by a MOS transistor in a fixed small bandwidth around a certain frequency, e.g. in 1 Hz bandwidth, is measured. If we repeat this measurements for a range of frequencies, we find the so-called power spectral density of noise as a function of frequency, denoted as $S_n(f)$. Figure 3 shows $S_n(f)$ of the noise current of a typical MOS transistor. It typically has a flat part at high frequencies due to white noise, related to the thermal energy kT.

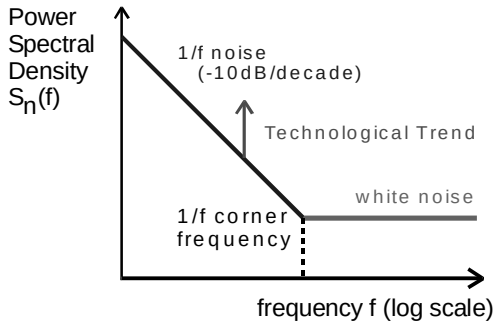

Figure 3: Measured power spectral density $S_n(f)$ of the noise of a MOS transistor, measured as the noise power in 1Hz bandwidth around frequency f.

Apart from this white noise, MOS transistors are notorious for exhibiting strong so-called 1/f noise or flicker noise below a so-called 1/f corner frequency (with a noise power spectral density inversely proportional to frequency, i.e. 10 dB/decade decay with frequency). This corner frequency lies in the lower MHz region for typical submicron MOS transistors, and tends to increase for newer processes (roughly proportional to f_T of the MOS transistor).

As is well-known from signal theory, the inverse Fourier transform of the power spectral density of a signal is the autocorrelation function (Wiener-Khinchin relations) [1]. Hence we can derive the autocorrelation function for noise from noise power spectral density measurements.

For white noise of infinite bandwidth the inverse Fourier transform is a delta-function. All timeshifts other than zero lead to zero autocorrelation. For bandlimited noise, a sinc-function is found, with significant correlation for time-shifts that are small compared to 1/Bandwidth.

For 1/f noise, matters are much more complicated, as 1/f noise signals are not stationary. Hence the power spectral density and autocorrelation function are time-dependent (this also solves the problem of infinite variance found by straightforward integration of S(f) for 1/f noise over all time, which is equivalent to neglecting the time-dependence of S(f) and hence assumes stationarity). It can however be shown [1] that 1/f noise can be approximated as stationary, for measurement times T_m that are much smaller than the time that has elapsed since the start of the 1/f process. Under this assumption, the approximated autocorrelation function shown in Figure 4 is found. Now a very strong correlation is found over a wide range of time-shifts [1]. This means that there is a strong correlation between subsequently measured samples of a 1/f noise signal over a long time. Put in another way: *the history of the 1/f noise signal to a large extent determines the value of the next sample to be found.*

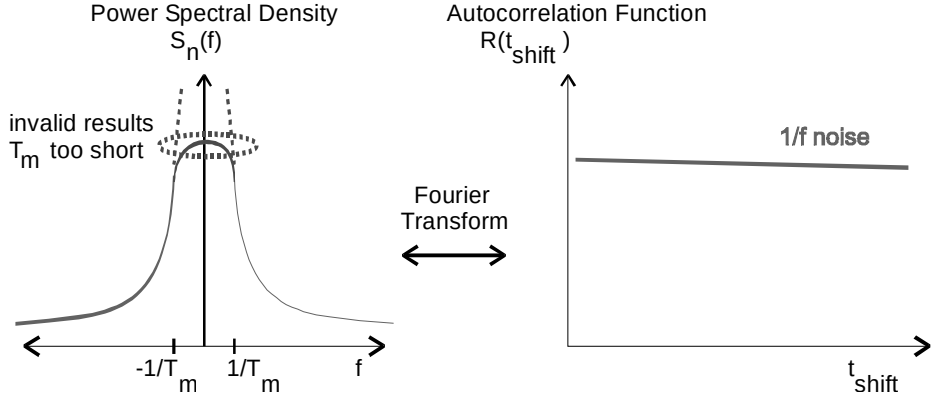

Figure 4: The autocorrelation function of a signal can be derived from the noise power spectral density by a Fourier transform. Assuming measurement time T_m to be small compared to time elapsed since the 1/f process started and $t_{shift}<T_m$, 1/f noise can be considered as stationary [1]. Strong correlation is found over a large range of timeshifts t_{shift}.

IV. THE 1/F NOISE REDUCTION HYPOTHESIS

Returning to the ring oscillator jitter problem stated in section II, we can now predict the accumulated timing jitter due to band-limited white noise and 1/f noise. Due to the strong correlation over a wide range of time-scales, the jitter accumulation due to 1/f noise is expected to dominate for long accumulation times (see Figure 2). However, jitter measurements failed to comply with this prediction: we found less jitter than expected. Moreover, phase noise oscillator measurements indicated dominant thermal noise at offset frequencies where we expected 1/f noise to dominate.

Because of the discrepancy between measurement and theory (and because young self-confident students prefer to question everything except for their analysis results), alternative explanations were sought. *As MOS transistors are switched off and on in a ring oscillator, the question was raised whether the switching might affect the noise*. Bearing in mind that 1/f noise is related to memory effects, one may intuitively suspect that it is possible to interfere with this memory (off-switching might "reset" the noise processes in some way, e.g. by forcing interface states to release captured electrons). We decided to investigate this possibility further by doing 1/f noise measurements under switched conditions.

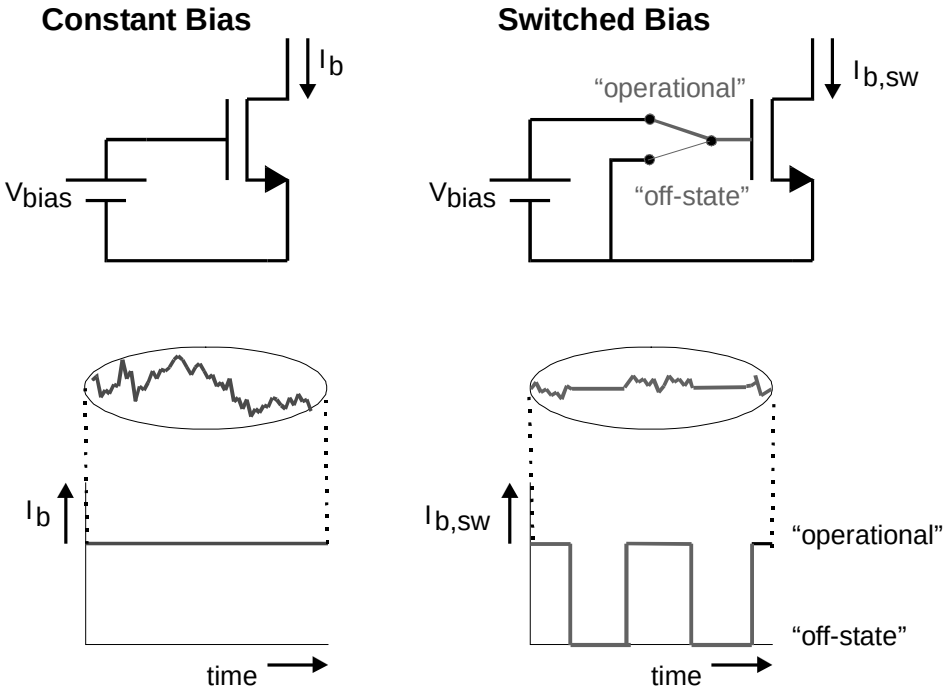

Figure 5: Principle of the Switched Bias Technique.

To be more exact, the main question is whether there will be 1/f noise reduction due to a technique that we will call *Switched Biasing*. Figure 5 illustrates the principle of the technique and compares it to constant biasing. Instead of applying a constant gate-source bias voltage, a MOS transistor is periodically switched between two states:

1. an "operational state" in strong inversion, in which it supplies a constant bias current I_b (required for circuit functionality).
2. a "rest-state" below threshold, for practical purposes 0 Volt. In this state the MOS transistor is not operational. By biasing the transistor periodically in this state, it is hoped to "forget" about its past 1/f noise behaviour resulting in less 1/f noise in the operational state (see Figure 5).

We will now try to measure the 1/f noise under switched bias conditions, to verify the hypothesis.

V. SWITCHED BIAS 1/F NOISE MEASUREMENTS

Having decided to measure the noise under switched bias conditions, the question is how to do this measurement. As a small noise signal is to be measured in the presence of a strong switching signal, the dynamic range requirements for the measurement are rather severe. To illustrate this point, consider the following example.

A MOS transistor capable of conducting a drain current in strong inversion of 1mA at an effective gate-source voltage of 1 Volt, has a transconductance in the order of 2mS. Furthermore, assume that we want to measure both the 1/f noise and thermal noise of this MOS. The thermal (drain) noise current power spectral density of this transistor, measured in 1Hz bandwidth, is in the order of 6pA/sqrt(Hz). In terms of measured power, this measured noise is more than 16 orders of magnitude (160dB) lower than the switched bias current of 1mA. As typical spectrum analysers offer 80-100 dB of dynamic range, special measures are needed to suppress the switching signal. We found a solution to this problem using two equal MOS devices and exploiting the large common mode rejection of a differential probe. Figure 6 shows the measurement setup.

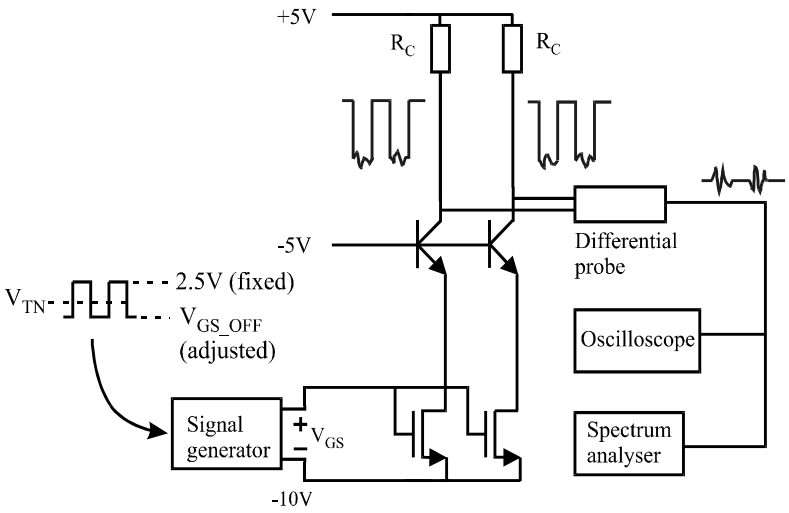

Figure 6: Measurement setup for switched bias 1/f noise measurements. The differential probe suppresses the common switched bias signal sufficiently to not overload the spectrum analyser.

Two NMOS transistors are driven by a common gate-source voltage supplied by the signal generator. Auxiliary bipolar cascoding devices and collector impedances convert the drain-current of the MOS transistors to voltages. It was verified that the setup is such that the noise of these voltages is dominated by the drain noise current of the MOS transistors. This noise is measured by the differential probe. The high common-mode rejection of the probe (>80dB for 10Hz to 50KHz) avoids overload of the spectrum analyser by the large, but common switched-bias signal.

For 50% duty cycle, the probe alternatively measures MOS device noise (“on-state”) and almost no noise (“off-state”) (see the measured voltage waveform in Figure 7).

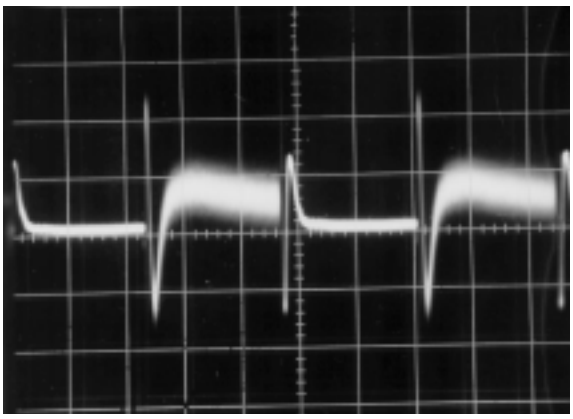

Figure 7: Output signal of the differential probe in Figure 6, showing alternative periods with almost no noise (MOS transistors off) and considerable noise (MOS transistors on).

Figure 8 shows the measured noise spectra for NMOS devices in commercially available HEF4007 MOS ICs. The upper curve shows the noise spectrum measured with the devices constantly biased at a gate-source voltage of 2.5 Volt ($V_{Threshold}$ = 1.5V), and the lower curve shows the noise spectrum of the devices switched periodically between 2.5V and 0V with a 10KHz, 50% duty cycle square wave signal (spectral peaks are due to 50Hz interference and switching residuals).

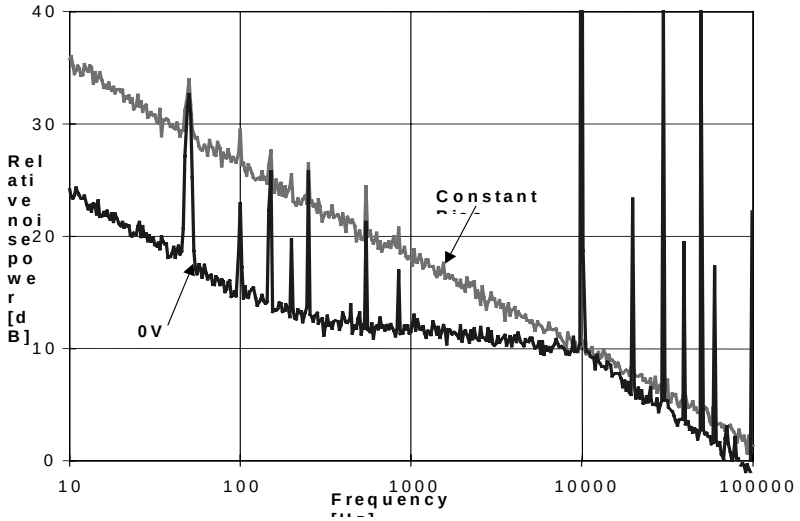

Figure 8: Measured power spectral density of noise as a function of frequency for constant gate-source bias and switched bias condition (HEF 4007 NMOS, f_{switch}=10KHz, 50% duty cycle, $V_{GS,on}$=2.5V, $V_{GS,off}$=0V).

Modelling the switching operation as a simple modulation action, 6dB noise reduction is expected for 1/f noise. However, the measurements show an *additional anomalous* reduction in 1/f noise power spectral density of about 8dB at low frequencies!! *This confirms the hypothesis on reduction of 1/f noise due to switching!*

Further measurements were done to characterize the dependence of the noise reduction to the off-voltage. Figure 9 shows the results for off-voltages of 1.5V, 1V, 0.5V, 0V and -0.5V. The conclusion that can be drawn from this figure is that the *noise reduction increases for decreasing off-voltage*.

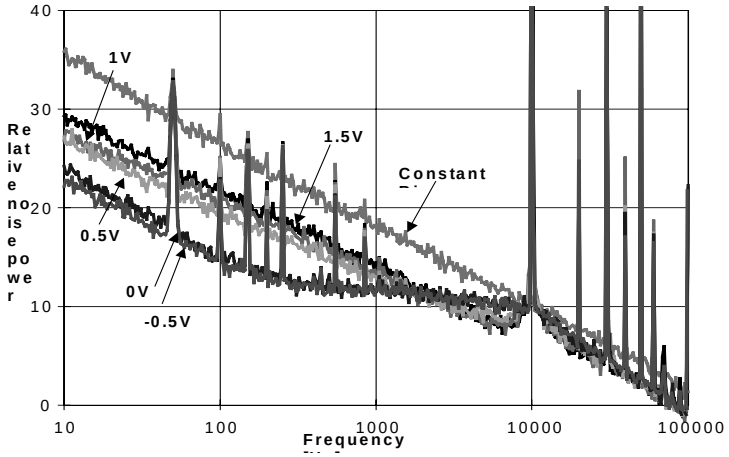

Figure 9: Measured power spectral density of noise as a function of frequency for constant gate-source bias and switched bias conditions with different off-voltages (HEF 4007 NMOS, f_{switch}=10KHz, 50% duty cycle, $V_{GS,on}$=2.5V, $V_{GS,off}$=1.5V, 1V, 0.5V, 0V,-0.5V).

VI. EXPLORING THE IMPACT OF 1/F NOISE REDUCTION IN CMOS RING OSCILLATOR

About half a year after we discovered the 1/f noise reduction, we found out that the 1/f noise reduction has been observed before in a weaker form, in 1991, by the physicists Bloom and Nemirovsky [2], using an alternative measurement setup. They showed that the noise reduction is maximised if the MOS transistor is cycled from strong inversion via weak inversion to accumulation. Shortly after, their results were reconfirmed [3] and related to Random Telegraph Signals. However, until recently this 1/f noise reduction mechanism received no attention in the solid-state circuits community (no references to [2, 3] according to the Science Citation Index from '91-'97). We seem to be the first to explore the impact of the effect on electronic circuits. We will now briefly discuss the results obtained so far, referring to publications presented elsewhere.

First of all we build and improved the measurement setup described in the previous section, and checked and double-checked the switched bias noise measurements [4,5]. Compared to the sampling measurement setup presented in [2], our main advantage is that noise reduction measurement can be done in a much wider frequency band (1Hz .. 1MHz region, instead of 1..100Hz). By using commercially available HEF 4007 device, we were able to do switched bias noise reduction measurements on ICs from 5 different manufacturers. In all cases we found significant anomalous noise reduction, ranging from 6 to 8 dB (4-8 times less noise power).

Furthermore, we tried to relate the switched bias baseband measurements to oscillator phase noise measurement. The 3-stage ring oscillator shown in Figure 10 was used, with additional resistors allowing for control of the amplitude of oscillation, and hence the off-voltage of the MOS transistors (see Figure 11). Based on the theory of 1/f noise induced phase noise available at that time [6], we predicted phase noise and were able to show correlation between the baseband noise reduction and phase noise reduction [7].

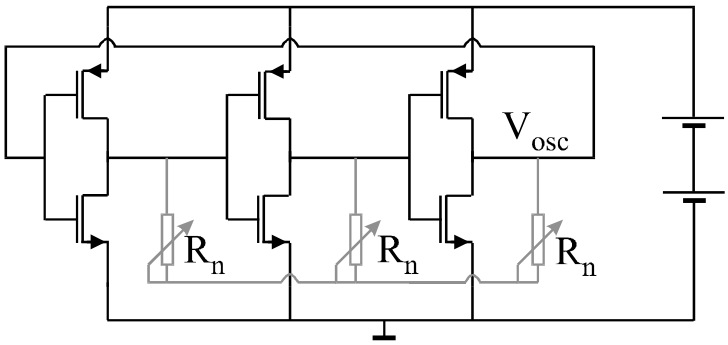

Figure 10: Measurement setup for analysing the effect of oscillation amplitude on 1/f noise induced phase noise. Decreasing the value of the resistors R_n reduces the gain of the inverters and results in lower oscillation amplitude as shown in Figure 11.

Due to the valueable contribution of Hajimiri on 1/f noise upconversion in ring oscillators [8], we examined variations in upconversion due to changes in the changes in symmetry of oscillator signal waveforms. It appeared that we were lucky in our first experiments, in finding strong correlation between phase noise measurements and baseband measurements. In general, also the variation in upconversion must be taken into account, and also the variation in the on-voltage of the MOS transistors [9,10]. After these correction, the phase noise measurement correspond to the baseband measurement, as shown in Figure 12.

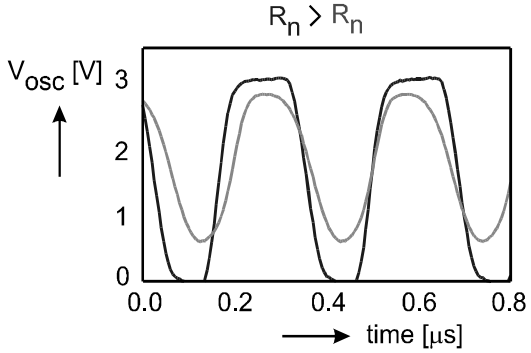

Figure 11: Measured waveform Vosc of the oscillator of Figure 10 for two values of Rn. Lowering Rn results in lower oscillation amplitude.

Summarizing so far, we have shown that 1/f noise due to switched biasing can give a considerable noise reduction in the order of 8dB, and that it play a significant role in the 1/f noise induced phase noise of CMOS ring oscillators..

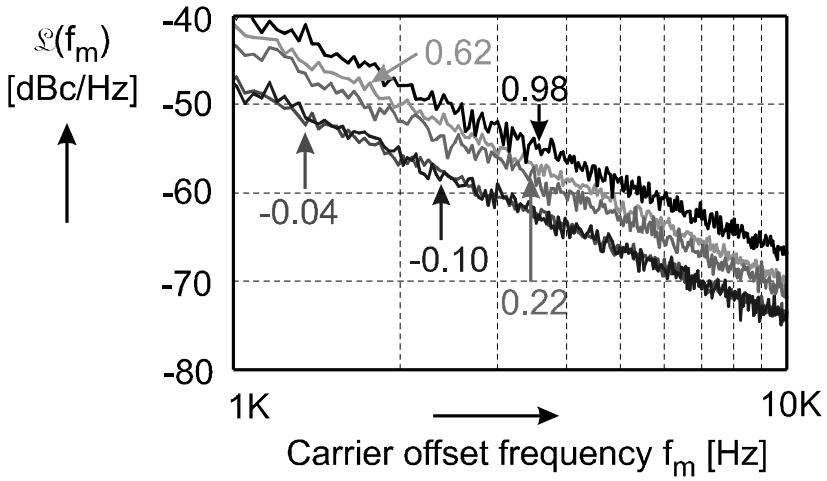

Figure 12: Measured phase noise of the oscillator shown in Figure 11 for different values of the off-voltage of the MOS transistors.

After evaluating the noise-reduction effect at baseband, and proving the behaviour in a 3-stage inverter ring oscillator, it was time to exploit the effect in a circuit. To enable a quick verification of the idea, an integrated CMOS sawtooth oscillator which was already available [12] is used as an implementation vehicle for the "switched bias technique"[13]. This oscillator has the following properties:

- it combines a high control linearity with low phase noise;
- it features some new concepts resulting in an improved phase noise behaviour. As a result, its phase noise is solely dominated by the (1/f) noise on the currents that periodically charge the oscillator's capacitors;
- the MOS transistors responsible for this 1/f noise are not switched by normal circuit operation;
- the oscillator is built up as a ring of identical stages and exhibits a timing scheme that allows the switched bias technique to be applied.

For sake of clarity, a brief review of the working and characteristics of the oscillator will be given.

VII. The Coupled Sawtooth Oscillator

The coupled sawtooth oscillator exhibits a timing scheme that is compatible with switched biasing: it consists of a ring of identical stages each of which subsequently produces a rising voltage ramp acrosss a capacitor. Its construction is such that only rising edges of the capacitor voltages determine the timing of the resulting period of oscillation. Figure 13 shows the circuit schematic of stage number "n" of a coupled sawtooth oscillator consisting of a ring of six stages. Transistor M_4 supplies the current I_b that is mirrored to become the tail current $I_{b,tail}$ of the differential pair $M_{1,2}$. This differential pair gradually starts charging the capacitor with $I_{b,tail}$ as soon as the capacitor voltage in stage (n-1) reaches the vicinity of the bias level V_{REF1}. Transistor M_3, whose gate is driven by two inverters in series, discharges the capacitor during the time that the capacitor voltage in stage (n+2) is larger than the inverter's decision level V_{REF2} (see Figure 14). Figure 14 shows the capacitor voltage waveforms in a six stage coupled sawtooth oscillator. Notice that each ramp is started gradually. Also shown in Figure 14 are the switching signal $V_{SW(1)}$ produced by the inverters that supply the gate voltage of M_3 in stage 1 (see Figure 13) and a signal $V_{G(1)}$ to be discussed later.

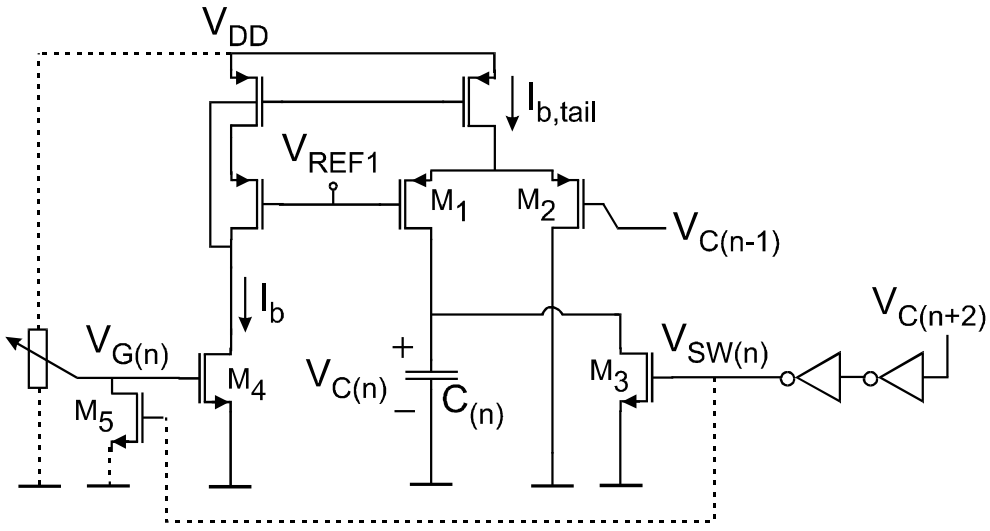

Figure 13 Circuit schematic of section (n) of the coupled sawtooth oscillator

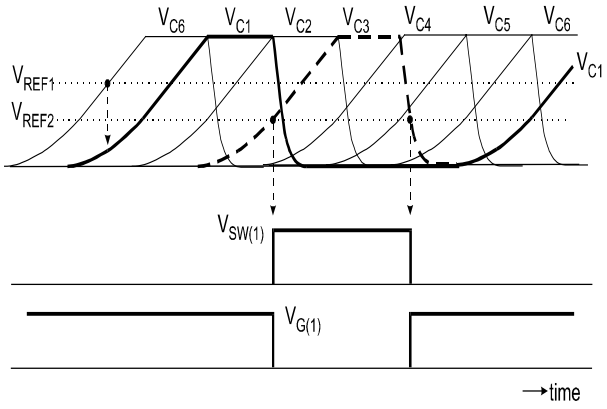

Figure 14 The capacitor voltage waveforms in the six stage coupled sawtooth oscillator and two switching signals Vsw(1) and VG(1) that are used in stage 1 (see Figure 13 with n=1) to respectively discharge C1 and accomplish switched biasing.

In [12] the coupled sawtooth oscillator was introduced as a new controlled oscillator principle that allows low phase noise to be achieved in combination with high control linearity. The phase noise of this type of oscillator is significantly lower (14dB improvement [12]) than that of a conventional regenerative oscillator, compared at equal control linearity and power dissipation. This is achieved by using an alternative for the Schmitt-trigger that is used normally in a regenerative oscillator to periodically reverse the capacitor current each time the capacitor voltage crosses one of the tigger's two threshold levels. The noise present on these decision levels is the dominant contributor to phase noise in a conventional regenerative oscillator [11]. This is due to the fast decisions taken by the trigger circuit, resulting in nearly ideal sampling of the threshold-level noise. As a consequence, the threshold-level noise is converted into phase noise over a large bandwidth.

In the coupled sawtooth oscillator the noise, present on the threshold-level V_{REF1} (see Figure 13 and Figure 14), is effectively filtered by the oscillator's capacitor. This is achieved by *gradually* turning on the capacitor's charge current instead of instantly, as happens in the regenerative oscillator. The simple differential pair $M_{1,2}$ (see Figure 13) performs this task. It is controlled by the capacitor voltage ramp of the previous stage. When this voltage reaches the vicinity of V_{REF1}, the differential pair starts to turn on the charge current. During the gradual transition of the differential pair, noise on V_{REF1} is integrated on the capacitor, thus establishing an effective filtering. Figure 15 gives a qualitative time-domain impression of this filtering. Also shown in this figure is the time error Δt_{trig} that would result if a trigger-circuit is used to instantly start a new capacitor voltage ramp. Its variance is much larger than the variance of the time error Δt_{saw} appearing in the sawtooth oscillator, due to the effective filtering [12].

It can be shown [12] that the gradual start-up of the charge current does not introduce any deterioration of the oscillator's control-linearity, due to the point-symmetrical transfer function of the differential pair.

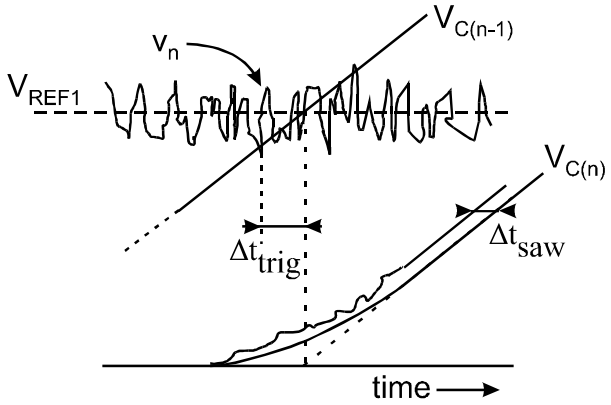

Figure 15 The effective filtering of noise vn on the threshold level VREF1 in the coupled sawtooth oscillator results in a smaller time error Δtsaw compared to the time error Δttrig that would appear in a regenerative oscillator

As a result of the filtering of the threshold-level noise, the (1/f) noise present on the capacitor's charge current now becomes the dominant contributor to (1/f induced) phase noise in the coupled sawtooth oscillator. Thus, in order to further reduce the 1/f induced phase noise of the coupled sawtooth oscillator using the switched bias technique, it has to be applied to the transistors that generate the capacitor currents.

As mentioned before, the (1/f) noise present on the capacitor's charge current $I_{b,tail}$ (see Figure 13) dominates the (1/f noise induced) phase noise of the oscillator. Consequently, the switched-bias technique should be applied to all transistors that contribute 1/f noise to this current. The oscillator's operation allows the current $I_{b,tail}$, and thus the 1/f noise contributing transistors, to be switched off when the capacitor in a particular stage is not producing a rising ramp. The easiest way to implement this is to switch off these transistors at the same time when the capacitor is discharged. In this way no change at all will be noticeable in the capacitor waveforms and the oscillator's timing is not harmed in any way. The signal, necessary to switch the transistors, is supplied by the oscillator itself.

As there appears no change in the capacitor waveforms, no change in the amount of upconversion of 1/f noise is expected [8]. As a result, any change in the 1/f noise induced phase noise when applying the switched bias technique is to be explained by a change in the transistors' 1/f noise.

In the experiments described here, an integrated version of the sawtooth oscillator was used with already available extra bond-outs for capacitors and bias currents. This enables a demonstration of the switched-bias technique. In the IC's available for experiments, not all transistors were accessible that contribute 1/f noise to the current $I_{b,tail}$. In order to demonstrate the feasibility and the result of the switched bias technique in this oscillator, the switched-biasing is applied to an external current-bias transistor M_4 (see Figure 13) which is available on the same die as the oscillator circuit. M_4 has a small W/L =4/0.8 such that its 1/f noise dominates in the current $I_{b(tail)}$.

The dashed lines in Figure 13 show the implementation of the switched biasing in the coupled sawtooth oscillator : transistor M_5 switches off the bias transistor M_4 at the same time when transistor M_3 discharges the capacitor. Figure 14 shows the gate voltage $V_{SW(1)}$ of transistors M_3 and M_5 in stage 1 together with the resulting gate voltage $V_{G(1)}$ of bias transistor M_4.

Due to experimental limitations, the switched bias technique could be applied only to one stage. In the other stages, low noise current sources are used as bias currents for the PMOS current mirrors. The bias current of stage 1 is realized using the before-mentioned transistor

M_4 that hence dominates the 1/f noise induced phase noise of the oscillator. This NMOS transistor is used in both constant bias and switched bias mode, for direct comparison.

VIII. Experimental Results of Switched Bias in Coupled Sawtooth Oscillator

In the experiments, the oscillator runs at f_{osc} = 120kHz. Measurements show no effect of switched biasing on any of the oscillator's capacitor-waveforms. However, a large difference is measured in the phase noise shown in Figure 16: for switched biasing (curve B) the phase noise at 100Hz carrier-offset frequency is about 8dB lower. In contrast to the baseband results of Figure 8 *no 6 dB correction* for duty-cycle effects is necessary here: transistor M_4 is switched off during a time interval in which stage 1 is not contributing to the oscillation period (and thus to phase noise).

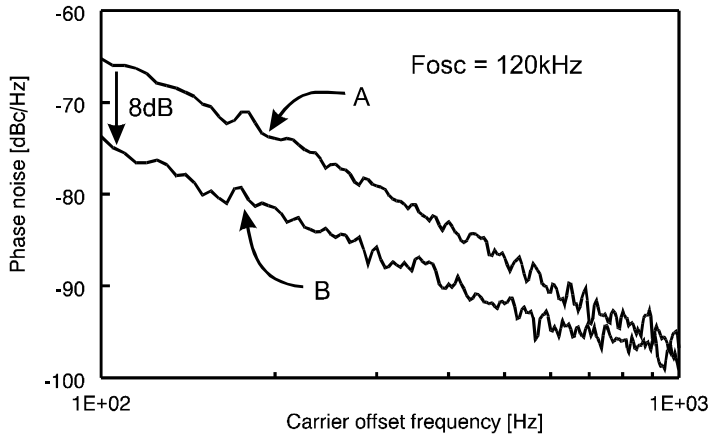

Figure 16 Measured phase noise [dBc/Hz] of the coupled sawtooth oscillator as a function of carrier offset frequency for the constant bias (curve A) and switched bias condition (curve B): 8 dB reduction at 100 Hz.

The experiment shows that switching-off a transistor during phases in which it is not actively contributing to the circuit's operation, helps to reduce its 1/f noise during active phases. In addition, the power consumption in stage 1 is reduced by more than 30%.

Although switched-biasing is applied to just one current source in this experimental circuit, it can of course just as well be applied to the other current sources. As all oscillator sections are identical and contribute to the phase noise equally, the same reduction in phase noise is expected in that case.

This example of applying the switched bias technique in an existing sawtooth oscillator illustrates the power of this technique. It reduces the 1/f induced phase noise as well as the power consumption of the oscillator. While normally lower phase noise is achieved in a circuit by burning *more* power.

IX. Conclusions

The intrinsic 1/f noise of MOS transistors is shown to decrease by periodically switching a transistor from an operational state in strong inversion to a rest state close to accumulation (switched bias technique). It has been shown that this physical effect has a significant effect on the phase noise of CMOS ring oscillator (Phase Noise reduction of 8dB). "Switched Biasing" has been proposed as a circuit technique that exploits intentional on-off switching of MOS transistors with the purpose to reduce their intrinsic 1/f noise. The technique was implemented in a 6-stage coupled sawtooth oscillator [12] running at f_{osc} = 120 kHz. Experiments show that the switched bias technique can be used with benefit: it not only

results in a 30% reduction of power consumption but also in a 8dB reduction of the 1/f noise induced phase noise. As a means to reduce 1/f noise, the authors believe that the switched-bias technique can be made applicable in many other circuits where 1/f noise is of concern.

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